WHAT IS CLAIMED IS:

1. A method of forming an integrated circuit, comprising:

forming a first level sacrificial structure on a first level over a substrate;

forming a first set of spacers along sidewalls of the first level sacrificial structure;

forming a first level filler material at sides of spacers of the first set of spacers, the first level filler material and the first level sacrificial structures defining a first level spacer volume therebetween;

forming a second level sacrificial structure on a second level above the first level sacrificial structure and the first level spacer volume, the second level sacrificial structure crossing a width of the first level sacrificial structure;

forming a second set of spacers along sidewalls of the second level sacrificial structure;

forming a second level filler material at sides of spacers of the second set of spacers;

selectively removing the second set of spacers to expose portions of the first level spacer volume;

selectively removing the exposed material in the first level spacer volume to form openings on the first level;

filling the openings; and

forming a top electrode on a third level over the second level, the electrode extending directly over one or more of the filled openings on the first level.

2. The method of Claim 1, wherein filling the opening comprises forming a phase change material in the opening.

3. The method of Claim 2, wherein selectively removing the second set of spacers defines trenches between the second level sacrificial structures and the second level filler material, wherein filling the openings also fills the trenches with phase change material.

4. The method of Claim 3, further comprising removing the phase change material outside of the openings before forming the top electrode.

5. The method of Claim 3, wherein the top electrode electrically contacts the phase change material filling the trenches and phase change material forms a part of a phase change memory cell.

6. The method of Claim 2, further comprising providing a bottom electrode underlying the first set of spacers, wherein the first set of spacers are formed of a conductor and electrically interconnect the phase change material in the openings to the bottom electrodes.

7. The method of Claim 1, further comprising:

recessing spacers of the first set of spacers after forming the first level filler material and before forming the second level sacrificial structure, thereby defining trenches in the first level spacer volume; and

forming a dielectric material in the trenches,

wherein selectively removing the exposed material removes portions of the dielectric material.

8. The method of Claim 1, wherein forming the first set or second set of spacers comprises:

blanket depositing a layer of spacer material on the first or the second level sacrificial structure; and

subjecting the layer of spacer material to a directional etch to define the first or second set of spacers.

9. A method for forming an integrated circuit, comprising:

providing a first set of spaced-apart lines of sacrificial material separated by dielectric material;

providing a second set of spaced-apart lines of sacrificial material separated by dielectric material, the second set of spaced-apart lines crossing and contacting tops of the first set of spaced apart lines;

selectively removing the second set of spaced-apart lines and portions of the first set of spaced-apart lines at the intersection of the first and second sets of spaced apart lines; and

forming an electrode over a remainder of the first set of spaced apart lines.

10. The method of Claim 9, wherein the integrated circuit is a phase change memory and wherein selectively removing the second set of spaced-apart lines and the portions of the first set of spaced-apart lines defines openings at the intersection of the first and second sets of spaced apart lines, further comprising:

filling the openings with a phase change material.

11. The method of Claim 10, further comprising, after filling the openings, etching material around the opening to define free-standing memory cell stacks separated by open space, wherein each stack comprises an opening filled with the phase change material.

12. The method of Claim 11, further comprising depositing dielectric material in the space separating the stacks.

13. The method of Claim 12, wherein the dielectric material in the space separating the stacks is different from dielectric material separating the first set of spaced-apart lines of sacrificial material.

14. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode;

an upper electrode; and

a conductive line in a channel extending vertically between the bottom and upper electrodes,

the conductive line having a cross-section substantially in a shape of a parallelogram as seen in a top down view, each side of the parallelogram having a length of about 40 nm or less.

15. The integrated circuit of Claim 14, wherein a width of the conductive line, as seen from a top down view, is defined by a width of a spacer volume.

16. The integrated circuit of Claim 14, wherein the length is about 25 nm or less.

17. The integrated circuit of Claim 14, wherein line edge roughness is about 3 nm or less.

18. The integrated circuit of Claim 14, further comprising a phase change material disposed in the channel and extending between the conductive line and the upper electrode.

19. The integrated circuit of Claim 18, wherein the conductive line comprises a resistive heater.

20. The integrated circuit of Claim 19, wherein the resistive heater includes a material chosen from the group consisting of W, Ni, Pt, TiN, TiW, TaN, TaSiN, TiSiN, and NbN.

21. The integrated circuit of Claim 14, wherein the cross-section is substantially in the shape of a square.

22. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode;

an upper electrode; and

a conductive wire extending vertically between the bottom and upper electrodes, the conductive wire disposed within a discrete, laterally elongated insulating region, the conductive wire extending across an entire width of the insulating region.

23. The integrated circuit of Claim 22, wherein a cross-section of the insulating region has a parallelogram shape as seen in a top down view.

24. The integrated circuit of Claim 22, wherein the conductive wire is at least partly formed of phase change material.

25. A memory device, comprising:

a memory cell, the memory cell comprising:

a lower electrode;

a vertically-extending lower conductive plate above and electrically connected to the lower electrode;

a vertically-extending conductive wire above and electrically connected to the lower conductive plate;

a vertically-extending upper conductive plate above and electrically connected to the wire; and

an upper electrode above and electrically connected to the vertically-extending upper conductive plate, the upper and lower conductive plates elongated into crossing directions.

26. The memory device of Claim 25, wherein the conductive wire comprises a phase change material.

CLAIMS

1. A method of forming an integrated circuit, comprising:

forming a first level sacrificial structure on a first level over a substrate;

forming a first set of spacers along sidewalls of the first level sacrificial structure;

forming a first level filler material at sides of spacers of the first set of spacers, the first level filler material and the first level sacrificial structures defining a first level spacer volume therebetween;

forming a second level sacrificial structure on a second level above the first level sacrificial structure and the first level spacer volume, the second level sacrificial structure crossing a width of the first level sacrificial structure;

forming a second set of spacers along sidewalls of the second level sacrificial structure;

forming a second level filler material at sides of spacers of the second set of spacers;

selectively removing the second set of spacers to expose portions of the first level spacer volume;

selectively removing the exposed material in the first level spacer volume to form openings on the first level;

filling the openings; and

forming a top electrode on a third level over the second level, the electrode extending directly over one or more of the filled openings on the first level.

2. The method of Claim 1, wherein filling the opening comprises forming a phase change material in the opening.

3. The method of Claim 2, wherein selectively removing the second set of spacers defines trenches between the second level sacrificial structures and the second level filler material, wherein filling the openings also fills the trenches with phase change material.

4. The method of Claim 3, further comprising removing the phase change material outside of the openings before forming the top electrode.

5. The method of Claim 3, wherein the top electrode electrically contacts the phase change material filling the trenches and phase change material forms a part of a phase change memory cell.

6. The method of Claim 2, further comprising providing a bottom electrode underlying the first set of spacers, wherein the first set of spacers are formed of a conductor and electrically interconnect the phase change material in the openings to the bottom electrodes.

7. The method of Claim 1, further comprising:

recessing spacers of the first set of spacers after forming the first level filler material and before forming the second level sacrificial structure, thereby defining trenches in the first level spacer volume; and

forming a dielectric material in the trenches,

wherein selectively removing the exposed material removes portions of the dielectric material.

8. The method of Claim 1, wherein forming the first set or second set of spacers comprises:

blanket depositing a layer of spacer material on the first or the second level sacrificial structure; and

subjecting the layer of spacer material to a directional etch to define the first or second set of spacers.

9. A method for forming an integrated circuit, comprising:

providing a first set of spaced-apart lines of sacrificial material separated by dielectric material;

providing a second set of spaced-apart lines of sacrificial material separated by dielectric material, the second set of spaced-apart lines crossing and contacting tops of the first set of spaced apart lines;

selectively removing the second set of spaced-apart lines and portions of the first set of spaced-apart lines at the intersection of the first and second sets of spaced apart lines; and

forming an electrode over a remainder of the first set of spaced apart lines.

10. The method of Claim 9, wherein the integrated circuit is a phase change memory and wherein selectively removing the second set of spaced-apart lines and the portions of the first set of spaced-apart lines defines openings at the intersection of the first and second sets of spaced apart lines, further comprising:

filling the openings with a phase change material.

11. The method of Claim 10, further comprising, after filling the openings, etching material around the opening to define free-standing memory cell stacks separated by open space, wherein each stack comprises an opening filled with the phase change material.

12. The method of Claim 11, further comprising depositing dielectric material in the space separating the stacks.

13. The method of Claim 12, wherein the dielectric material in the space separating the stacks is different from dielectric material separating the first set of spaced-apart lines of sacrificial material.

14. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode associated with a first set of spaced-apart lines of sacrificial material that interconnect with the bottom electrode;

an upper electrode associated with a second set of spaced-apart lines of sacrificial material, wherein the second set of spaced-apart lines cross and contact a portion of the first set of spaced-apart lines; and

a conductive line in a channel extending vertically between the bottom and upper electrodes,

the conductive line having a cross-section including a remainder portion of the first set of spaced-apart lines present after a removal of the second set of spaced-apart lines and a removed portion of the first set of spaced-apart lines at the cross-section.

15. The integrated circuit of Claim 14, wherein a width of the conductive line, as seen from a top down view, is defined by a width of a spacer volume.

16. The integrated circuit of Claim 14, wherein the cross-section is substantially in a shape of a parallelogram, a side of the parallelogram having a length of about 25 nm or less.

17. The integrated circuit of Claim 14, wherein line edge roughness is about 3 nm or less.

18. The integrated circuit of Claim 14, further comprising a phase change material disposed in the channel and extending between the conductive line and the upper electrode.

19. The integrated circuit of Claim 18, wherein the conductive line comprises a resistive heater.

20. The integrated circuit of Claim 19, wherein the resistive heater includes a material chosen from the group consisting of W, Ni, Pt, TiN, TiW, TaN, TaSiN, TiSiN, and NbN.

21. The integrated circuit of Claim 14, wherein the cross-section is substantially in the shape of a square.

22. An integrated circuit, comprising:

a memory cell, comprising:

a bottom electrode;

an upper electrode; and

a conductive wire extending vertically between the bottom and upper electrodes, the conductive wire disposed within a discrete, laterally elongated insulating region, the conductive wire extending across an entire width of the insulating region,

wherein a cross-sectional area at a height of the conductive wire includes a remainder portion of a first set of spaced-apart lines associated with the bottom electrode, the remainder portion being present after a removal of a second set of spaced-apart lines associated with the upper electrode and a removed portion of the first set of spaced-apart lines at the height.

23. The integrated circuit of Claim 22, wherein a cross-section of the insulating region has a parallelogram shape as seen in a top down view.

24. The integrated circuit of Claim 22, wherein the conductive wire is at least partly formed of phase change material.

25. A memory device, comprising:

a memory cell, the memory cell comprising:

a lower electrode;

a vertically-extending lower conductive plate above and electrically connected to the lower electrode;

a vertically-extending conductive wire above and electrically connected to the lower conductive plate;

a vertically-extending upper conductive plate above and electrically connected to the wire; and

an upper electrode above and electrically connected to the vertically-extending upper conductive plate, the upper and lower conductive plates elongated into crossing directions,

wherein a cross-sectional area at a height of the conductive wire includes a remainder portion of a first set of spaced-apart lines associated with the bottom electrode, the remainder portion being present after a removal of a second set of spaced-apart lines

associated with the upper electrode and a removed portion of the first set of spaced-apart lines at the height.

26. The memory device of Claim 25, wherein the conductive wire comprises a phase change material.