

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic timepieces of the kind comprising a time standard oscillator and at least one divider chain for dividing down the output frequency of said oscillator to produce time signals for the display of time. Although an important application of the invention is to electronic timepieces having at least two divider chains associated with the same time standard, one for producing time signals for the display of time down to a smallest unit of one magnitude and the other or others for producing time signals for the display of time down to a unit, or units of smaller magnitudes—i.e. for producing one or more so-called "chronograph" time displays—the invention is not limited to this application but may be applied to timepieces without chronograph time display provision.

According to this invention there is provided an electronic timepiece comprising a time standard oscillator, a binary divider chain and at least one counter chain fed from said divider chain wherein said counter chain includes a counter consisting of a logic circuit to which a predetermined output from the binary divider chain is applied as input and which produces output pulses at a frequency of approximately 10^K Hz (where K is an integral number), and control means operative automatically to control the effective division ratio of said counter so as to cause a predetermined number of said periodic output pulses from said counter to be supplied in a time interval which is integrally related to a 1 second signal period.

Preferably the time standard oscillator is a quartz crystal oscillator.

The timepiece may have a single time standard oscillator, a binary divider chain and at least two counter chains fed from said divider chain, at least one of said counter chains including a counter consisting of a logic circuit to which a predetermined output from the binary divider chain is applied as input and which produces output pulses at a frequency of 10^K Hz (where K is an integral number), the effective division ratio of said counter being automatically so controlled that a predetermined number of said periodic output pulses from said counter is supplied in a time interval which is integrally related to a 1 second signal period, and the quartz crystal oscillator being the only time standard oscillator of the timepiece.

The effective division ratio of the counter consisting of a logic circuit is varied in response to the internal state of the counter chain which includes said counter.

The time standard oscillator is preferably a quartz crystal oscillator having a nominal natural vibration frequency of 2^n Hz, where n is an integer.

The time interval in which the predetermined number of pulses is supplied from the counter which consists of a logic circuit may be exactly 1 second and there may be two counter chains one of which constitutes a time counter circuit supplying signals for the display of time in units of which the smallest is 1 second, the other counter chain constituting a time counter circuit supplying signals for the display of time in units of which the smallest is smaller than 1 second and in decimal relationship therewith.

The frequency of the pulses produced by the counter which consists of a logic circuit may be, for example, approximately 10 Hz or approximately 100 Hz or approximately 1000 Hz, depending upon the magnitude of the smallest displayable time unit required.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:—

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Figures 1, 2 and 3 are diagrammatic representations of timepieces which are not embodiments of the invention, these Figures being provided for purposes of preliminary explanation: Figures 6 and 7 illustrate embodiments of the invention; Figure 11 shows, in some detail circuitry which may be used in part of the embodiment of Figure 6; and the remaining Figures are explanatory graphical figures.

Figure 1 shows a known conventional electronic timepiece. It has a time standard oscillator 2 provided with a quartz crystal vibrator having a natural frequency of 2^n Hz (typically $2^{16} = 32768$ Hz). The output from this oscillator is divided down to 1 second signals by a divider 3 the output from which is fed to successive counters 106, 105, . . . 102, and 101 to give signals at required different longer intervals. As indicated in Figure 1 the counters 106 and 105 respectively pass on to the immediately following counter 10 sec and 60 sec (1 min) signals. The count in the counters actuate corresponding drive circuits 206, 205, . . . 201 driving displays 306, 305, . . . 301 which indicate time digitally. In the construction shown in Figure 1, the smallest displayable time unit is 1 second. If the displayable smallest time is required to be smaller e.g. 0.1 second or 0.01 second usual practice is to use a crystal of suitably increased frequency in the quartz crystal oscillator. This practice is illustrated by Figure 2 for the case, given by way of example, in which the smallest displayable time unit is 0.1 second. Here the crystal, referenced 4 in Figure 2 has a natural frequency of 40960 Hz so that this frequency is produced from the oscillator circuit which is referenced 5 in Figure 2. This frequency is divided by a frequency divider 6 of such ratio as to produce from the output of the oscillator 5 a 1/10th sec signal which is fed to a counter 107 which counts tenths of a second and operates a driving circuit 207 and a one-tenths sec display 307. The remainder of Figure 2 is the same as in Figure 1 to provide a display of seconds, minutes . . . and required other units of time.

Figure 3 shows a known electronic timepiece having two counter chains for providing two different smallest displayable time units. Both are operated by the same time standard oscillator. The time standard crystal 4 has a natural frequency of 40960 Hz and the output at this frequency from the oscillator 5 is divided down by the divider 6 to 10 Hz. The output of this divider 6 is applied on the one hand to what may be termed a chronograph counter chain consisting of counters 407, 406, . . . 402 and 401 and on the other hand to what may be termed the time counter chain consisting of a divider 7 followed by counters 10, 105 . . . 101. As

the input to both counter chains is the same frequency, namely 10 Hz, (0.1 signals), counting, driving and display are performed in the same manner as shown in Figure 2. In the case of the chronograph counter chain there are counters 407, 406, . . . 402 and 401, operating drive circuits 507, 506, 505 . . . 501 and displays 607, 606, 605 . . . 601 and giving a smallest time display unit of 0.1 sec. In the other chain the divider 7, which is a 1/10 divider, generates a 1 sec signal output which is applied to the counter chain 106, 105, . . . 102 and 101 to perform counting driving and display in the same manner as in the case shown in Figure 1.

The known arrangement of Figure 3 has a number of important defects from the point of view of practical manufacturing.

1) Because the smallest displaying time unit is other than 1 second, (0.1 second in the particular example given) and, in general manufacturing practice with electronic timepieces, the most usual displayable time unit is 1 second, the most generally manufactured and available quartz crystal vibrators, which are those having a natural frequency of 2^n Hz, cannot be used unaltered to provide the required smaller displaying unit (0.1 sec).

2) If the two counter chains, each of which provides a different lowest displayable time unit are driven by the same quartz crystal vibrator having a frequency other than 2^n Hz, as in the case in Figure 3, one of the two counter chains is not to effectively used as is desirable for, although the divider 7 in Figure 3 is capable of dealing with a 16-pulse count because it generally comprises 4-bit flip-flops, what is usable in this case is only a 10-pulse count.

Defect (1) above is particularly significant from the viewpoint of manufacture. The reason of this is as follows. When quartz crystal vibrators of a certain intended natural frequency f_0 are manufactured, there is, as is well known, a liability to the occurrence, in manufacture, of a frequency error Δf the distribution of which is, in general, as shown graphically in Figure 4. In this figure f_{02} is the natural frequency of the quartz crystal, N is the number of crystals produced and δ is the standard deviation. From the viewpoint of timepiece manufacturing the less the variation of the error Δf from one crystal to another the more easily can accuracy be obtained from the timepieces can be improved and the more easily can adjustment thereof at an early stage of manufacture be achieved. Thus less the variation of Δf the better the production which can be achieved. The standard deviation δ is a measure of the variation of error Δf and is apt to decrease in accordance with increase in the quantity of manufactured quartz crystal vibrators not proportioned thereof. Figure 5 is a graph illustrating

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5 this for the case of quartz crystal vibrators having a centre frequency of 32768 Hz, and showing variation of the standard deviation of sampled vibrators in relation to actually manufactured quantity converted into error of frequency. N is the number of crystals produced monthly, Δf is the error of frequency which is proportional to the standard deviation. As shown in Figure 5, when the quantity, in thousands of crystals manufactured per month, goes up by one figure, the standard deviation is improved by one figure. And it has been found that this tendency continues when the numbers of crystals manufactured exceed 10000. Accordingly, when quartz crystal vibrators for timepieces are manufactured, it is of very substantial advantage from the viewpoint of production and timepiece manufacturing technique to manufacture large numbers of crystals to one frequency—the larger the quantity the better. The second of the two defects previously mentioned is of principal disadvantage in militating against economical construction of integrated circuitry.

25 As already mentioned the quartz crystal vibrators generally manufactured in the largest numbers for use in electronic timepieces are those having natural frequencies of 2^n Hz.

30 The present invention, an embodiment of which will be later herein described with reference to Figure 6 seeks to take the foregoing manufacturing considerations into account to best advantage.

35 Referring to Figure 6, the timepiece therein represented has a time standard oscillator 9 with a quartz crystal vibrator 8 of 32768 Hz ($=2^{15}$ Hz), output of oscillator 9 is divided down by a divider 10 to an output of 128 Hz (1/128 second signal) which is branched out into two. One of these outputs is fed to what is herein termed a time counter chain consisting of a divider 11 and counters 106, 105, . . . 102 and 101. The other is fed to what is herein termed a chronograph counter chain consisting of a divider 12 and counters 407, 406, . . . 403, . . . The 128 Hz signal applied to the time counter chain is divided down to 1 Hz (1 second) signals by the divider 11 and applied to the counter 106. The subsequent counting, driving and display

following divider 11 are performed in the similar manner as shown in Figure 1, 206, 205, . . . 201 being the driving circuits and 306, 305 . . . 301 being the display units for the displays displaying time down to 1 sec corresponding to the counters 106, 105, . . . 101, respectively.

The 128 Hz signal applied to what is herein termed the chronograph counter chain is divided down to about 10 Hz by the divider 12, the output from which is further divided down to 1 Hz (a 1 sec. signal) by the counter 407. This divider 12 is a 1/12—1/13 variable divider circuit whose control input S_c is applied from the output of a control gate circuit 13 which detects the condition of the counter 407 and responds in such manner as to cause the divider 12 to operate alternately as a 1/12 or as a 1/13 divider at certain different timings. This control gate circuit 13 is adjusted to operate to effect control satisfactorily provided that the quartz crystal is within a specified tolerance range of peripheries. Figure 8 shows the actual timings. Line M(407) in Figure 8 shows the counting mode of the counter 407. The line NC shows ten conditions from "1" to "10". Line CR shows the counting rate of the divider 12 for each of these ten conditions. As will be seen CR is 12 when NC is 3 or 8, and is 13 in other conditions. A cycle of the conditions 1 to 10 and therefore a cycle of changes of the division ratio of divider 12 takes place over a period in which 128 pulses are fed into 12. Therefore the feeding in to the divider 12 of the 1/128 sec signal results in the production of an exact 1 second signal from counter 407. Figure 9 shows part of the operation graphically to an enlarged time scale. Line IN (12) is the 1/128 sec input to 12; line OUT (12) is the output from divider 12; and line M shows the signal sent from the counter 407 to 13. Each of the ten conditions of the counter 407 corresponds to each 1/10 second unit, and the conditions change in response to the output timings of the divider 12, substantially coincidentally with each 1/10 second timing approximately. The error at each of 1/10 second timings is as given by the following table:—

1/10 timing	approximate error	1/10 timing	approximate error
1/10	-0.00156	6/10	-0.00156
2/10	-0.00312	7/10	-0.00312
3/10	+0.00312	8/10	+0.00312
4/10	+0.00156	9/10	+0.00156
5/10	zero	10/10	zero

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In the table the minus signs are indicative of delay and the plus signs are indicative of advance with respect to a precise 1/10 timing.

As will be apparent from the table the error is not a cause of practical trouble and it is significant that the error becomes zero every 5/10 second and 10/10 second, and is not accumulated.

Figure 7 shows sufficiently to an understanding thereof another embodiment of the invention. In this embodiment the timings of the divider 11 in the time counter chain are controlled. Figure 10 shows the timings in manner similar to that of Figure 8. In Figure 10 line M(707) shows the mode of condition of the counter 707. In this case, it may be shown that the maximum error is 0.014 second. This arrangement is not applicable to a timepiece whose time counter chain is provided with a zero-set function for units of 1 second or less and, to this extent, the embodiment of Figure 7 is not so good as that shown in Figure 6.

Figure 11 shows in more detail circuitry for carrying out the method of operation adopted in the embodiment of Figure 6. Here 15 is a counter (such as the counter 407 of Figure 6); 16 is a variable divider (such as the divider 12 of Figure 6); and 17 is a control gate circuit (such as the circuit 13 of Figure 6 and adjusted similarly). The counter 15 is constituted by data-type flip-flops 18, 19, 20 and 21 and decimal gates 22 and 23. The variable divider 16 is constituted by flip-flops 24, 25, 26 and 27. The gate control circuit 17 is constituted by gates 28, 29, 30 and 31 and an R—S flip-flop consisting of gates 32 and 33. W, CL, Q, $\bar{Q}$ and R are, respectively, a writing input, a clock input, a positive input, a negative output and a reset input for the data-type flip-flops; 22, 23, 31, 32 and 33 are NOR gates. 28 is a NAND gate, 29 and 30 are AND gates. When an output O (28) of the gate 28 is "negative", the divider 16 counts up to the end of condition 3 and then condition 4 is reached, an output O (30) of the gate 30 turning "positive", inverting the R—S flip-flop consisting of the gates 32 and 33 to turn the output R "positive" so that the flip-flops 24 to 27 of the divider 16 are reset and return to zero. The output O (30) of the gate 30 is thus turned "negative", and the R—S flip-flop is instantaneously reset by an input IN (16) of the divider 16 to turn the output R "negative". In the case in which the state of the counter 15 is such that the Q output of the flip-flop 18 is "negative" and the Q output of the flip-flop 19 is "positive", the output O (28) of the gate 28 turns "positive" when the divider 16 is in condition 3. Then the divider 16 is reset and operates as a 1/12 divider. As the state of the counter 15 is such that the Q output of the flip-flop 18 is "negative" and the Q output

of the flip-flop 19 is "positive" only when either condition "3" or condition "8" (among the possible ten conditions) applies, the divider 16 acts as a 1/12 divider only in conditions 3 and 8 and as a 1/13 divider in all other conditions. Figure 12 is a timing chart explanatory of the operation of the circuit of Figure 11. In Figure 12 lines QC₁, QC₂, QC₃ and QC₄ show respectively the waveforms of the outputs of the flip-flops 18, 19, 20 and 21 of the counter 15. In Figure 13 which is drawn to a larger time scale, QD₁, QD₂, QD₃ and QD₄ show respectively the waveforms of the outputs of the flip-flops 24, 25, 26 and 27 of the divider 16.

As will now be seen this invention enables an output which is closely approximate to 10 Hz to be obtained from a standard 128 Hz signal. If as may sometimes be the case a waveform with a 50% duty cycle is required as the output OUT (16) from the divider 16, this may be achieved by setting the standard signal at 256 Hz (or more) instead of 128 Hz and adding the necessary number of binary dividing stages to the divider 16 of Figure 11.

Although, in the illustrated embodiments above described, an approximate 10 Hz signal is obtained from the 128 Hz signal, the invention may be employed to obtain signals of other frequencies in a similar manner—for example, an approximate 100 Hz signal from a standard 4096 Hz signal or an approximate 1000 Hz signal from a standard 131076 Hz signal.

Again, although the invention has been particularly described as applied to a timepiece having two counter chains producing time signals corresponding to two difficult smallest displayable time units and driven from the same time-standard source, the invention is not limited to this application but could equally well be applied to a timepiece having only one counter chain producing time signals corresponding to one smallest displayable time unit which is other than 1 sec e.g. 0.1 sec or 0.01 sec and would be of obvious advantage when so applied.

The invention thereof lends admirably to the use of integrated circuitry and its use as described in a counter circuit in an electronic timepiece simplifies and cheapens production of such timepieces and their adjustment after manufacture of the time standard quartz crystal employed. The invention is particularly advantageous for small compact timepieces such as wrist watches. An important and characteristic advantage of the invention, is that, despite the use of what may be termed an approximate divider, the accumulated error due to such use tends to zero.

WHAT WE CLAIM IS:—

1. An electronic timepiece comprising a

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of the flip-flop 19 is "positive" only when either condition "3" or condition "8" (among the possible ten conditions) applies, the divider 16 acts as a 1/12 divider only in conditions 3 and 8 and as a 1/13 divider in all other conditions. Figure 12 is a timing chart explanatory of the operation of the circuit of Figure 11. In Figure 12 lines QC₁, QC₂, QC₃ and QC₄ show respectively the waveforms of the outputs of the flip-flops 18, 19, 20 and 21 of the counter 15. In Figure 13 which is drawn to a larger time scale, QD₁, QD₂, QD₃ and QD₄ show respectively the waveforms of the outputs of the flip-flops 24, 25, 26 and 27 of the divider 16.

As will now be seen this invention enables an output which is closely approximate to 10 Hz to be obtained from a standard 128 Hz signal. If as may sometimes be the case a waveform with a 50% duty cycle is required as the output OUT (16) from the divider 16, this may be achieved by setting the standard signal at 256 Hz (or more) instead of 128 Hz and adding the necessary number of binary dividing stages to the divider 16 of Figure 11.

Although, in the illustrated embodiments above described, an approximate 10 Hz signal is obtained from the 128 Hz signal, the invention may be employed to obtain signals of other frequencies in a similar manner—for example, an approximate 100 Hz signal from a standard 4096 Hz signal or an approximate 1000 Hz signal from a standard 131076 Hz signal.

Again, although the invention has been particularly described as applied to a timepiece having two counter chains producing time signals corresponding to two difficult smallest displayable time units and driven from the same time-standard source, the invention is not limited to this application but could equally well be applied to a timepiece having only one counter chain producing time signals corresponding to one smallest displayable time unit which is other than 1 sec e.g. 0.1 sec or 0.01 sec and would be of obvious advantage when so applied.

The invention thereof lends admirably to the use of integrated circuitry and its use as described in a counter circuit in an electronic timepiece simplifies and cheapens production of such timepieces and their adjustment after manufacture of the time standard quartz crystal employed. The invention is particularly advantageous for small compact timepieces such as wrist watches. An important and characteristic advantage of the invention, is that, despite the use of what may be termed an approximate divider, the accumulated error due to such use tends to zero.

WHAT WE CLAIM IS:—

1. An electronic timepiece comprising a



time standard oscillator, a binary divider chain and at least one counter chain fed from said divider chain wherein said counter chain includes a counter consisting of a logic circuit to which a predetermined output from the binary divider chain is applied as input and which produces output pulses at a frequency of approximately 10^K Hz (where K is an integral number) and control means operative automatically to control the effective division ratio of said counter so as to cause a predetermined number of said periodic output pulses from said counter to be supplied in a time interval which is integrally related to a 1 second signal period.

2. A timepiece as claimed in claim 1 wherein there is a single time standard oscillator, a binary divider chain and at least two counter chains fed from said divider chain, at least one of said counter chains including a counter consisting of a logic circuit to which a predetermined output from the binary divider chain is applied as input and which produces output pulses at a frequency of approximately 10^K Hz, a predetermined number of said periodic output pulses from said counter being supplied in a time interval which is integrally related to a 1 second signal period.

3. A timepiece as claimed in claim 1 or 2 wherein the time standard oscillator is a quartz crystal oscillator.

4. An electronic timepiece as claimed in any of the preceding claims wherein the effective division ratio of said counter is varied in response to the internal state of the counter chain which includes said counter.

5. An electronic timepiece as claimed in any of the preceding claims wherein the time standard oscillator is a quartz crystal oscillator having a nominal natural vibration frequency of 2^n Hz, where n is an integer.

6. A timepiece as claimed in any of the preceding claims wherein the time interval in which the predetermined number of pulses is supplied from the counter which consists of a logic circuit is 1 second.

7. A timepiece as claimed in claims 2 and 5 wherein one of the counter chains constitutes a time counter circuit supplying signals for the display of time in units of which the smallest is 1 second, the other counter chain constituting a time counter circuit supplying signals for the display of time in units of which the smallest is smaller than 1 second and in decimal relationship therewith.

8. A timepiece as claimed in any of the preceding claims wherein the frequency of the pulses produced by the counter which consists of a logic circuit is approximately 10 Hz.

9. A timepiece as claimed in any of the preceding claims wherein the frequency of the pulses produced by the counter which consists of a logic circuit is approximately 100 Hz.

10. A timepiece as claimed in any of the preceding claims wherein the frequency of the pulses produced by the counter which consists of a logic circuit is approximately 1000 Hz.

11. Electronic timepieces having time standard pulse counting means substantially as herein described and illustrated in Figures 6 and 7 of the accompanying drawings.

12. Electronic timepieces substantially as hereinbefore described with reference to Figures 6 to 13 inclusive of the accompanying drawings.

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