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HYBRID DIELECTRIC STRUCTURE FOR IMPROVING THE STIFFNESS OF BACK END OF THE LINE STRUCTURES

FIELD OF THE INVENTION

This invention relates to a multi-level, coplanar interconnect structure on an integrated circuit and, more particularly, to a hybrid dielectric structure for improving stiffness of back end of the line structures.

BACKGROUND OF THE INVENTION

Continued improvement in integrated circuit density is due, in part, to advances in interconnection technology. IC manufacturing generally includes front end of the line (FEOL) and back end of the line (BEOL) processes. The FEOL processes relate to formation of transistors and capacitors and the like along with polysilicon gate layers. BEOL processes include steps to form metal interconnects and associated dielectrics. Conventional interconnect structures used aluminum for conductors. The aluminum was deposited as a film and then patterned to form interconnects. The dielectric insulation material was then added and planarized.

More recently, processes using copper interconnects have been developed. One such process uses damascene copper electroplating for chip interconnections. This process initially forms a planar insulation layer. The insulation layer is etched to form trenches or vias which are then filled with metal and polished to planarize. In a dual damascene process two patterns are combined into one.



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The transition from aluminum to copper interconnects has resulted in reduction in resistance of interconnects. To reduce RC noise, dielectric materials having low dielectric constants (also referred to as "low k") are now being integrated into BEOL structures. However, low k dielectric materials are not generally structural in nature. They can not support applied loads encountered during wire bonding or ball bonding without adversely affecting the electrical reliability of the device. However, these changes must be addressed as the industry changes from quartz which has a high elastic modulus to low modulus materials used as dielectrics.

The present invention is directed to overcoming one or more of the problems discussed above, in a novel and simple manner.

SUMMARY

According to a first aspect of the invention, there is provided a multi-level, coplanar interconnect structure on an integrated circuit chip, comprising a planar line layer having plural interconnect conductors separated by a dielectric material having a dielectric constant less than 4.0 and an elastic modulus less than 75 GPa and a planar via layer comprising a dielectric film having an elastic modulus higher than in the line layer and conductive vias therethrough, wherein one of the line and via layers is on an integrated circuit substrate and defines a first layer and another of the line and via layers is on the first layer so that the vias in the via layer are selectively in contact with the conductors in the line layer.

According to a second aspect of the invention, there is provided a multi-level, coplanar copper damascene interconnect structure on an integrated circuit chip, comprising a first planar interconnect layer on an integrated circuit substrate and having plural line conductors separated by a dielectric material having a dielectric constant less than 4.0 and an elastic modulus less than 75 GPa; a second planar interconnect layer on the first planar interconnect layer comprising a dielectric film having an elastic modulus higher than in the first planar interconnect layer and conductive vias therethrough, the vias in the second layer being selectively in contact with the line conductors in the first layer and a third planar interconnect layer on the second planar interconnect layer and having plural line conductors

separated by the dielectic material and selectively in contact with the vias in the second layer.

According to a final aspect of the invention, there is provided a multi-level, coplanar interconnect structure on an integrated circuit chip, comprising a planar line layer having plural interconnect conductors all separated by a dielectric material having a dielectric constant less than 4.0 and a planar via layer comprising an inorganic dielectric film having a dielectric constant less than 4.0 and conductive vias therethrough, wherein one of the line and via layers is on an integrated circuit substrate and defines a first layer having an upper horizontal planar surface and another of the line and via layers has a lower horizontal planar surface on the first layer upper horizontal planar surface so that the vias in the via layer are selectively in contact with the conductors in the line layer and all interfaces between the dielectric material and the dielectric film are horizontal, and wherein

the dielectric material has a lower elastic modulus than the dielectric film.

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Further features and advantages of the invention will be readily apparent from the specification and from the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view illustrating a multi-level, coplanar interconnect structure in accordance with the invention used on an integrated circuit chip; and

Figs. 2-4 illustrate the process for fabricating the interconnect structure of Fig. 1.

DETAILED DESCRIPTION OF THE INVENTION

As aspect ratios for copper interconnects are increased with next-generation devices, crosstalk between lines is most likely between lines on the same line level, and less likely to occur between lines existing on different line levels, i.e., capacitance across a via level. In accordance with the invention, dielectric materials having low k dielectric constants separate lines on a given line level. At the via levels, where copper density is insignificant, stiffness is increased by using higher modulus dielectric materials at the via levels.

Referring initially to Fig. 1, an integrated circuit chip 10 is illustrated having a multi-level, coplanar interconnect structure 12 in accordance with the invention. The interconnect structure includes a first planar layer 14 on a substrate 16. A second planar layer 18 is on the first planar layer 14. Finally, a third planar layer 20 is on the second planar layer 18.

The substrate 16 comprises a silicon integrated circuit with underlying electronic devices. The first planar layer 14 comprises a line layer. The second planar layer 18 comprises a via layer. The third planar layer 20 comprises a line layer.

The line layers 14 and 20 have plural interconnect conductors 22 separated by a dielectric material 24. The via layer 18 comprises a dielectric film 26 having plural conductive vias 28 therethrough. The vias 28 are in selective contact with certain ones of the conductors 22. As is apparent, the particular connections are determined as required by the design of the integrated circuit chip 10.

In accordance with the invention, the dielectric material 24 in the line layers 14 and 20 comprises a low k and low elastic modulus dielectric. The dielectric film 26 in the via layer 18 has a moderately low k dielectric constant and a higher elastic modulus. A conventional dielectric material used in integrated circuits is silicon dioxide which has a dielectric constant k=4.0 and an elastic modulus of about 75 GPa. In the illustrated embodiment of the invention, the dielectric constant at the line levels 14 and 20 are lower than 4.0 and advantageously lower than 3.0 and an elastic modulus is less than 20 GPa. In the illustrated embodiment of the invention, the dielectric material 24 may comprise a SiLK semiconductor dielectric resin from the Dow Chemical Company. SiLK is a polyarylene ether spun on organic material cured to form an insulating film. Alternatively, the dielectric material 24 may be an inorganic material. SiLK has a dielectric constant of k=2.65. The dielectric film 26 may comprise, for example, an inorganic thin film such as SiCOH which has a dielectric constant of k=2.7. In accordance with the invention, a higher dielectric constant material could be used for the film 26 in the via layer18, including SiO_2. However, the higher k material is not used in the line layers 14 or 20.

Referring to Figs. 2-4, the process of forming the interconnect structure 12 is illustrated. Fig. 2 illustrates the substrate 16 including the first layer 14, comprising the line layer, thereon. The layer 14 includes one of the copper interconnect conductors 22 and the dielectric material 24. In the illustrated embodiment of the invention, as discussed above, the dielectric material 24 comprises SiLK which is spun on and cured to form an insulating film. The interconnect line conductor 22 is then formed using conventional copper damascene

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processing. A barrier layer 30 overlies the first layer 14. The inorganic dielectric thin film 26 is then deposited on the first layer 14 using plasma-enhanced chemical vapor deposition (PECVD) of SiCOH. A via opening 32 is then formed using conventional patterning and etching techniques.

Referring to Fig. 3, the SiLK dielectric material 24 is spun on and cured. As illustrated, a void 34 may be formed in the via opening 32. A hard mask cap layer 36 is formed on top of the SiLK 24 and then a photo-resist layer 38 is patterned according to the conductor line pattern to be formed. Referring to Fig. 4, a SiLK etch is performed to remove the SiLK dielectric material 24 in the non-patterned area. A different gas is used to remove the barrier layer 30 underlying the via opening 32. The dual-damascene process can then be used to electroplate the conductive vias 28 at the via level 18 and the line conductors 22 in the third planar layer 20.

As is apparent, the interconnect structure 12 could use additional line layers and/or via layers. Likewise, the first layer could be a via layer and the second layer a line layer, etc., according to chip requirements.

Thus, the present invention is particularly directed toward use of dual low-dielectric constant materials with copper damascene interconnects. Each dielectric is used in a planar film, deposited on a planar surface. Each gap between the interconnects on a planar level, regardless of spacing, is filled with the same low k material. All interfaces between different dielectrics are purely horizontal. A higher k material may be used at the via level, but not between the interconnect conductors, in accordance with the invention.

WE CLAIM:

1. A multi-level, coplanar interconnect structure on an integrated circuit chip, comprising:

a planar line layer having plural interconnect conductors separated by a dielectric material having a dielectric constant less than 4.0 and an elastic modulus less than 75 GPa; and

a planar via layer comprising a dielectric film having an elastic modulus higher than in the line layer and conductive vias therethrough, wherein

one of the line and via layers is on an integrated circuit substrate and defines a first layer and another of the line and via layers is on the first layer so that the vias in the via layer are selectively in contact with the conductors in the line layer.

2. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric film has a dielectric constant less than 4.0.

3. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric material has a dielectric constant less than 3.0.

4. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric material comprises a polyarylene ether material.

5. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric material comprises an organic material.

6. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric film comprises an inorganic thin film.

7. The multi-level, coplanar interconnect structure of claim 1 wherein the dielectric film comprises SiCOH film.

8. The multi-level, coplanar interconnect structure of claim 1, wherein:

said plural interconnect conductors are all separated by said dielectric material;

said first layer has an upper horizontal planar surface;

said another of the line and via layer has a lower horizontal planar surface on the first layer upper horizontal planar surface; and

all interfaces between the dielectric material and the dielectric film are horizontal.

9. A multi-level, coplanar copper damascene interconnect structure on an integrated circuit chip, comprising:

a first planar interconnect layer on an integrated circuit substrate and having plural line conductors separated by a dielectric material having a dielectric constant less than 4.0 and an elastic modulus less than 75 GPa;

a second planar interconnect layer on the first planar interconnect layer comprising a dielectric film having an elastic modulus higher than in the first planar interconnect layer and conductive vias therethrough, the vias in the second layer being selectively in contact with the line conductors in the first layer; and

a third planar interconnect layer on the second planar interconnect layer and having plural line conductors separated by the dielectic material and selectively in contact with the vias in the second layer.

10. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric film has a dielectric constant less than 4.0.

11. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric material has a dielectric constant less than about 3.0.

12. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric material comprises an polyarylene ether material.

13. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric material comprises an organic material.

14. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric film comprises an inorganic thin film.

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15. The multi-level, coplanar damascene interconnect structure of claim 9 wherein the dielectric film comprises SiCOH film.

16. A multi-level, coplanar interconnect structure on an integrated circuit chip, comprising:

a planar line layer having plural interconnect conductors all separated by a dielectric material having a dielectric constant less than 4.0; and

a planar via layer comprising an inorganic dielectric film having a dielectric constant less than 4.0 and conductive vias therethrough, wherein

one of the line and via layers is on an integrated circuit substrate and defines a first layer having an upper horizontal planar surface and another of the line and via layers has a lower horizontal planar surface on the first layer upper horizontal planar surface so that the vias in the via layer are selectively in contact with the conductors in the line layer and all interfaces between the dielectric material and the dielectric film are horizontal, and wherein

the dielectric material has a lower elastic modulus than the dielectric film.

17. The multi-level, coplanar interconnect structure of claim 16 wherein the dielectric material and the dielectric film each have a dielectric constant less than 3.0.

18. The multi-level, coplanar interconnect structure of claim 16 wherein the dielectric material has an elastic modulus less than 20 GPa.