

ABSTRACT OF THE DISCLOSURE



162162

CLOCK ENABLE CIRCUIT FOR USE IN A HIGH SPEED
REPROGRAMMABLE DELAY LINE INCORPORATING
GLITCHLESS ENABLE/DISABLE FUNCTIONALITY

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A clock qualification circuit (50) used to selectively enable a clock edge to transfer new delay data from a first-in-first-out (FIFO) circuit (14) in a precision delay line circuit (11). The circuit (50) qualifies the clock without generating undesirable pulses (glitches) and causing false loading of new delay data in a timing on the fly delay line implementation.

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Figure 4



G00002