(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 September 2007 (13.09.2007)

PCT

(10) International Publication Number
WO 2007/103343 A1

(51) International Patent Classification:
H01L 21/033 (2006.01) *H01L 21/311* (2006.01)
H01L 21/308 (2006.01) *H01L 21/3213* (2006.01)

(21) International Application Number:
PCT/US2007/005639

(22) International Filing Date: 5 March 2007 (05.03.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/372,825 9 March 2006 (09.03.2006) US

(71) Applicant *(for all designated States except US)*: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **ABATCHEV, Mirzafer, K.** [RU/US]; 6349 S. Mangrove Place, Boise, Idaho 83716 (US). **SUBRAMANIAN, Krupakar, Murali** [IN/US]; 5541 S. Fuchsia Place, Boise, Idaho 83716 (US). **ZHOU, Baosuo** [CN/US]; 4177 S. Barbar Station Way, Boise, Idaho 83716 (US).

(74) Agent: **ALTMAN, Daniel E.**; Knobbe, Martens, Olson & Bear, LLP, 2040 Main Street, 14th Floor, Irvine, California 92614 (US).

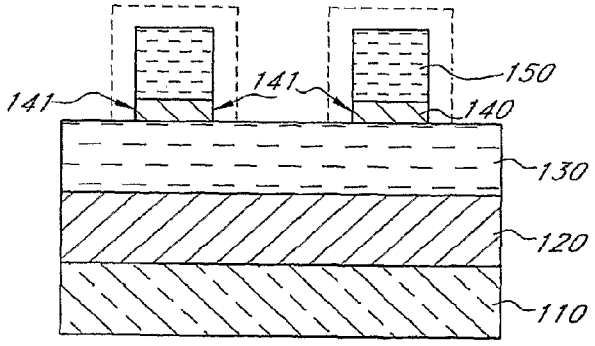
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** TRIM PROCESS FOR CRITICAL DIMENSION CONTROL FOR INTEGRATED CIRCUITS



(57) **Abstract:** Methods of etching substrates employing a trim process for critical dimension control for integrated circuits are disclosed. In one embodiment, the method of etching includes providing a first hard mask layer (130) over a target layer (120); providing a second hard mask layer (140) over the first hard mask layer (130); providing a photoresist layer (150) over the second hard mask layer (140); forming a pattern in the photoresist layer (150); transferring the pattern into the second hard mask layer (140); and trimming the second hard mask layer (140) with the photoresist layer (150) on top of the second hard mask layer (140). The top surface of the second hard mask layer (140) is protected by the photoresist (150) and the target layer (120) is protected by the overlying first hard mask layer (130) during the trim etch, which can therefore be aggressive.

WO 2007/103343 A1