CHARGE RESERVOIR STRUCTURE

Field of the invention

The invention relates to a production process of a semi-conductor on insulator type structure, used to store data within the structure.

Background of the invention

The production of flash memories is based on the use of MOS (Metal Oxide Semiconductor) devices with a floating grid embedded in the grid oxide, between the channel and the grid. The data is stored by trapping electrons in the floating grid, which acts as the memory component.

The principle of memory consists of modifying the current-voltage characteristics of a transistor according to the data stored.

Data storage consists of storing charges in the floating grid or, if applicable, in nodules. These charges induce the shift in the current-voltage curve, as represented by the arrow in figure 1. The data is read by looking at the current level at the reading voltage. In the example in figure 1, in state 0 (corresponding to a discharged grid), no current flows, in state 1 (corresponding to a charged grid), a current can flow.

The main advantage of nodules and other discrete storage devices lies in the fact that if a localised fault of the grid oxide occurs, the leak induced only discharges a single nodule and not the entire floating grid as in the case for continuous grids.

As a matter of fact, for around ten years, new memory devices comprising discrete storage devices and not conventional continuous storage devices in the floating grid have been developed to overcome the problems due to component miniaturisation. In this way, discrete trapping memories can be found with materials such as nitride, so-called "high k" (i.e. high permittivity) materials or semiconductor nano-crystals.

Semiconductor nano-crystal (also referred to as nodules or dots) memories are very promising in terms of size reduction as they offer the advantage of a high integration density, low power consumption and low production cost. In this way, flash memories with silicon or germanium nano-crystals are found. In this respect, it is possible to refer for example to the article by Kan et al., "Nanocrystalline Ge Flash Memories: Electrical Characterization and Trap Engineering", Advanced Materials for Micro and Nanosystems, January 2005.

The principle of these nodule memories is based on an exchange of charges between the nano-crystals and the inversion layer via a thin tunnel dielectric. The charging and discharging of the electrons and therefore of the data is performed on each nodule.

Various techniques are now available to form nano-crystals within substrates, for example aerosol techniques, or by means of PECVD (Plasma Enhanced Chemical Vapour Deposition), or by means of implantation.

Patent application US 2002/0017657 thus describes the formation of nodules by means of implantation and heat treatment. The nano-crystals are formed in the oxide layer which will subsequently be used as a grid oxide for non-volatile memory production.

However, the formation of nodules as described in this document is limited to silicon substrates and cannot be applied to multi-layer substrates, such as SeOI (semiconductor on insulator) type substrates.

In fact, the presence of the semiconductor layer on the substrate surface, above the insulating layer, renders the implantation step difficult. It would in fact be necessary to apply high implantation energies inducing in particular a loss of precision of the implanted region and the creation of damage in the semiconductor film.

In addition, the presence of the semiconductor layer does not enable the application of a heat treatment such as that described in the document. In fact, the heat treatment used is an oxidising treatment and

the oxygen present would not react with the embedded insulator layer but, on the surface, with the semiconductor layer.

Patent application US 2004/0108537 provides for the formation of a structure comprising a base substrate, a charge trapping region and a semiconductor layer wherein electronic components such as transistors may be produced. The trapping region comprises one or more insulator layers, wherein atomic species or nano-crystals forming trapping centres are incorporated. However, this trapping region must have a sufficient thickness for the memory to function correctly. In fact, it is difficult to form a very thin region with a satisfactory homogeneity and a satisfactory quality. However, the thicker the trapping region, the higher the voltages to be applied.

Therefore, one of the aims of the invention is to enable data storage in a semiconductor on insulator (SeOI) type substrate, enabling the use of lower voltages than in the prior art.

Brief description of the invention

A first aim of the invention relates to a production process of a semiconductor on insulator type structure comprising a semiconductor layer of a donor substrate, an insulator layer and a receiver substrate, the process comprising the bonding of the donor substrate on the receiver substrate, at least one of the substrates being coated with an insulator layer, said process comprising the formation at the bonding interface of a so-called trapping interface comprising electrically active traps suitable for retaining charge carriers.

The term "trapping interface" herein refers to the fact that the traps are located at a given depth Z of the structure, between two layers belonging to said structure, as opposed to a "layer" which displays a certain thickness. This term indicates that both layers on either side of the

interface are in direct contact, and are not separated by a continuous surface. As illustrated in figure 2, the Z axis is perpendicular to the surface of the various layers, with its origin at the free surface of the semiconductor layer and oriented in the direction of increasing depths.

According to a first embodiment of the invention, the trapping interface is formed at the interface between the insulator layer coating one of the substrates, and the other substrate.

According to another embodiment of the invention, one of the substrates is coated with a first dielectric layer and the other substrate is coated with a second dielectric layer, such that the insulator layer is obtained by bonding both dielectric layers, the trapping interface being formed at the interface between these two layers.

Particularly advantageously, the thickness of the first dielectric layer, referred to as the "tunnel dielectric" is between 1.5 and 25 nm and the thickness of the second dielectric layer, referred to as the "control dielectric", is between 4 and 50 nm.

According to other characteristics of the invention, taken alone or in combination:

- the process comprises, before bonding, the formation of electrically active defects on the surface of at least one of the layers located on the interface;

- the formation of said defects is obtained by means of a plasma treatment, said plasma treatment being preferentially applied on the control dielectric layer; the plasma comprising oxygen, argon, nitrogen, chlorine or fluorine.

- according to one alternative embodiment of the invention, said defects are obtained by means of a treatment suitable for depositing contaminants on the surface of at least one of the layers located on the interface;

- the treatment is a heat treatment in an environment containing said contaminants; the contaminants are advantageously germanium atoms;

- said treatment is a spin coating of a solution containing said contaminants; the contaminants are germanium, dopants selected from column III, IV or V elements, ions selected from K^+, Na^+, F^-, Cl^- or metals selected from iron and aluminium;

- the bonding is bonding by means of molecular adhesion;

- before bonding, at least one of the layers located at the interface is activated by means of plasma;

- the process comprises, before the bonding, the formation of an embrittlement zone in the donor substrate so as to define a semiconductor layer and, after the bonding, a detachment along the embrittlement zone so as to transfer the semiconductor layer to the receiver substrate;

- the receiver substrate is coated with the control dielectric layer and before the bonding, dopants displaying a density greater than 10^{17} cm^{-3} are implanted in the receiver substrate, under said layer, so as to form a conductive doped layer under the control dielectric layer.

Another aim of the invention relates to a semiconductor on insulator type structure comprising a semiconductor layer of a donor substrate, an insulator layer and a receiver substrate, said structure comprising a so-called trapping interface located in the insulator layer or at the interface between the insulator layer and one of the substrates, the trapping interface comprising electrically active traps suitable for retaining charge carriers.

Particularly advantageously, the insulator layer comprises a first dielectric layer and a second dielectric layer, the trapping interface being located at the interface between the two dielectric layers.

Preferentially, the thickness of the first dielectric layer, referred to as the "tunnel dielectric" is between 1.5 and 25 nm and the thickness of the

second dielectric layer, referred to as the "control dielectric", is between 4 and 50 nm.

According to one particular embodiment, the receiver substrate is coated with the control dielectric layer, said substrate being a composite substrate comprising a base substrate, an oxide layer and a conductive or semiconductor layer located under the control dielectric layer.

The first and second dielectric layers are preferentially in materials selected from SiO_2, $SiO_{2-x}N_x$ ($0 < x \leq 1$), high k type dielectrics such as hafnium dioxide or yttrium oxide, strontium and titanium dioxide, alumina, zirconium dioxide, tantalum pentoxide, titanium dioxide, the nitrides and silicides thereof.

The trapping interface advantageously comprises contaminants selected from nitrogen, germanium, dopants selected from column III, IV or V elements, ions selected from K^+, Na^+, F^-, Cl^- or metals selected from iron and aluminium, the contaminant concentration being between 10^{13} and 10^{15} atoms/cm^2.

Brief description of figures

Other characteristics, aims and advantages of the invention will emerge from the detailed description hereinafter, with reference to the annotated figures wherein:

- figure 1 illustrates the current-voltage curves according to the charged or discharged state of the grid,

- figure 2A illustrates an SeOI type structure according to the invention,

- figure 2B illustrates an alternative embodiment of this structure,

- figures 3A to 3E represent the steps of the process according to a first embodiment of the invention,

- figures 4A to 4E represent the steps of the process according to a second embodiment of the invention

- figure 5 illustrates a substrate according to a specific embodiment of the invention.

Detailed description of the invention

As a general rule, the invention makes it possible to produce an SeOI type structure comprising two substrates and an embedded insulator layer, wherein a so-called trapping interface contains electrically active traps suitable for retaining charge carriers. This trapping interface is located either inside the insulator layer (as represented in figure 2A which will be described in detail below), or at the interface between one of the substrates and the insulator layer (as represented in figure 2B).

The traps are obtained by trapping, during bonding, electrically active defects present on the interface.

These defects are preferentially obtained by contamination of the surface of one of the two substrates before bonding.

Contamination consists of concentrating the impurities or contaminants on the surface of one of the substrates, which will form traps after placing the substrates in contact.

The term contaminant refers to any extraneous elements to the layer whereon they are located. Within the scope of the invention, the contaminants are electrically active or display hanging bonds or generate hanging bonds locally in the dielectric, such that the traps are suitable for capturing and retaining charge carriers. The term "charge carriers" refers either to electrons or holes.

In the case of memory applications, trapping is performed on an insulator layer.

Trapping consists generally of localising a charge at a given point of the structure so that it can no longer move physically and, consequently, it can no longer take part in conduction. The charge may be released by means of an energy supply. The charge reaches the trap by means of a

direct tunnel effect, indirect tunnel effect or, if applicable, by means of hot carriers and it is released by means of a direct or indirect tunnel effect.

The use of the invention to produce an SeOI type, more specifically an UTBOX (Ultra Thin Buried Oxide) type structure, wherein the embedded insulator comprises a trapping interface containing electrically active traps.

Such a structure is represented in figure 2A. It comprises a receiver substrate 20, an insulator layer 60 formed from two dielectric layers 40 and 50 and a thin layer 11 from a donor substrate, the trapping interface 30 being located inside the layer 60, at the interface between the two dielectric layers 40 and 50.

For memory applications, it is in fact preferred to form structures with thin embedded dielectric layers of 5 to 50 nm in order to favour the tunnel effect with reasonable voltages.

The traps are electrically active defects present on the bonding interface and act as nodules generally present in non-volatile memories.

As a general rule, the proposed process comprises the following steps:

- formation of a so-called "tunnel" dielectric on one of the two substrates
- formation of a so-called "control" dielectric on the other substrate
- treatment of the surface of at least one of the two dielectrics in order to create electrically active defects forming traps or charge reservoirs after bonding
- placing contact of the two substrates via the tunnel dielectric and control dielectric, for bonding by means of molecular adhesion.

The term dielectric refers to a material wherein the electrical conductivity is practically null. The term "tunnel dielectric" refers to a very thin dielectric; the so-called "control" dielectric being thicker. The ratio of the dielectric thicknesses must be sufficient so that it is possible to have charges pass through the tunnel dielectric by applying a voltage at the

structure terminals, without said charges being able to pass through the control dielectric. To this end, it is possible either to use a sufficiently thin tunnel dielectric, i.e. of the order of 2 nm, so that it is possible for it to be passed through by means a direct tunnel effect, or use a thicker dielectric and a higher voltage so that the charges pass via an indirect tunnel effect (or Folder-Nordheim effect). In the latter case, the control dielectric should be substantially thicker than the tunnel dielectric - typically, the difference in thickness will be the order of a factor of 3 or more.

The substrates may consist of any type of semiconductor material such as silicon, germanium, III-V (GaAs, InP, etc.) compounds or alloys of these materials.

Both substrates may be of different types.

Either of the substrates may also be a composite structure such as an SeOI: in this case, it consists at least partially of conductive and/or insulating materials.

As a general rule, the layer of the structure in contact with the tunnel dielectric will preferentially be a semiconductor.

Similarly, the layer of the structure in contact with the control dielectric will preferentially be a semiconductor or a conductor (metal or very highly doped semiconductor). In this way, it is possible to implant a high dopant dose under the control dielectric layer. In this respect, it is possible to refer to example 3 described below, and to figure 5.

The various steps of the process will now be described.

Tunnel dielectric formation

The tunnel dielectric material is selected from the following materials: SiO_2, $SiO_{2-x}N_x$ ($0 < x \leq 1$), high k type dielectrics such as hafnium dioxide (HfO_2) or yttrium oxide, strontium and titanium dioxide,

alumina, zirconium dioxide, tantalum pentoxide, titanium dioxide, the nitrides and silicides thereof.

As a general rule, any technique known to those skilled in the art to obtain a dielectric of an equivalent quality to that of a CMOS component grid dielectric may be used. The expected quality is the thickness of a grid oxide of similar thickness for transistors dedicated to logical applications. Roadmaps issued by ITRS ("International Technology Roadmap for Semiconductors") well-known to those skilled in the art are available, used to define the desired physical and electrical characteristics, which will be directly dependent on the thickness of the layer.

It is also necessary to note that the dielectric layers used (tunnel or control) may be "composite" structures obtained from the reaction between two different types of layers. For example, if it is desired to deposit a layer of HfO_2 on Si, it is not deposited directly on a silicon surface but on an SiO_y ($1 < y \leq 2$) type oxidised surface to subsequently deposit the HfO_2. In addition, irrespective of the type of layers present, the subsequent treatments applied to their structure may generate an interface which will no longer be clear but rather a gradient between the species present.

In this way, for the dielectrics deposited, any interface passivation technique, well-known to those skilled in the art, may be used.

In particular, it may be envisaged to use dry thermal oxidation, CVD (Chemical Vapour Deposition) or ALD (Atomic Layer Deposition), or a combination of these techniques or heat treatments intended to make several layers interact.

The thickness of the dielectric formed in this way is between 1.5 and 25 nm.

Control dielectric formation

The control dielectric material is selected from the following materials: SiO_2, $SiO_{2-x}N_x$ ($0 < x \leq 1$), high k type dielectrics such as hafnium dioxide or yttrium oxide, strontium and titanium dioxide, alumina,

zirconium dioxide, tantalum pentoxide, titanium dioxide, the nitrides and silicides thereof.

It is possible to use a thermal oxidation which makes it possible for example, if the substrate is made of silicon, to form a silicon oxide layer. The deposition techniques mentioned above (CVD, ALD) may also be envisaged, along with wet thermal oxidation.

The thickness of the control dielectric is between 4 and 50 nm.

According to an alternative embodiment of the invention, illustrated in figure 2B, it is possible to only form an insulating layer 60 on the surface of one of the substrates (typically, the donor substrate from which the thin layer 11 is obtained) so as to form the trapping interface 30 at the interface between the insulator layer 60 and the receiver substrate 20 whereon the insulator layer 60 is bonded. In this case, it is no longer necessary to make a distinction between the "tunnel" and "control" dielectric. The following steps are applicable in this case. The treatment process is then applied onto the surface of the receiver substrate 20 and/or on the surface of the insulator layer 60. In this case, the treatment is preferentially performed on the surface of the insulating layer.

Defect formation

As a general rule, electrically active defects are generated, for example atoms capable of capturing, and to a certain extent retaining, charge carriers (electrons or holes).

Various processes may be used to form this type of defect on the surface of either of the dielectrics.

According to a first technique, surface defects are formed by applying a plasma preferentially on the control dielectric.

Plasma makes is possible to incorporate atomic species in the material to which it is applied. Incorporation is performed as in the case of

a low-energy implantation with, if applicable, an additional chemical reaction between the plasma constituents and the material.

As the material is subject to ionic bombardment, its structure may be damaged or modified on a very low thickness (generally 3 to 6 nm under the conditions described herein). The defects generated may generally be subsequently restored by applying a heat treatment at a sufficient temperature. This heat treatment may lead to the diffusion of the incorporated atomic species and transform the very low thickness of damaged or modified material into an interface of defects.

The plasma treatment is preferentially applied to the control dielectric as, if it is applied to a very thin tunnel dielectric, the plasma treatment is liable to modify the thickness thereof, which is to be avoided so as not to affect the characteristics thereof.

Various types of plasma may be used for this purpose, such as oxygen, argon, nitrogen plasma or even with chlorine, fluorine. The plasma power, pressure and exposure time will be adapted according to the desired defect size but also according to the type of plasma used.

However, plasma may only be used as a defect creation technique in some cases. In fact, if, at the end of the production process, all the effects of the plasma have been eliminated, this indicates that it did not create any defects. Typically, activation with O_2 or Ar plasma of an SiO_2 or Si layer, followed by annealing (possibly bonding reinforcement annealing) at a temperature of 950°C, will not leave any electrical active defects in the insulator layer.

The most effective defect generation will be obtained with plasmas containing elements wherein the presence generates defects and which are subject to low diffusion in the dielectric, such as nitrogen.

In this way, a nitrogen plasma converts the surface of an oxide into a oxynitride surface layer which is electrically active. After thermal treatment, this surface layer may be considered as an interface or a surface of defects.

Another means to generate defects is to contaminate the surface of the treated layer. In this way, a heat treatment conducted in a furnace containing a specific level of contaminants generates surface defects.

Another technique consists of contaminating the dielectric surface by means of a spin coating process. The principle of this process is to spread a small quantity of contaminants on a substrate using centrifugal forces. The selected contaminants are elements that can be placed in solution, for example germanium or dopants, but also ions or metals. The dopants include the usual semiconductor dopants, i.e. B, As, P, Sb, In, Ga and, as a general rule, column III, IV and V elements of the periodic table. The ions may be selected from K^+, Na^+, F^- or Cl^-. The metals will be selected from aluminium and iron. Elements liable to segregate at the bonding interface or which have a low diffusion coefficient in the dielectric will preferentially be selected.

In both cases (surface contamination or spin coating), it is possible to achieve a thickness of contamination that corresponds to a fraction of atomic monolayer, i.e. some atomic species are disposed over the surface without forming a continuous layer over that surface.

The spin coating may comprise the following successive steps:

- deposition of contaminant in solution on the dielectric,
- distribution of the contaminant on the entire surface of the dielectric by means of rotation,
- increase in the rotation speed in order to eliminate the excess contaminant,
- rotation at constant speed in order to establish the contaminant thickness
- rotation for a specified time to enable the evaporation of the solvent.

Surface activation before bonding

As the dielectric layers are very thin, the surfaces are preferentially activated before the placing in contact thereof. Particularly advantageously, plasma activation will be used. In fact, thin dielectrics are applicable in this case and it is necessary to retain low heat treatments to prevent the diffusion of any contaminants. As a result, even if plasma is not used to create defects, it may be used to facilitate bonding. Therefore, it is possible to combine plasma activation with any of the contamination techniques described above.

Any plasma enabling bonding, such as an oxygen, nitrogen, argon, helium plasma or a combination thereof, may be used for this purpose. In the case of a direct tunnel, the control dielectric is preferentially activated, so as not to modify the thickness of the tunnel dielectric. In the case of the indirect or Fowler-Nordheim tunnel, where the dielectrics are thicker, it is possible to activate one or both of the dielectrics.

Wafer bonding and carrier trap creation

The substrates are placed in contact with a view to bonding by means of molecular adhesion. To this end, surface preparation is performed prior to bonding: in this way, suitable cleaning, brushing and rinsing operations are applied in order to obtain a satisfactory substrate surface condition.

By placing both substrates in contact along an interface comprising electrically active defects, said defects are enclosed between the two substrates, which forms a trapping interface containing electrically active traps.

Only a portion of the contaminants may form traps, but depending on the kind of contaminant, it is possible that an atom of contaminant generates more than one trap.

The density of traps thus formed at the interface is comprised between 10^{12} and 10^{15} cm^{-2}.

The presence of defects on the bonding interface makes it possible to trap or release these charge carriers, thus creating a memory effect. In fact, isolated defects may create a unique state in the insulator forbidden band. Physically, this state may be due to a hanging bond or to an atom which would benefit considerably, in terms of energy, from retrieving an additional electron (electron trap) or, on the other hand, supplying an electron (hole trap).

The fact that the traps are located at the bonding interface and not in a layer of a certain thickness makes it possible to use lower voltages than in the prior art.

Furthermore, when the traps are located at an interface between two dielectric layers, the application of a voltage is required in order to charge or discharge them.

These traps are then said "slow" as compared to traps located at an interface between a dielectric layer and a semiconductor material. In the latter case, the "fast" traps charge and discharge during the normal use of the device and are usually not able to retain a charge during a time long enough to fulfil a memory function.

Another advantage of forming a trapping interface between two dielectric layers instead of a charge trapping layer as in prior art, is that the traps are all located at the same depth of the structure. Hence, when a device is formed based on this structure, the traps are all located at the same distance from a channel layer or a control electrode, which allows a better control of the traps by the grid. This results on a lower variability of the required voltages, and on a more abrupt transition between charged and discharged states.

Optionally, an additional heat treatment is used to reinforce the bonding interface.

Semiconductor layer detachment

If one of the two substrates (referred to as the donor substrate) has been previously implanted with a view to transferring a thin layer to the other substrate, a heat treatment is applied which enables this transfer. If the donor substrate comprises a porous zone, the application of mechanical forces enables the detachment and transfer to the other substrate.

Finally, optionally, a finishing treatment may be applied in order to smooth the semiconductor layer transferred in this way.

Several examples of embodiments of the invention will now be described. The examples explained below are restricted to SeOI type structures obtained by means of Smart Cut™ technology; however, it goes without saying that any other process using molecular bonding can be envisaged.

Example 1 – Single SOI – Contamination by means of heat treatment

With reference to figure 3A, on the surface of a donor substrate 10 a 2 nm thick tunnel dielectric layer 40 is formed, and an implantation via the layer 40 is performed to form an embrittlement zone in the donor substrate 10, so as to define a thin layer 11.

With reference to figure 3B, a base substrate (or receiver substrate) 20 comprising on the surface thereof an SiO_2 control dielectric layer 50 of the order of 5 nm, in a furnace generally used for wafers comprising germanium. Therefore, the furnace is contaminated by germanium atoms.

With reference to figure 3C, the base substrate 20 is subjected to a heat treatment of the order of 600°C, for approximately 1 hour, in argon. The concentration of contaminants 31 on the control dielectric surface 50 is of the order of 10^{13} to 10^{14} cm^{-2}.

The surface of the control dielectric 50 is then activated by means of a plasma treatment in argon, applied with a 150 W power and a 150 mTorr pressure for 20 seconds.

With reference to figure 3D, the donor substrate 10 is bonded on the base substrate 20 via dielectric layers 40 and 50, which makes it possible to form, at the bonding interface, a trapping interface 30. All the dielectric layers 40 and 50 form the embedded insulator layer 60 of the SeOI structure.

With reference to figure 3E, the thin layer 11 is detached from the donor substrate 10 by means of the application of a heat treatment of the order of 500°C. Stabilisation annealing then makes it possible to reinforce the bonding interface.

Finally, optionally, a finishing treatment may be applied in order to smooth the thin layer 11 transferred in this way.

Example 2 – Double SOI – Contamination by means of spin coating

With reference to figure 4A, a donor substrate 10 is implanted so as to create an embrittlement zone defining a thin layer 11. A 7 nm thick control dielectric layer 50 is formed on the surface thereon.

An O_2 plasma treatment at 250 W, 150 mTorr is performed on the control dielectric for 15 seconds.

Moreover, with reference to figure 4B, an SeOI type base substrate 20 is formed, comprising a substrate 23, a 145 nm thick embedded oxide layer 22 and a thin semiconductor layer 21. On this substrate, a tunnel dielectric 40 is formed.

With reference to figure 4C, the surface of the tunnel dielectric 40 is contaminated by means of spin coating.

To enable the deposition of germanium contaminants, of a concentration of the order of 10^{15} atoms/cm^2 by means of spin coating, it is necessary to use germanium in a 0.01 mol/l acidified aqueous solution (i.e. approximately 0.7 g/l of germanium contaminants), the solution containing almost 1% nitric acid. The rotation speed is of the order of 3500 rpm. In this respect, it is possible to refer to the article by R. Hölzl et al, Journal of The Electrochemical Society, 146 (6), 2245-2253 (1999).

With reference to figure 4D, the substrate 10 is bonded on the substrate 20.

The remainder of the process is not different to that of the previous example.

Example 3 – Single SOI – Plasma contamination

This alternative embodiment may be described with reference to figures 3A to 3E.

With reference to figure 3A, a donor substrate 10 comprising a tunnel dielectric layer 40 is implanted so as to define a thin layer. The tunnel dielectric thickness is 5 nm.

With reference to figures 3B and 3C, a second substrate 20, or receiver substrate, made of silicon, comprises a control dielectric layer 50 made of SiO_2, formed by oxidising the substrate and displaying a thickness of the order of 20 nm.

Optionally, with reference to figure 5, dopants are implanted in the receiver substrate 20, under the layer 50. The dopant density to be achieved under the layer 50 is greater than 10^{17} cm^{-3}, over a thickness of at least a few nanometres. This doped layer 24 under the control dielectric 50 is thus conductive.

To this substrate 20, a plasma treatment is applied, which is intended, firstly, to create defects represented by the reference 31, and, secondly, to activate the surface to be bonded. To this end, a nitrogen plasma is used with a 250 W output, at a pressure of 50 mTorr, for 20 seconds.

With reference to figure 3D, the first and the second substrate are bonded such that the defects 31 are located at the interface, so as to form the trapping interface 30.

The remainder of the process is similar to that of example 1.

The applications of such structures comprising a trapping interface include:

Application No. 1: adjustable voltage devices and/or circuits for low-consumption applications.

The transistors or circuits are in principle manufactured in the SeOI thin semiconductor layer. The design of the components makes it possible to charge and discharge the traps present in the dielectric by means of a specially provided operation, such as for example a high polarisation of the substrate or an electrode located under the BOX and the grounding of the source and the drain of the transistors.

When the BOX is charged, the transistor threshold voltage is increased, the current level of a given operating voltage is reduced (in particular, the leak current in static mode, generally referenced I_{off}).

This operation is not very fast but is particularly suitable in devices which have a stand-by function, particularly typically all mobile applications.

Application No. 2: Double-grid flash memories

In order to reduce the size of "flash" type memories, double-grid memories are manufactured. In this way, the effective surface area of the memory is doubled without increasing its effective surface area on the silicon, which increases the integration density. By operating in double grid mode, the control of the grid on the current is also reinforced. On Therefore, improved control of the threshold voltage of the device is obtained by means of the memory effect, which provides higher-performance memories.

Claims

1. Production process of a semiconductor on insulator type structure comprising, in combination, the steps of:

forming a donor substrate having a semiconductor layer;

forming a receiver substrate;

coating at least one of the donor substrate and the receiver substrate with a first dielectric layer;

forming an insulator layer comprising the first dielectric layer, a second dielectric layer, and a trapping interface between the two dielectric layers comprising electrically active traps suitable for retaining charge carriers;

bonding the substrates together; and

forming electrically active defects at the trapping interface by means of plasma treatment, or depositing contaminants at the trapping interface by spin coating a solution of contaminants. .

2. Process according to claim 1, wherein the step of coating further comprises coating the other substrate with the second dielectric layer.

3. Process according to claim 2, wherein the first dielectric layer is a tunnel dielectric layer having a thickness between 1.5 and 25 nm, and the second dielectric layer is a control dielectric layer having a thickness between 4 and 50 nm.

4. Process according to claim 1 wherein before bonding, electrically active defects are formed on a surface of at least one of the dielectric layers.

5. Process according to claim 1, wherein defects are formed by plasma treatment.

6. Process according to claim 3, wherein the plasma treatment is applied on the control dielectric layer.

7. Process according to 1 to 6, wherein the plasma treatment comprises oxygen, argon, nitrogen, chlorine or fluorine.

8. Process according to claim 1, wherein the defects are obtained by depositing contaminants on the surface of at least one of the dielectric layers.

9. Process according to claim 8, wherein the contaminants are germanium atoms.

10. Process according to claim 9, wherein the contaminants are germanium, dopants selected from column III, IV or V elements, ions selected from K^+, Na^+, F^-, Cl^- or metals selected from iron and aluminium.

11. Process according to any of claims 1 to 10, wherein the bonding is bonding by molecular adhesion.

12. Process according to claim 11, wherein, before bonding, at least one of the layers of the interface is activated by means of plasma.

13. Process according to any of claims 1 to 12, wherein

before the bonding, forming of an embrittlement zone in the donor substrate so as to define the semiconductor layer and,

after bonding, detaching the semiconductor layer along the embrittlement zone so as to transfer the semiconductor layer to the receiver substrate.

14. Process according to claim 3, wherein the receiver substrate (20) is coated with the control dielectric layer and before the bonding, dopants displaying a density greater than 10^{17} cm^3 are implanted in the receiver substrate, under the control dielectric layer, so as to form a conductive doped layer under the control dielectric layer.