

FIG. 1

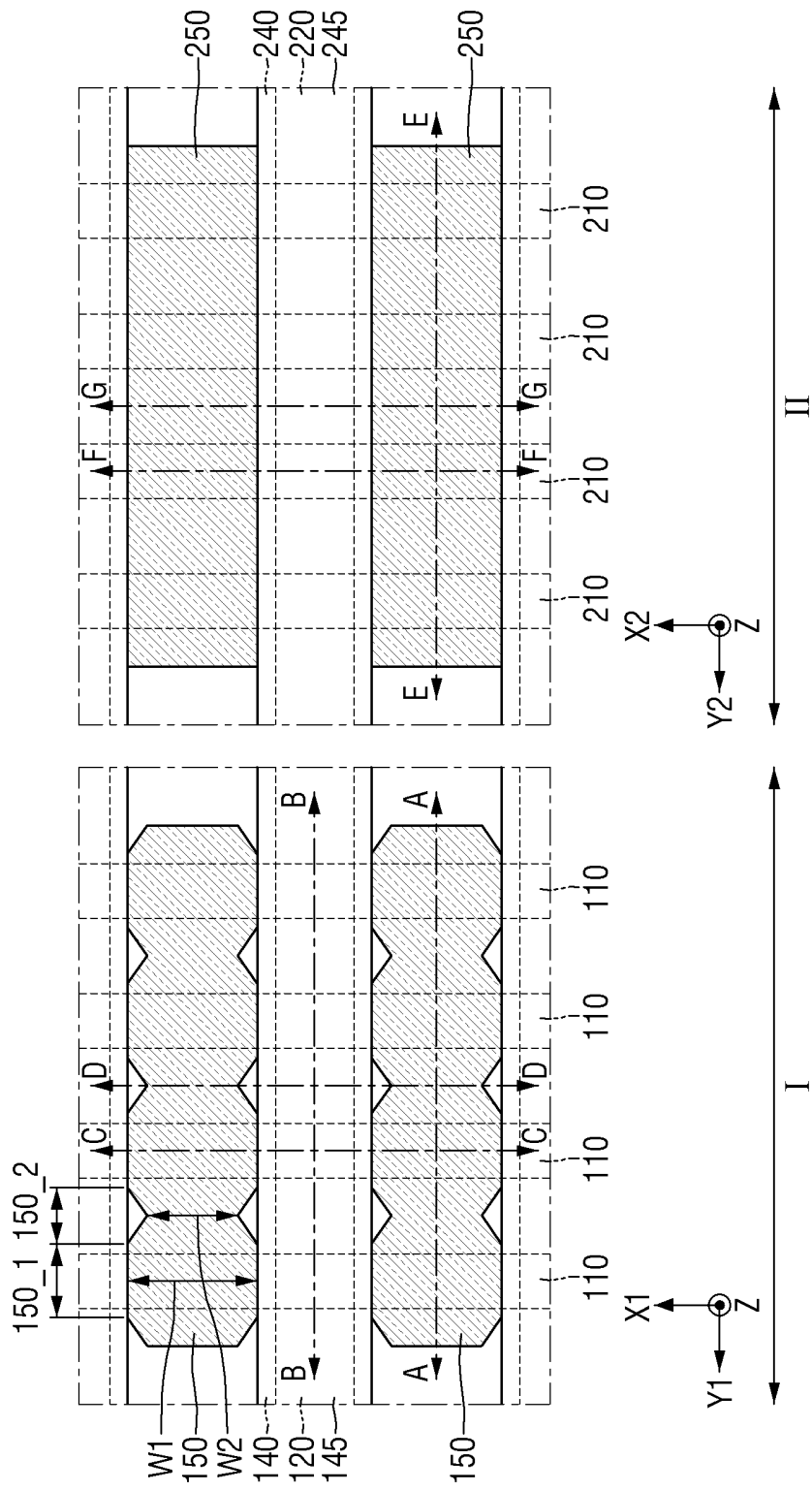


FIG. 2

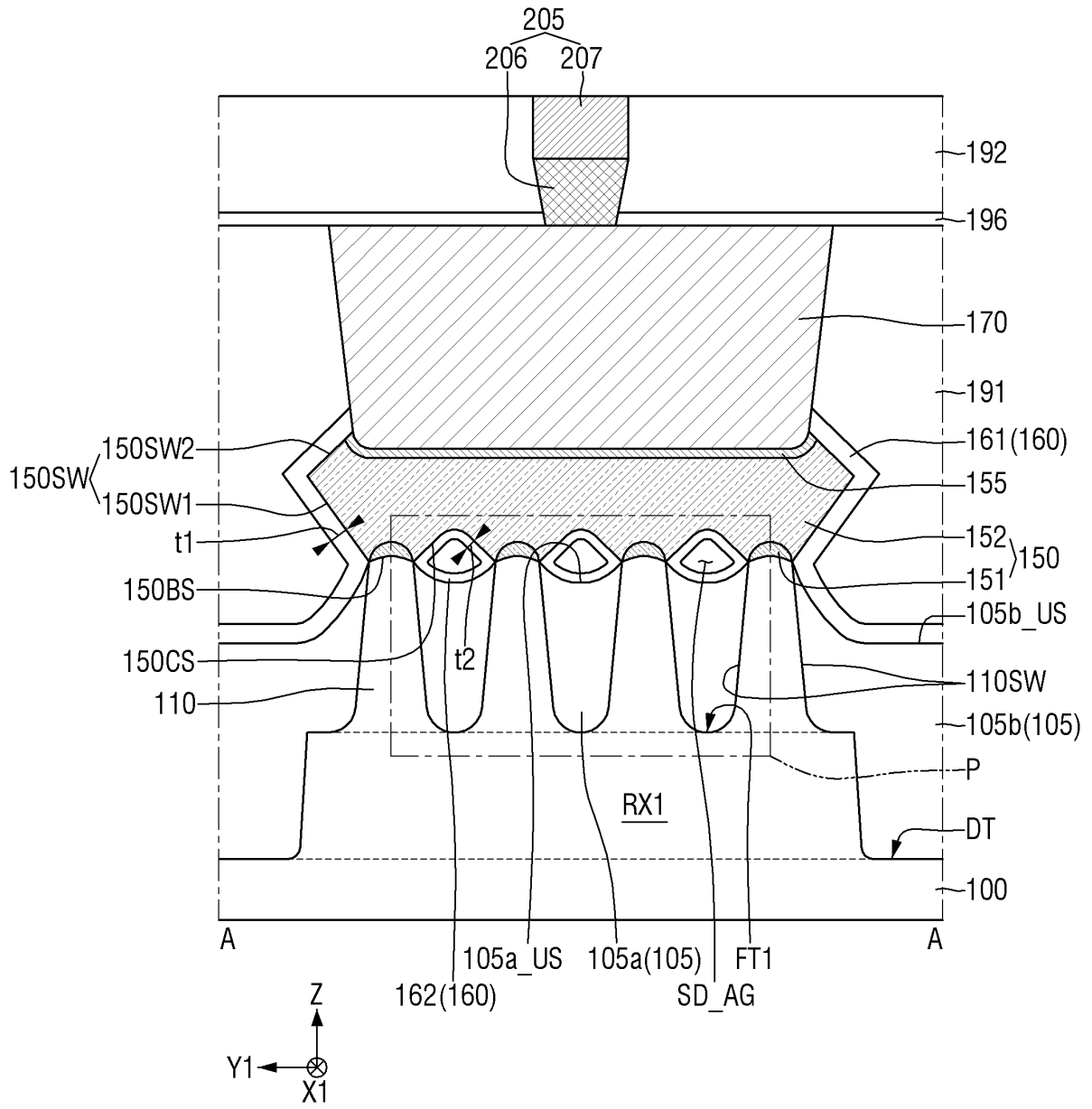


FIG. 3

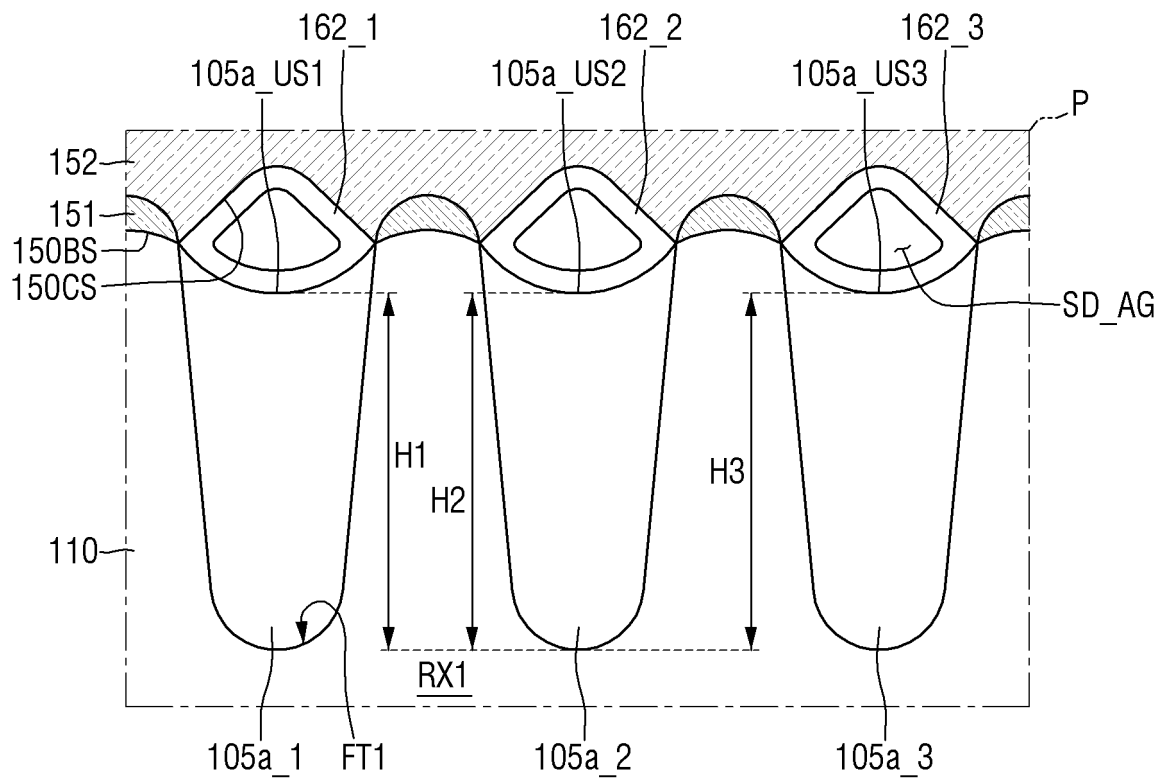


FIG. 4

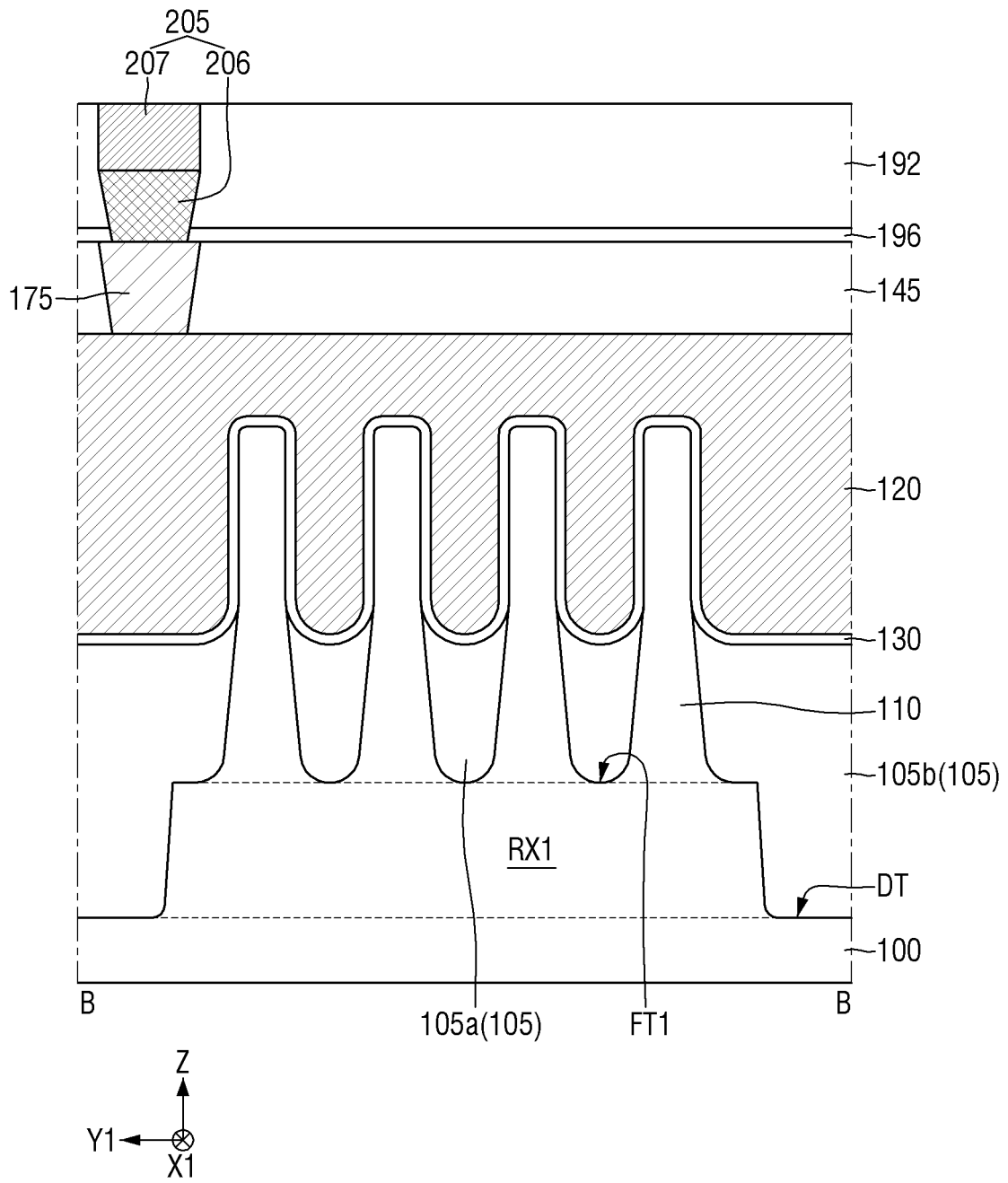


FIG. 5

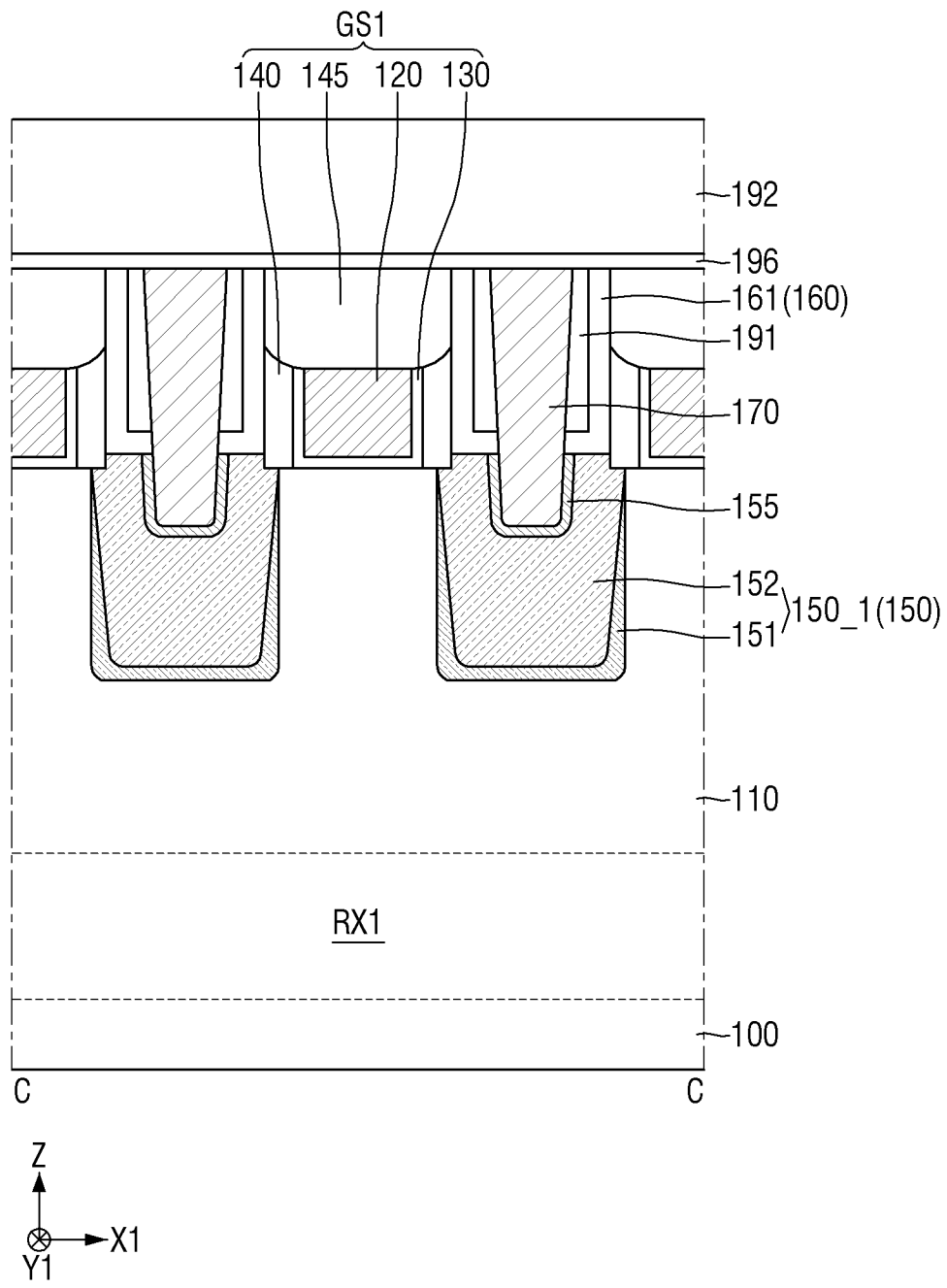


FIG. 6

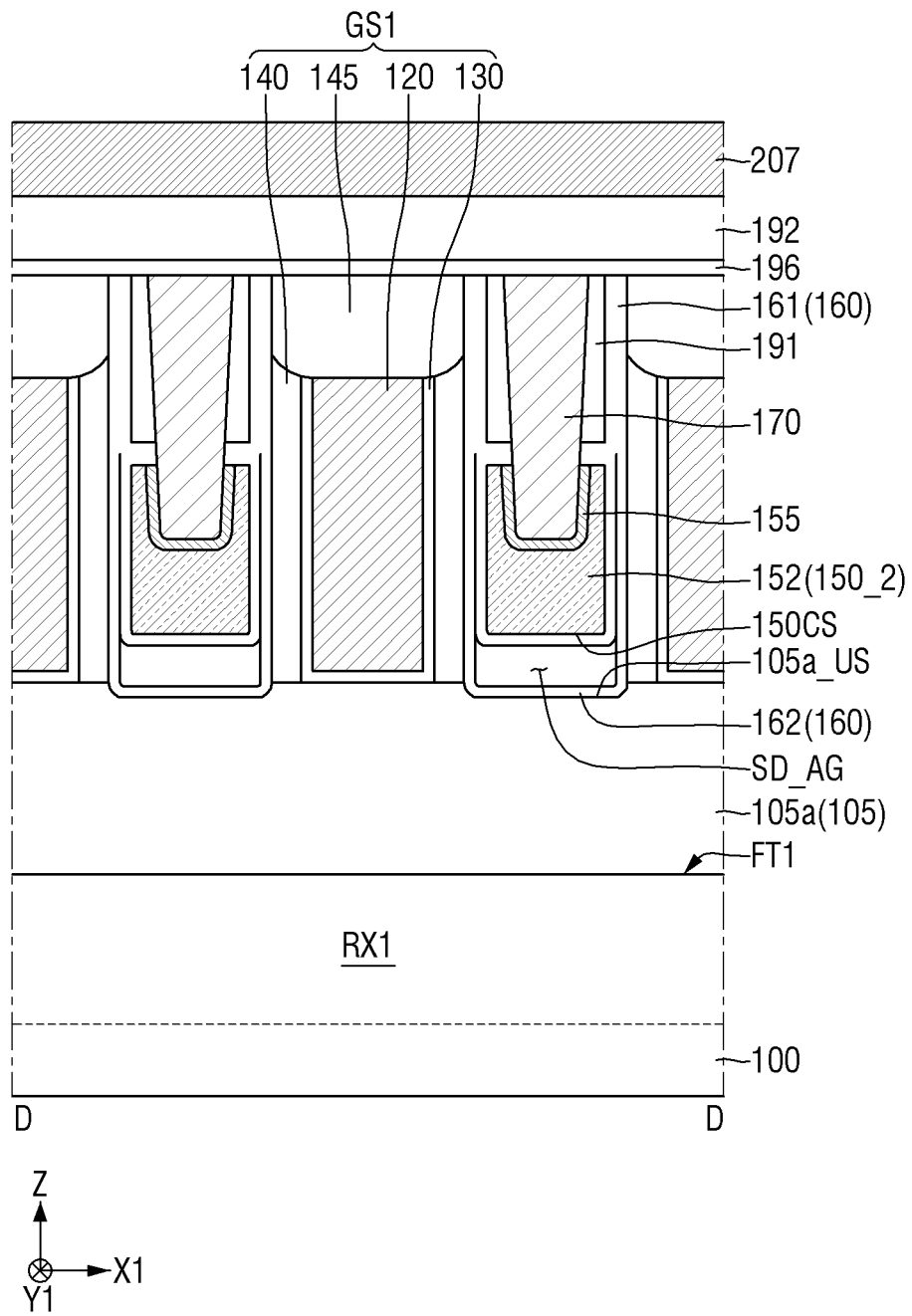


FIG. 7

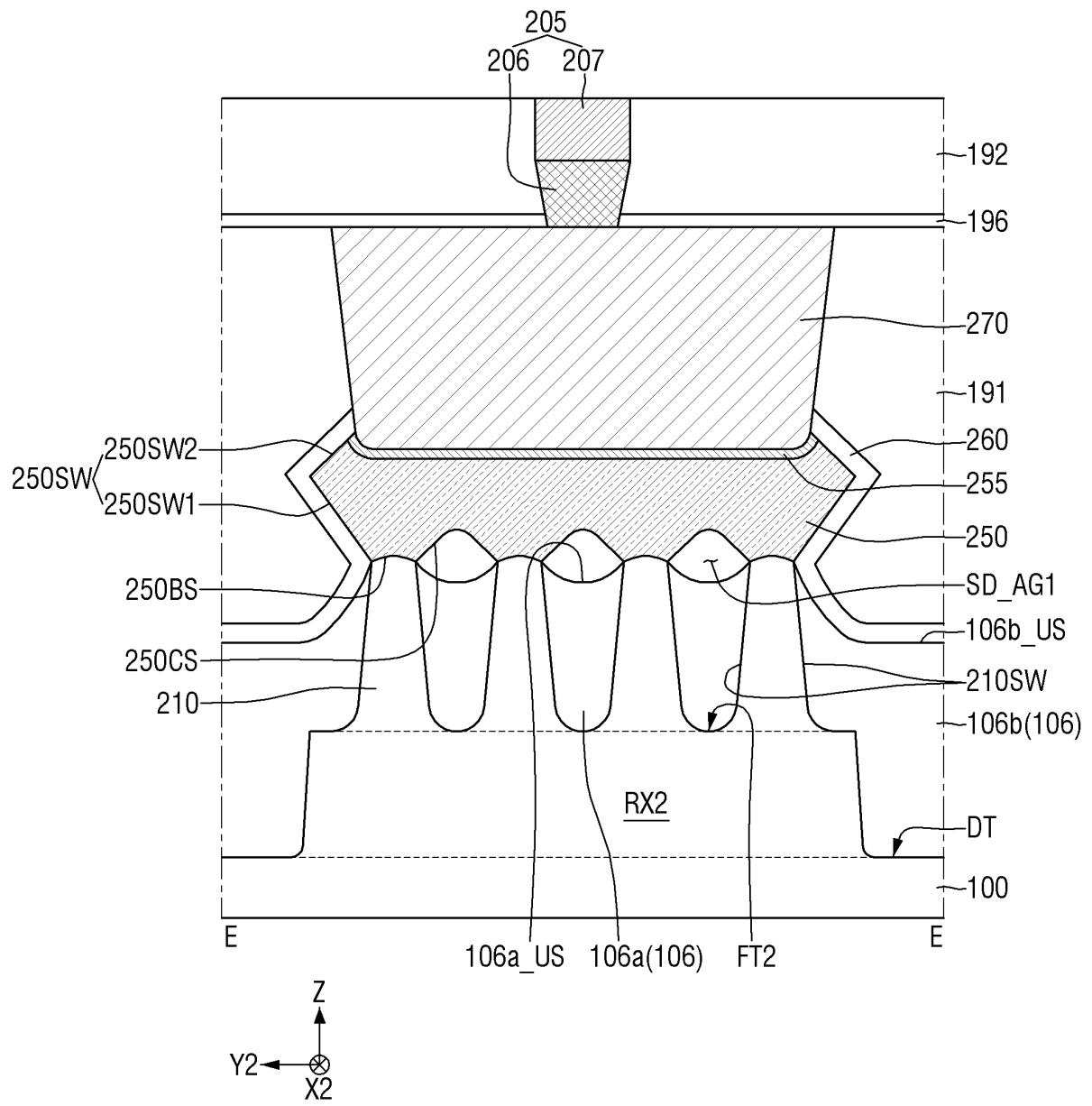


Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100 with a top layer 192 and a bottom layer 196. A central region 220 is surrounded by a gate stack 240, 245, 230, and 230. A gate electrode 260 is positioned above the gate stack. A gate insulating layer 191 is located between the gate electrode 260 and the gate stack. A gate contact 270 is formed on the gate stack. A gate contact 255 is formed on the gate stack. A gate contact 250 is formed on the gate stack. A gate contact 210 is formed on the gate stack. A gate contact 100 is formed on the gate stack. A coordinate system is shown at the bottom left with Z, X1, and Y1 axes.

FIG. 9

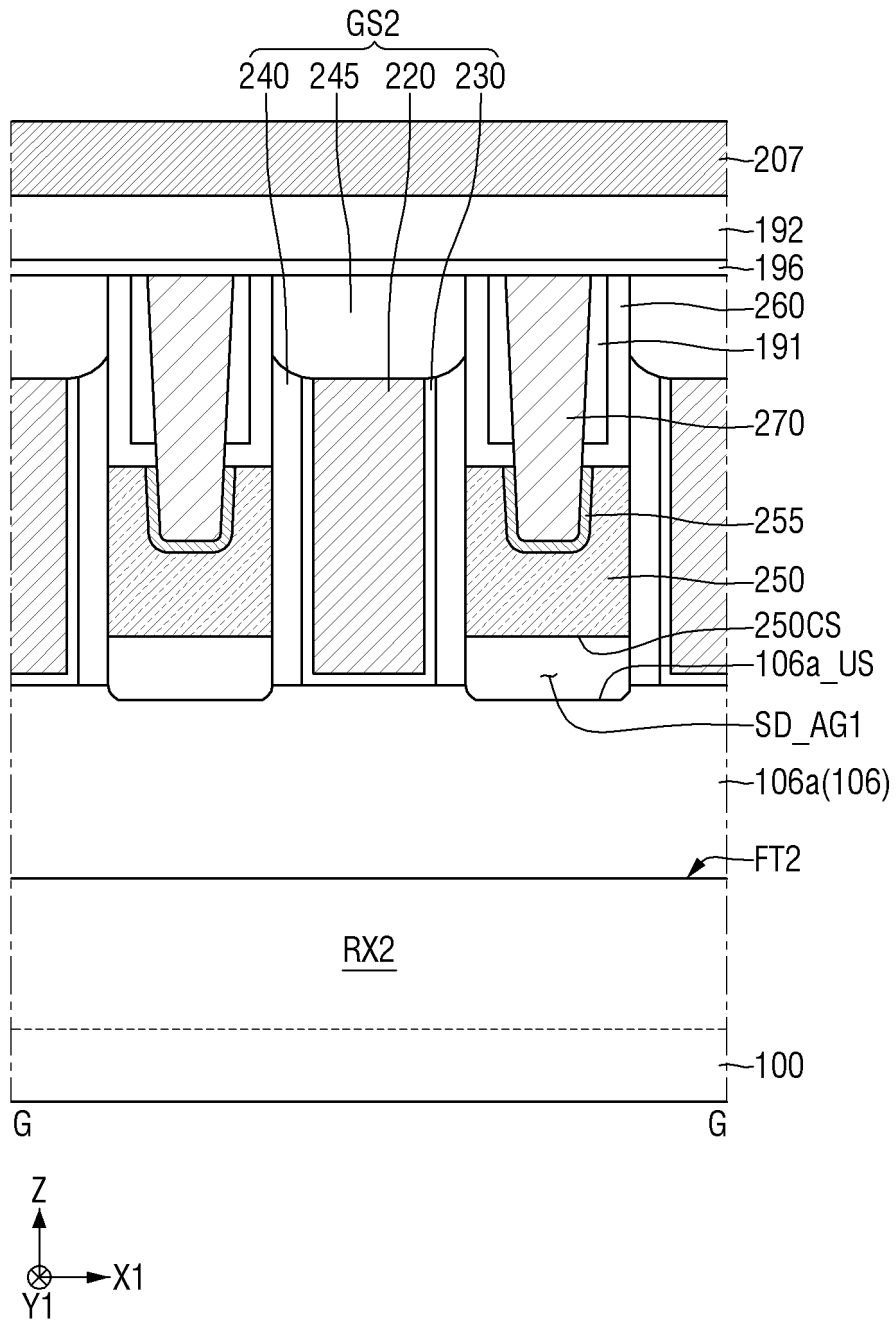


FIG. 10

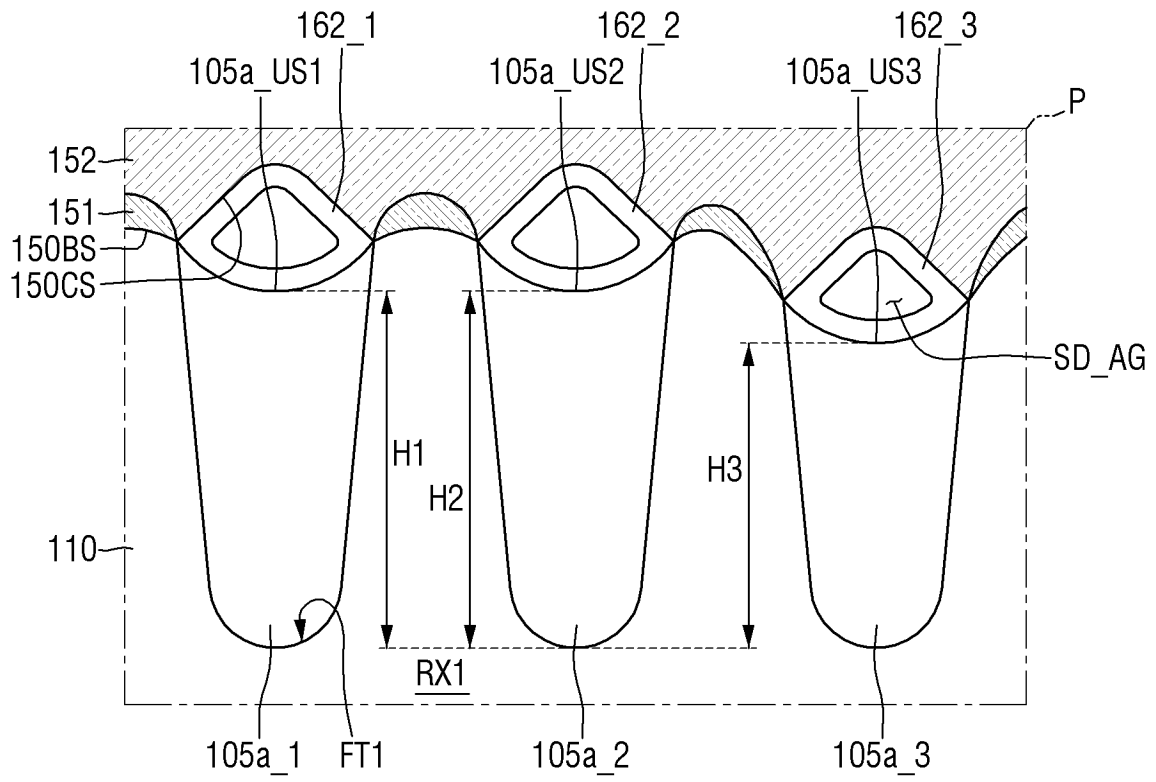


FIG. 11

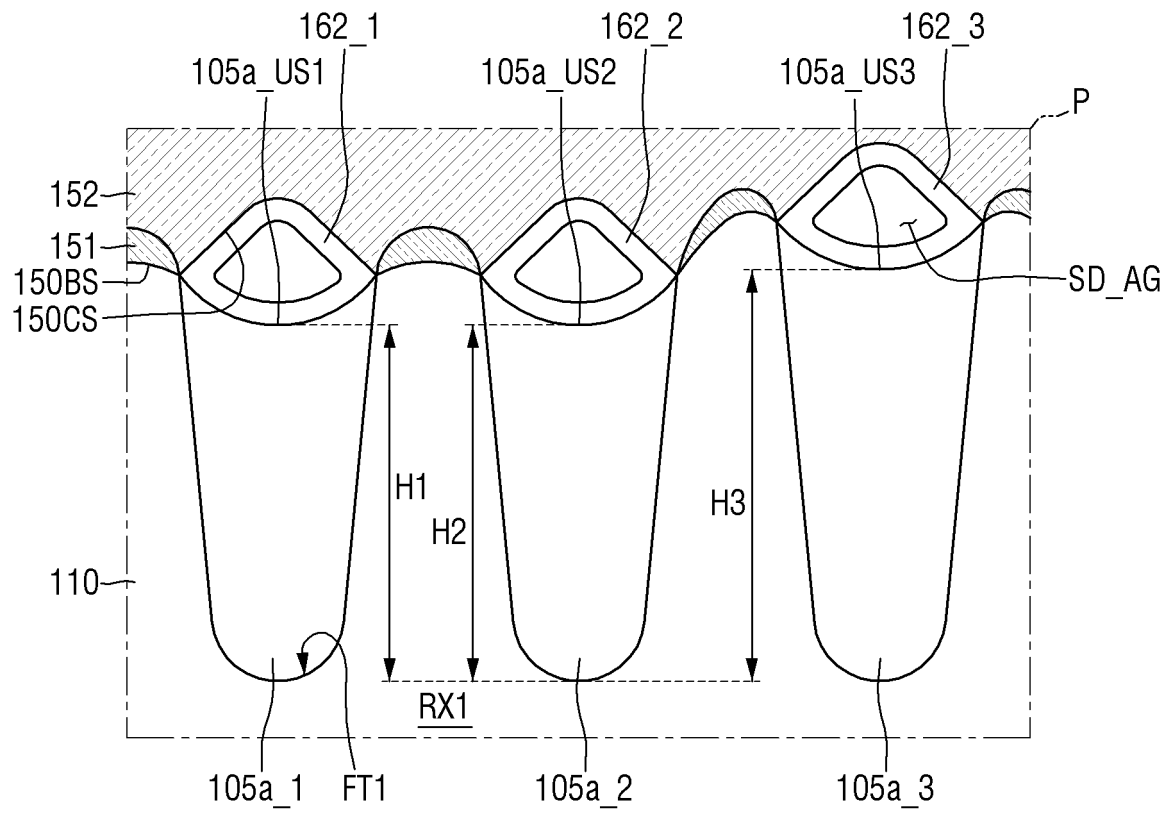


FIG. 12

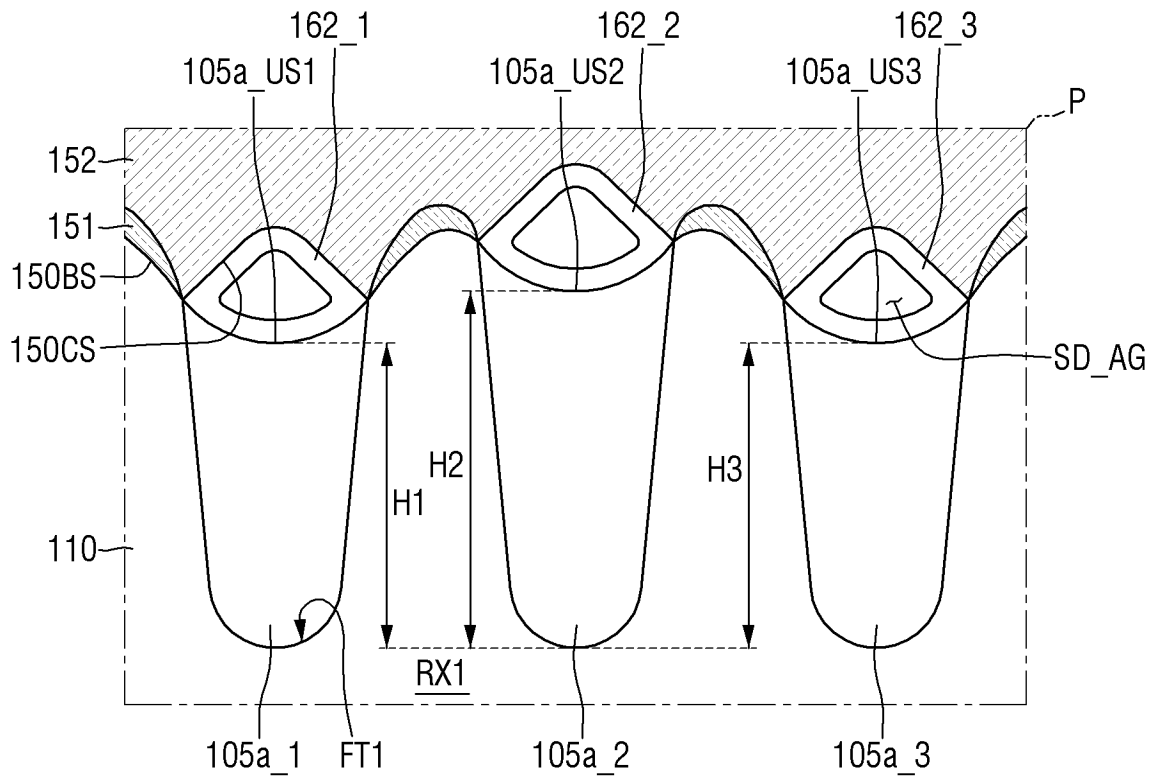


FIG. 13

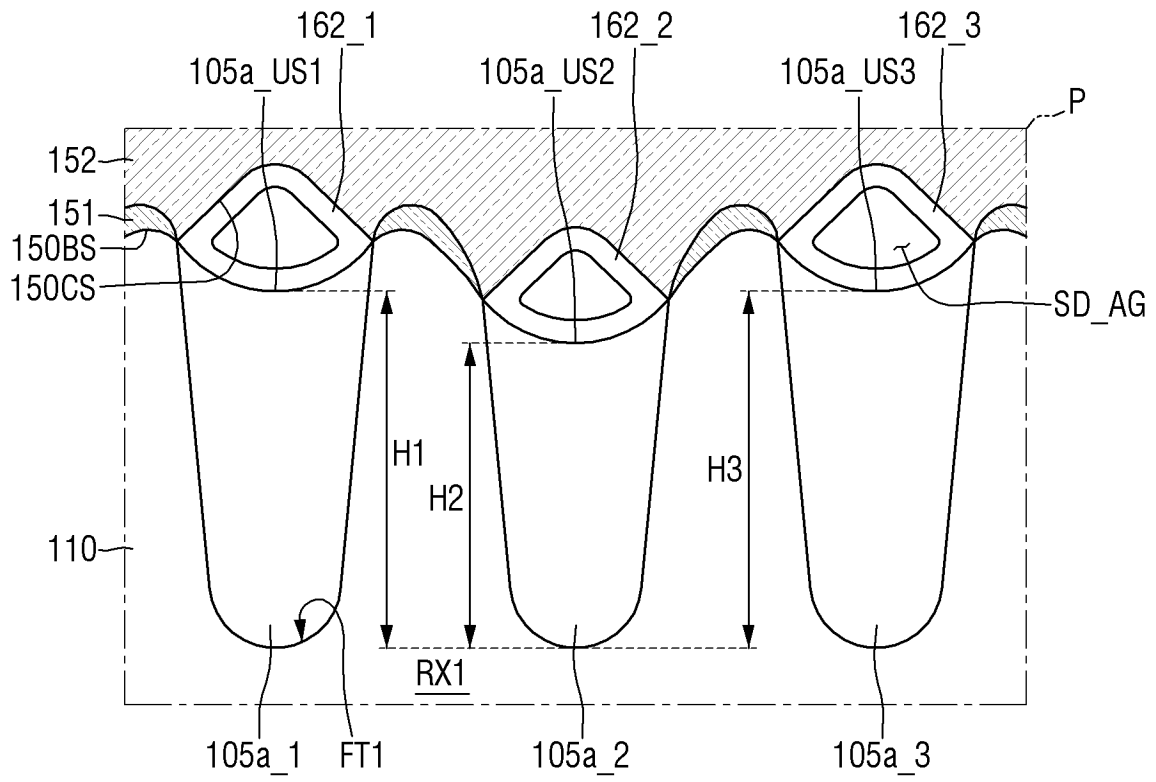


FIG. 14

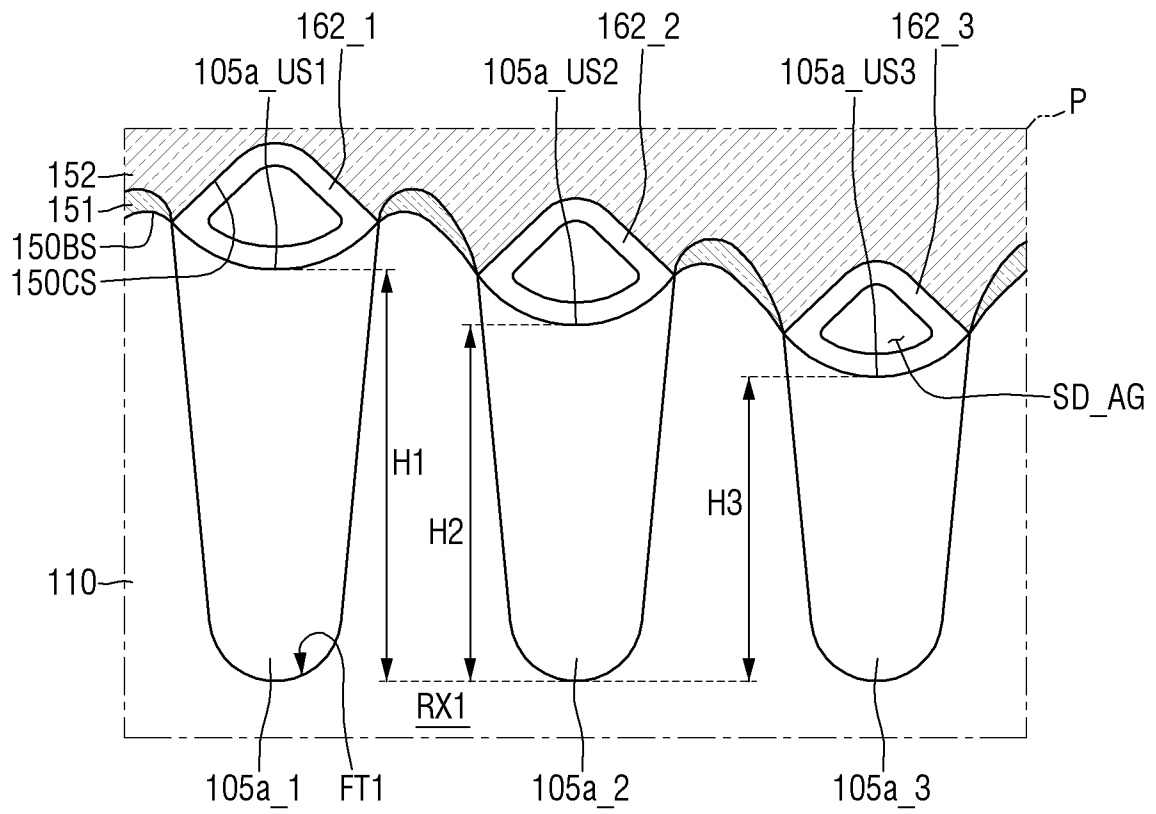


FIG. 15

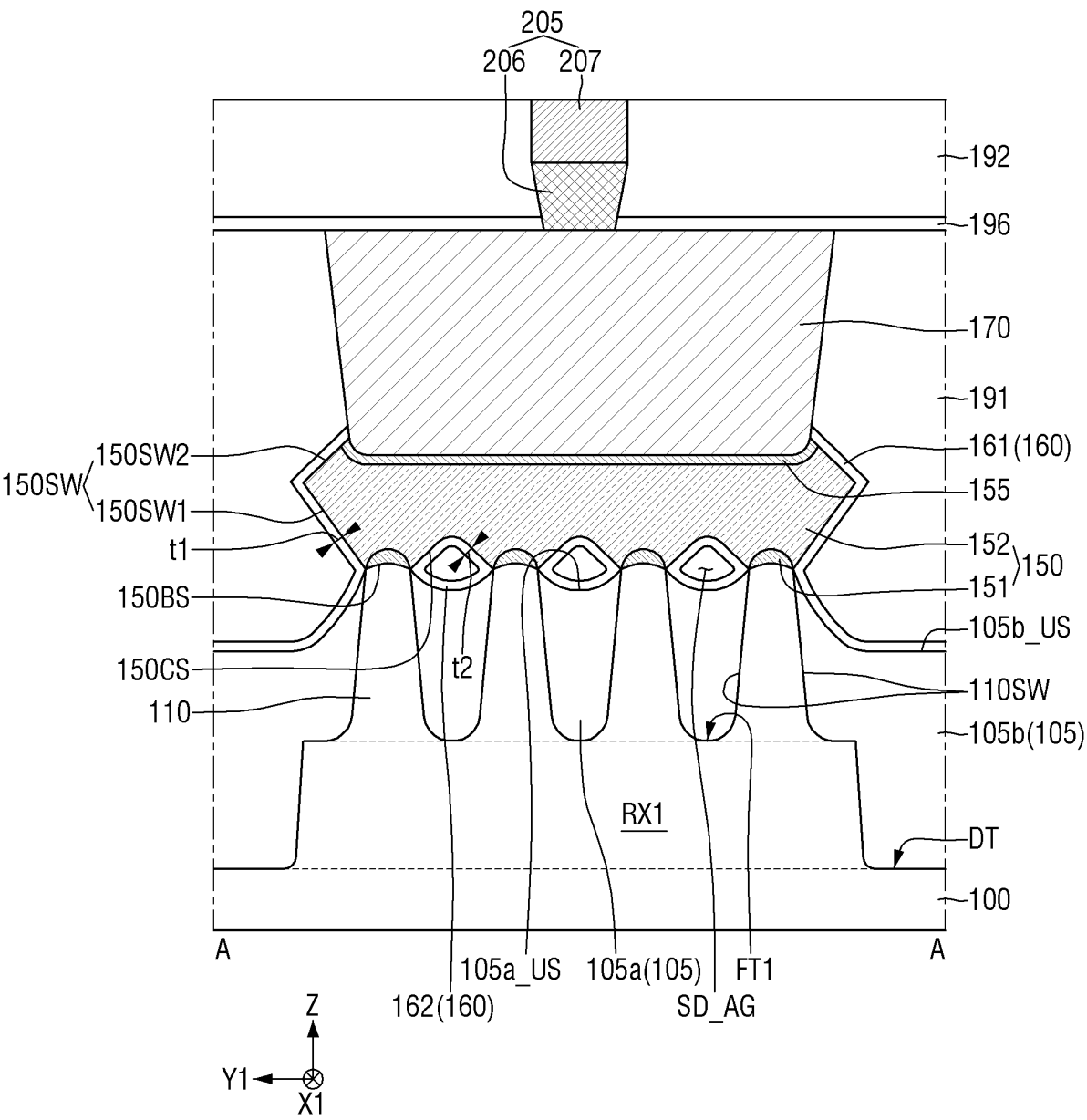


FIG. 16

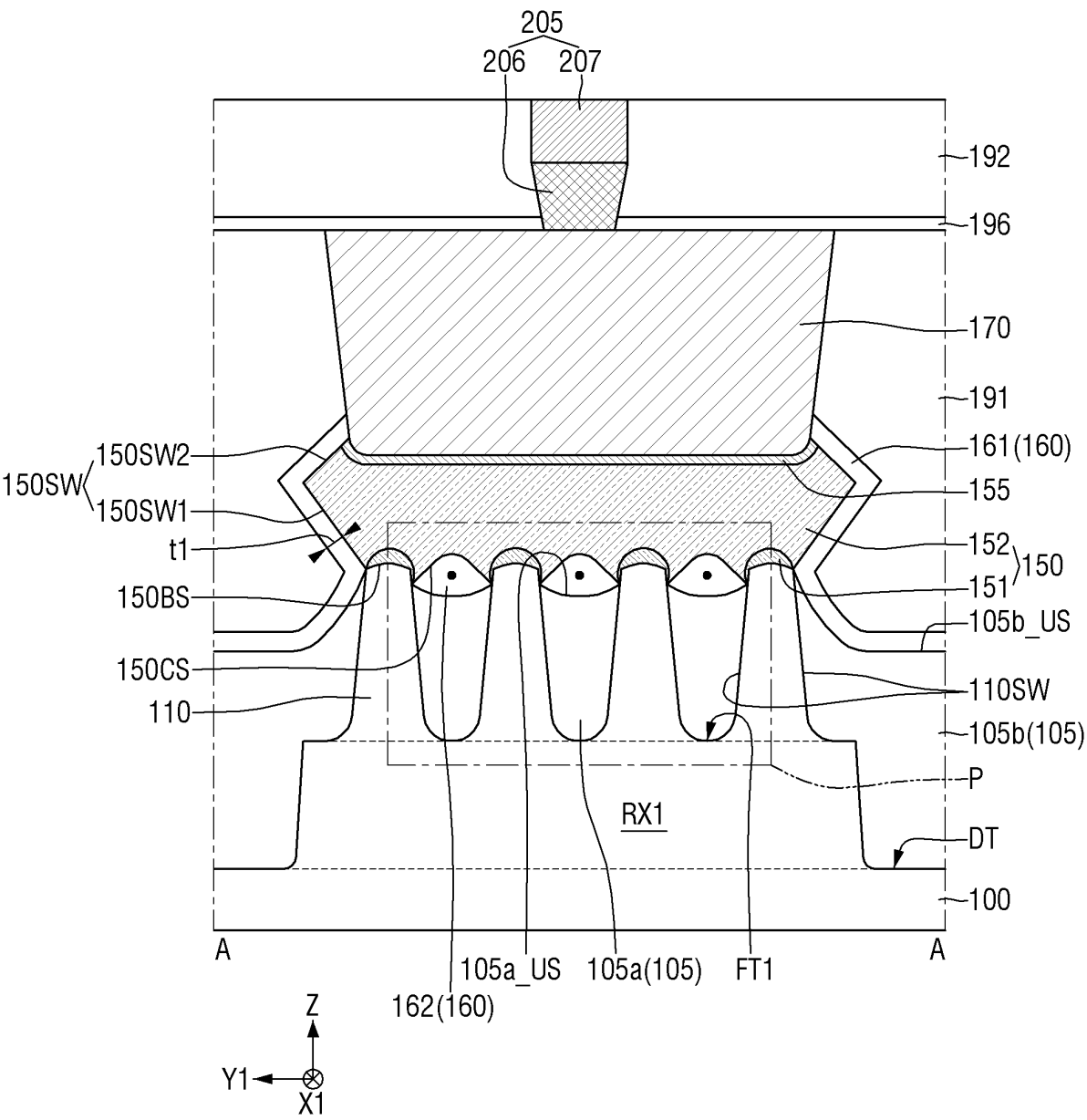


FIG. 17

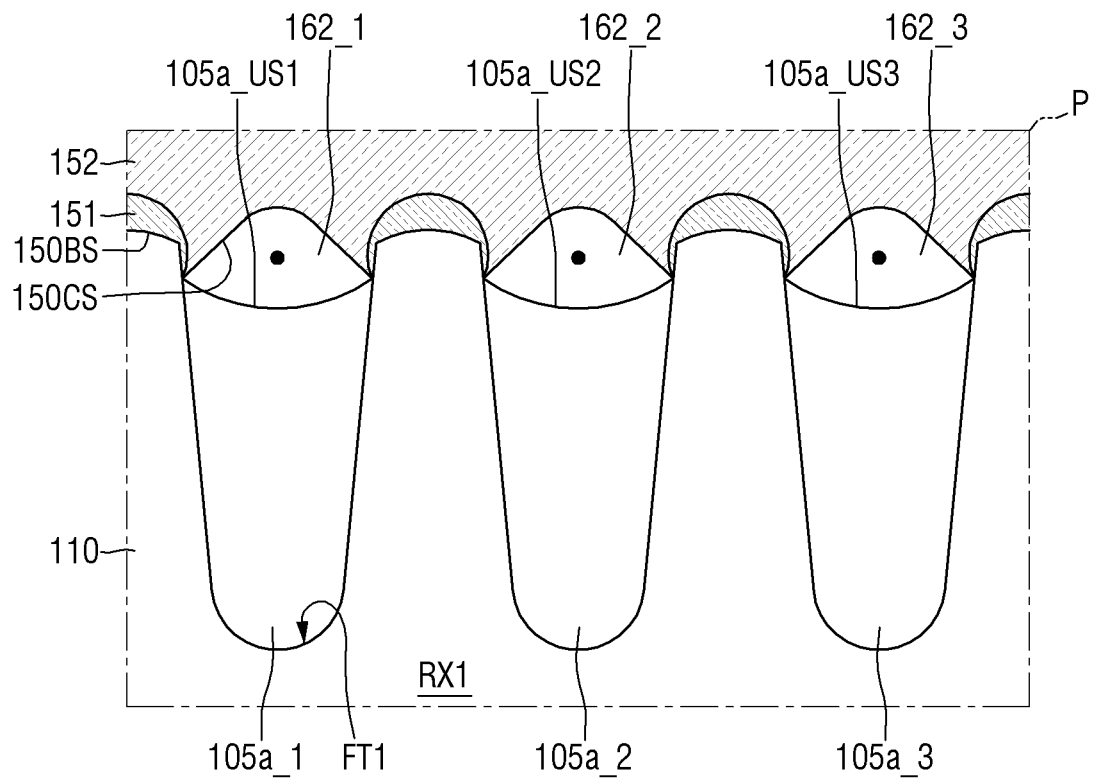


FIG. 18

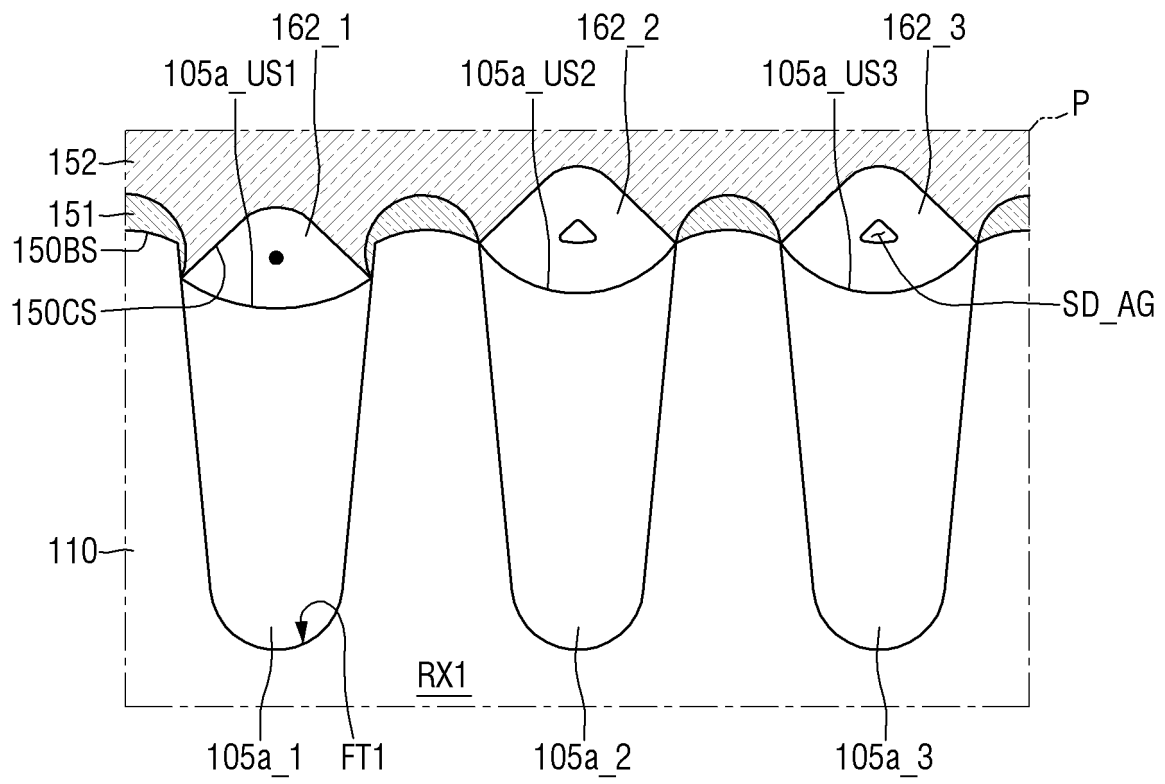


FIG. 19

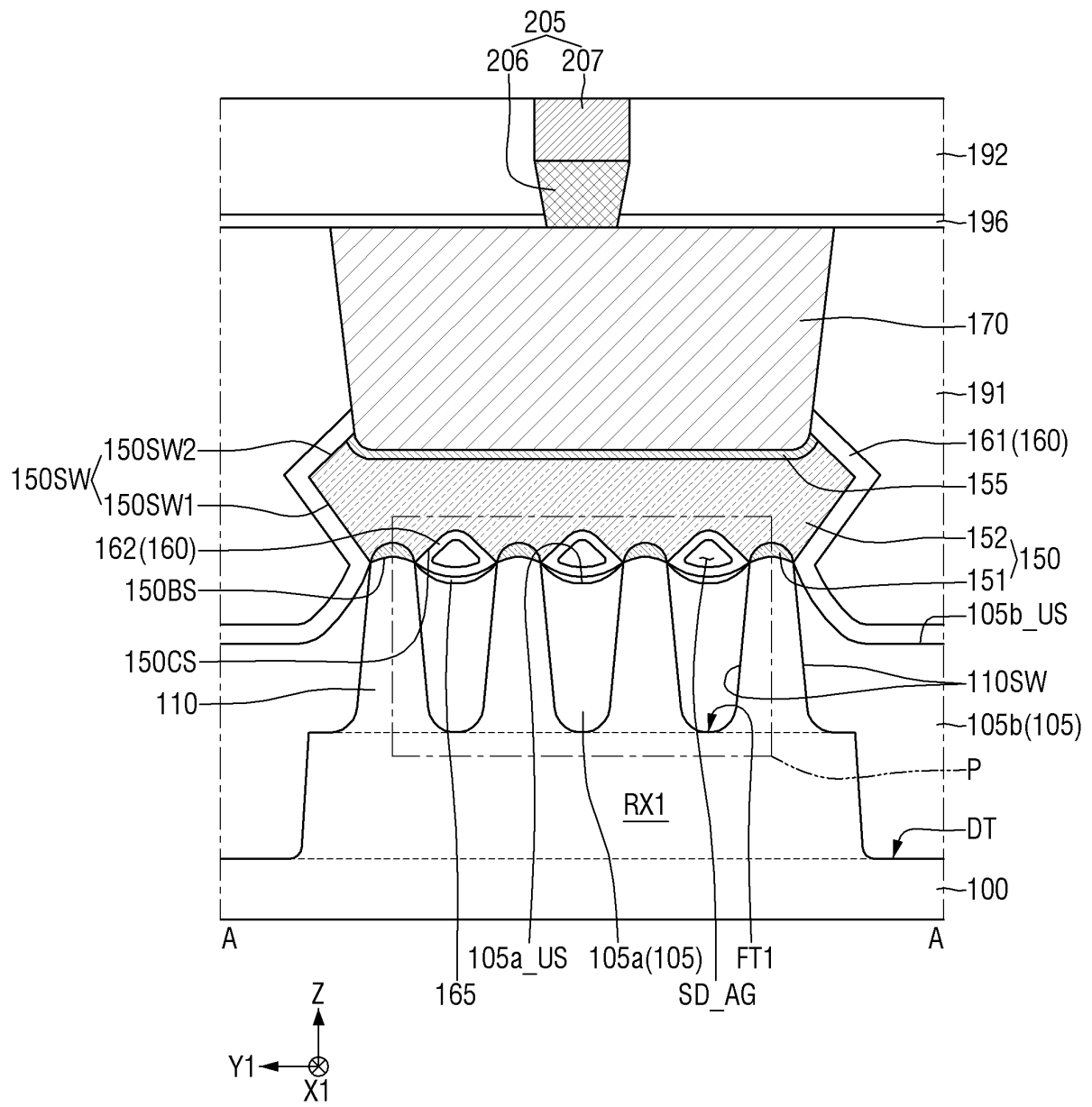


FIG. 20

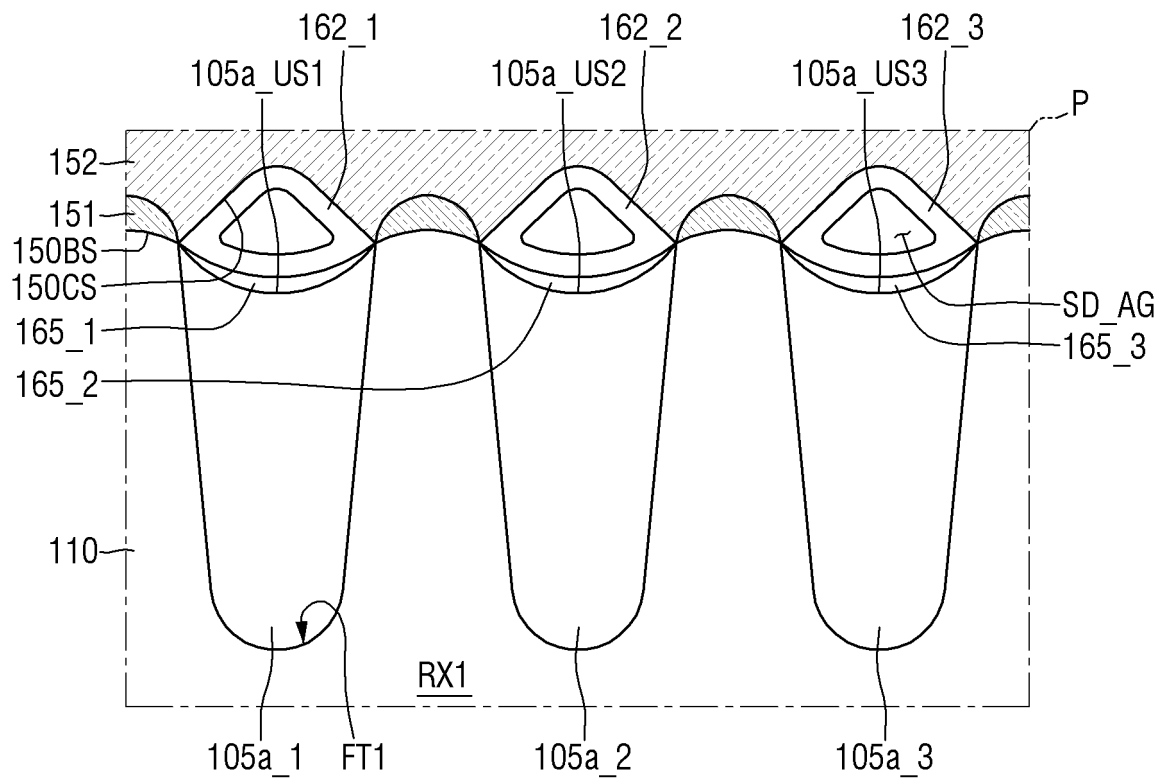


FIG. 21

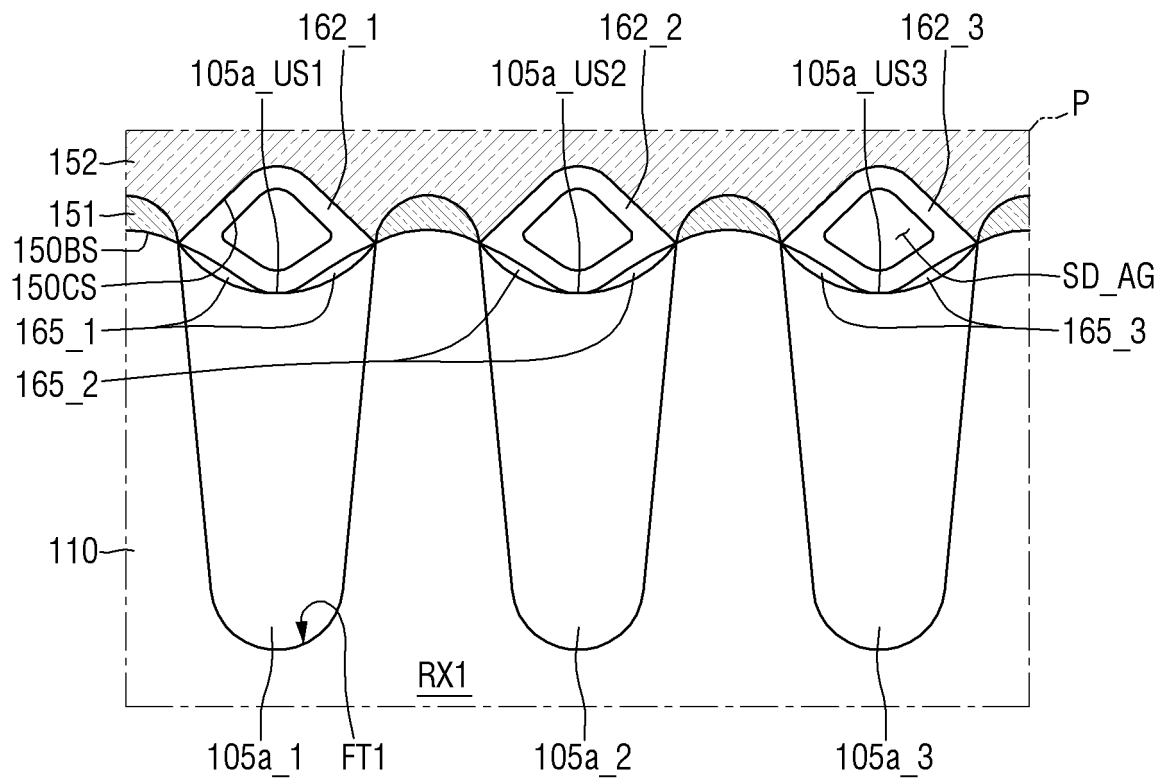


FIG. 22

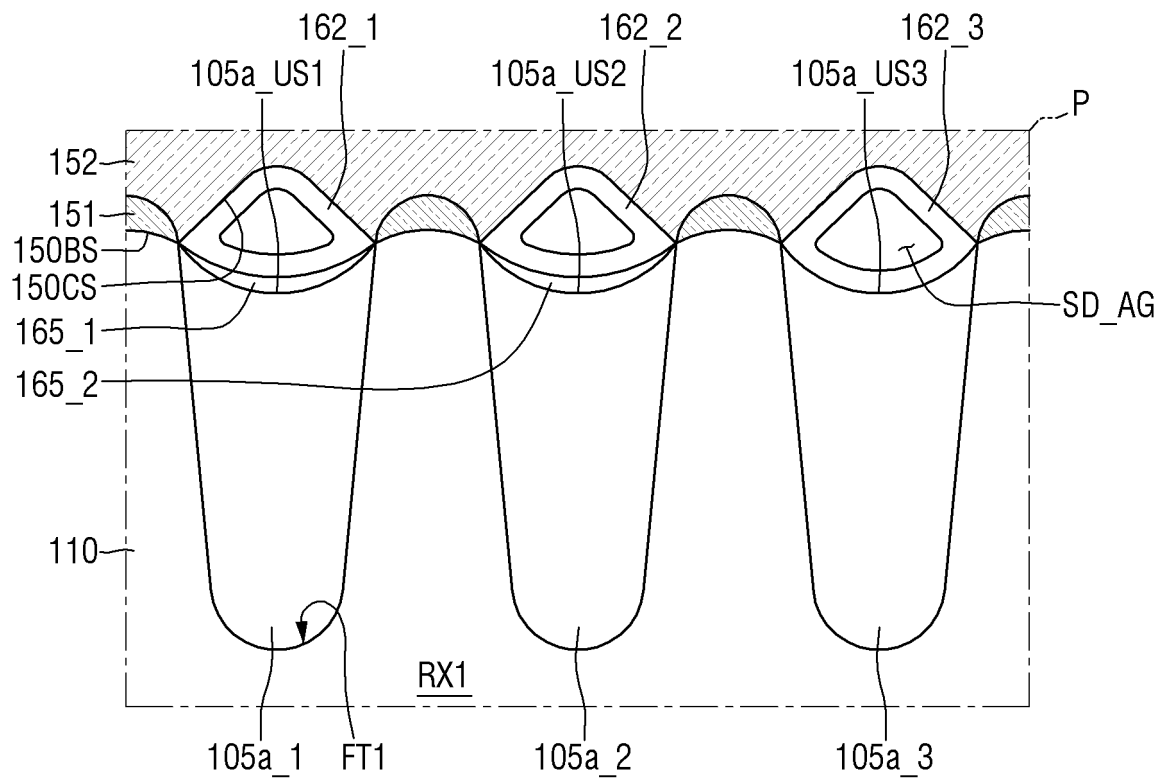


FIG. 23

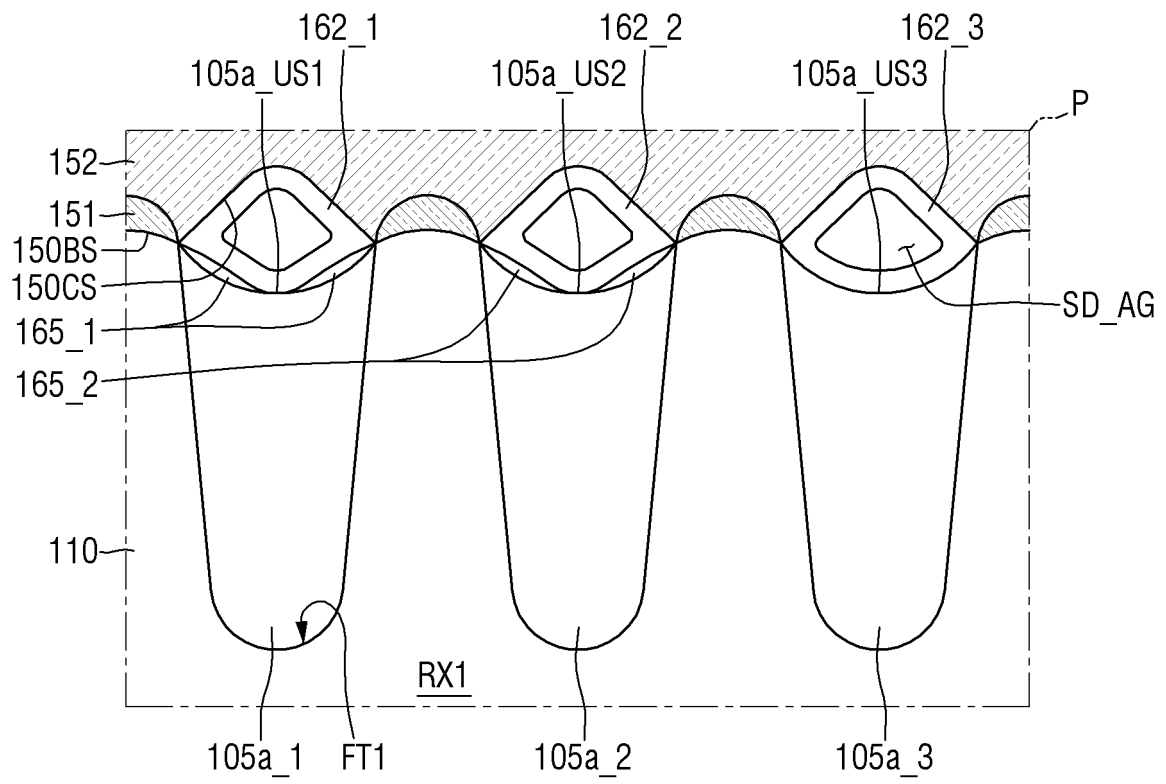


FIG. 24

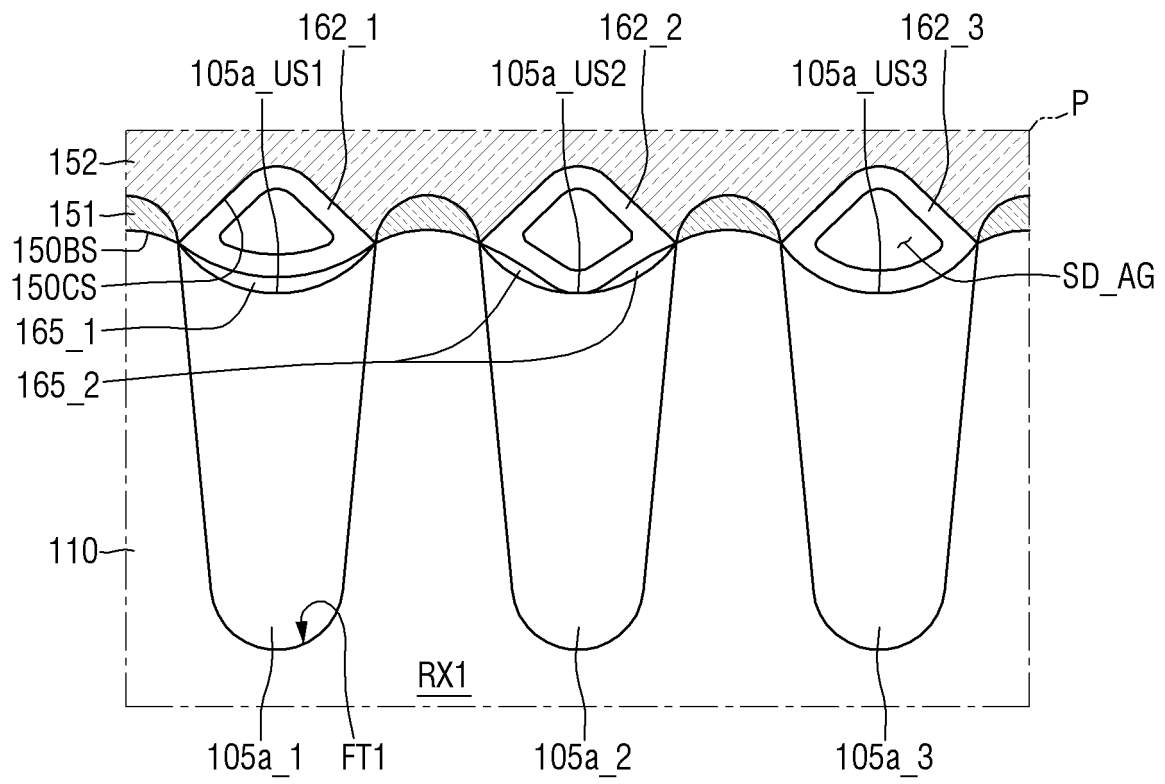


FIG. 25

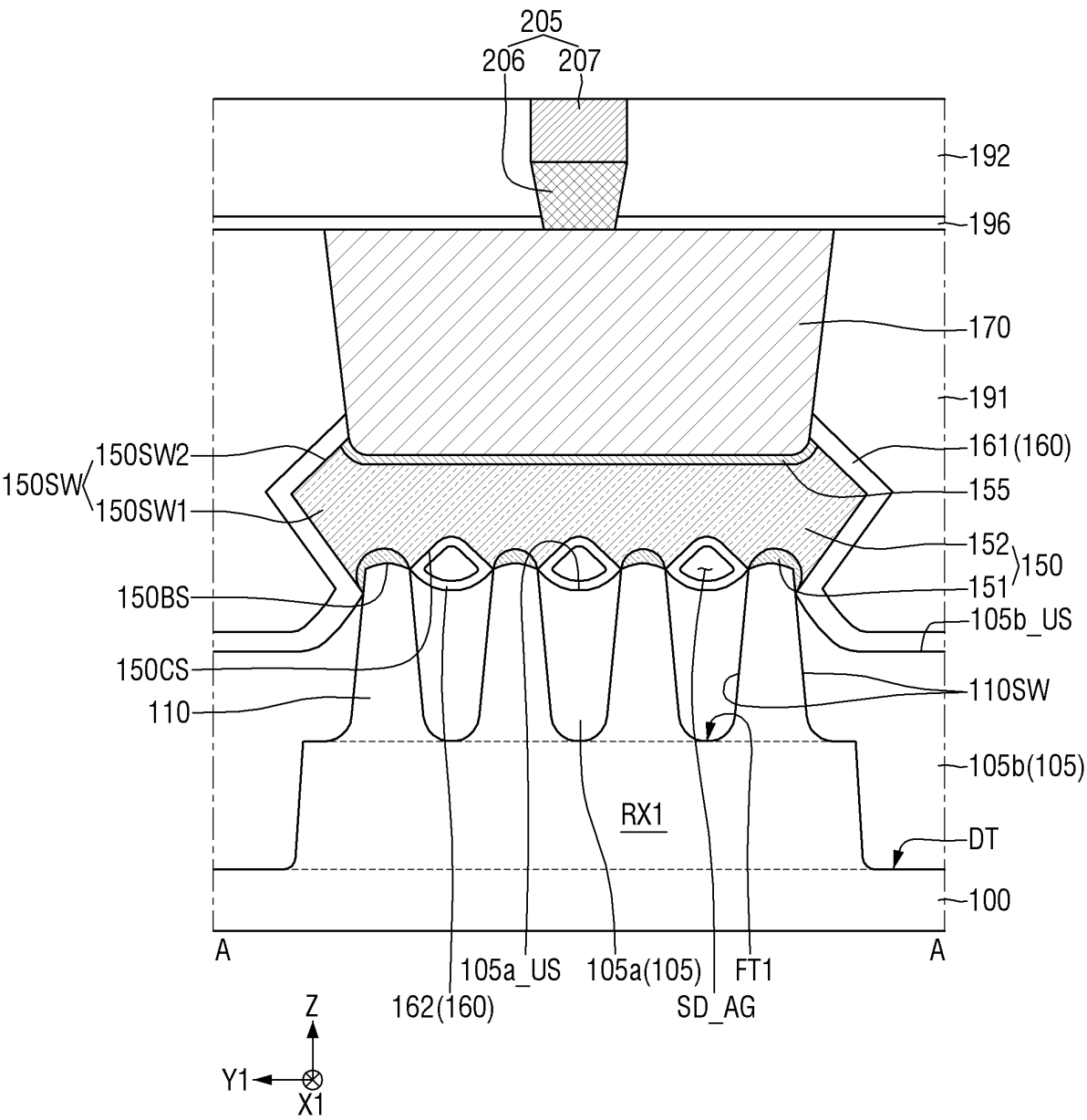


FIG. 26

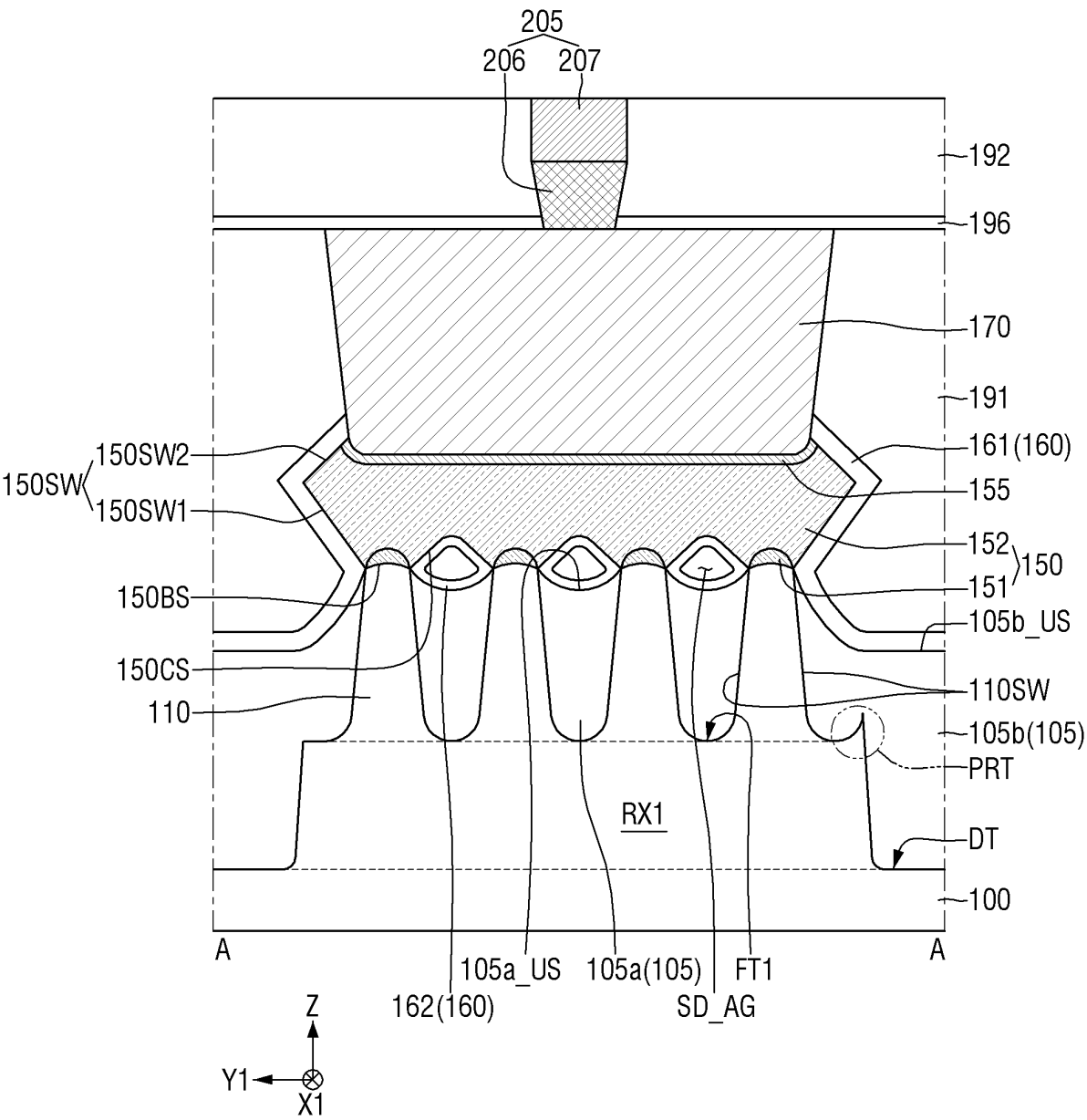


FIG. 27

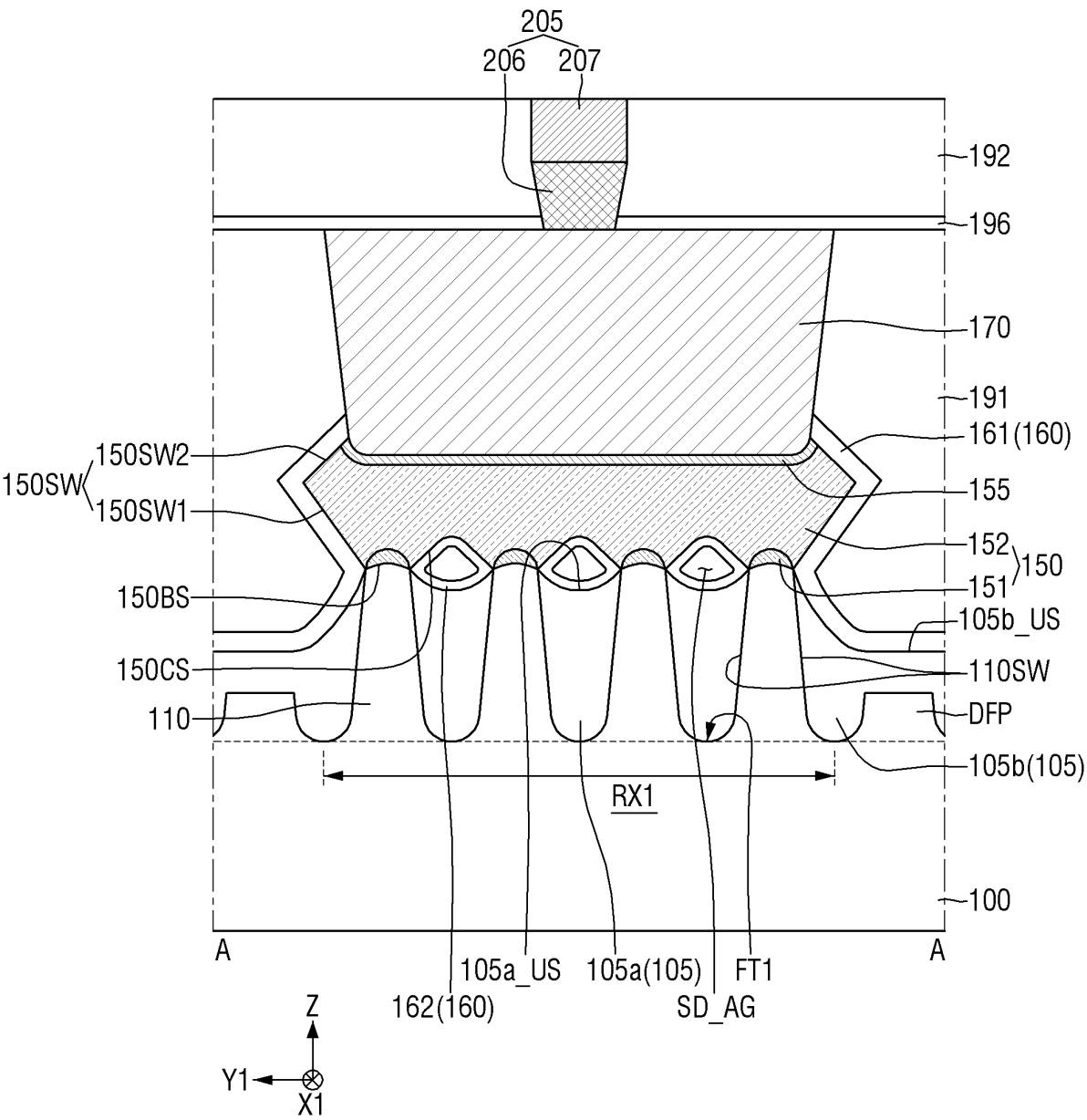


FIG. 29

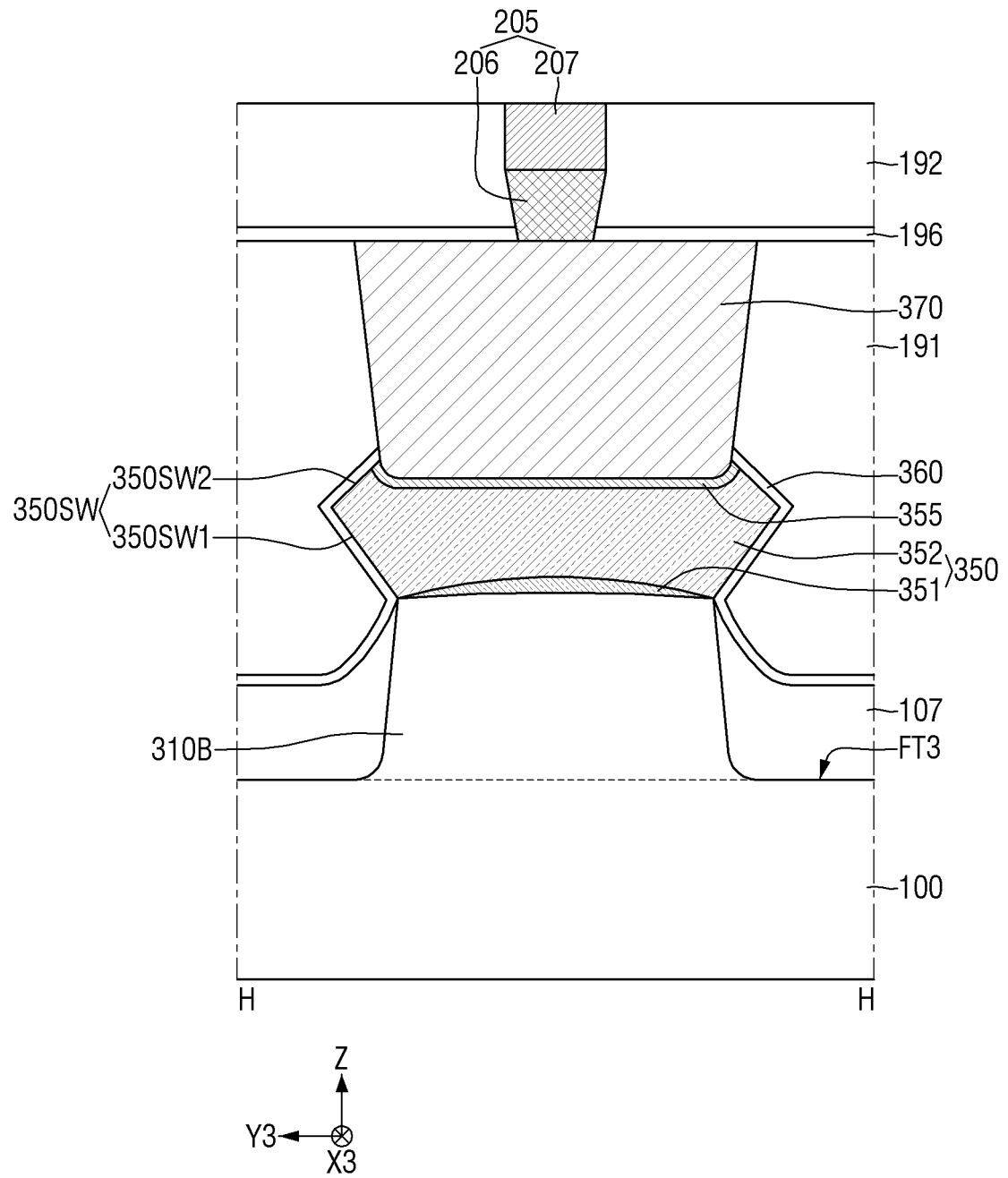


FIG. 30

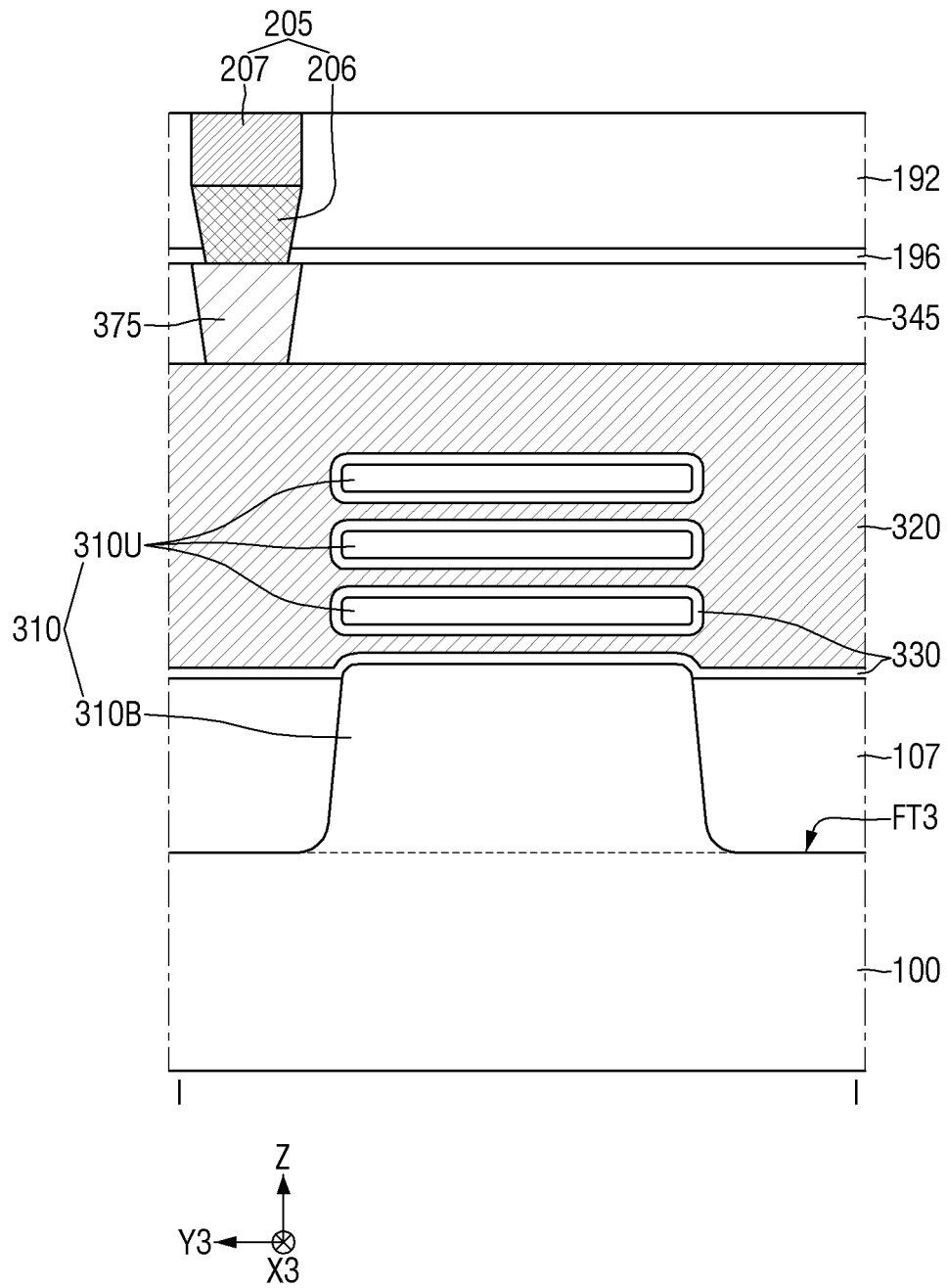


FIG. 31

