

ABSTRACT

METHOD OF FABRICATING STRAINED CHANNEL DEVICES

A process for forming both tensile and compressive strained silicon layers to accommodate channel regions of MOSFET or CMOS devices has been developed. After formation of shallow trench isolation structures as well as application of high temperature oxidation and activation procedures, the fabrication sequences used to obtain the strained silicon layers is initiated. A semiconductor alloy layer is deposited followed by an oxidation procedure used to segregate a germanium component from the overlying semiconductor alloy layer into an underlying single crystalline silicon body. The level of germanium segregated into the underlying single crystalline silicon body determines the level of strain, which is in tensile state of a subsequently selectively grown silicon layer. A second embodiment of this invention features the thinning of a portion of the semiconductor alloy layer prior to the oxidation procedure allowing a lower level of germanium to be segregated into a first underlying portion of the underlying single crystalline silicon body, while during the same oxidation procedure a second portion of the underlying single crystalline silicon body receives a higher level of germanium segregation. So the subsequently deposited silicon-germanium layer, although the same process and thickness, can be strained in different states (tensile or compressive) and levels, depending different underlying portions= germanium concentration.

Fig. 10