WHAT IS CLAIMED IS:

1. A static random access memory (SRAM) cell comprising:

first and second inverters cross-coupled for data storage, each inverter including a pull-up device (PU) and a plurality of pull-down devices (PDs);

a plurality of pass gate devices (PGs) configured with the two cross-coupled inverters; and

at least two ports coupled with the plurality of PGs for ~~reading and~~ writing, wherein:

each of the PU, PDs, and PGs includes a fin field-effect transistor (FinFET),

a ratio between a number of PDs in the ~~SRAM cell~~first and second inverters and a number of PGs in the ~~SRAM cell~~at least two ports is greater than 1, ~~and~~

a number of FinFETs in the SRAM cell is equal to or greater than 12;

a first metal layer providing local interconnection to the first and second inverters, the first metal layer including:

a first Vss line and a second Vss line;

a Vdd line;

a first constant voltage line and a second constant voltage line; and

a first bit line and a second bit line, wherein the first and second Vss lines, the Vdd line, the first and second constant voltage lines, and the first and second bit lines are oriented in a first direction;

a second metal layer formed over the first metal layer, the second metal layer including a first word line and a second word line oriented in a second direction that is different from the first direction, wherein the first word line is a write word line and the second word line is a read word line; and

a read port for reading, wherein the read port includes at least two PDs in parallel and at least two PGs in parallel.

~~2. The SRAM cell of claim 1, wherein each FinFET includes a channel having a top portion with a first width and a sidewall portion with a second width, the first width being less than the second width.~~

~~3~~2. The SRAM cell of claim 1, further comprising a plurality of FinFETs formed on a plurality of fin-type active regions.

~~4~~3. The SRAM cell of claim 1, wherein the ratio is equal to one of 3/2, 2, and 5/4.

~~5~~4. The SRAM cell of claim 1, further comprising at least four pass-gate devices, at least six pull-down devices, and at least two pull-up devices.

~~6~~5. The SRAM cell of claim ~~5~~4, comprising:

a first PU (PU1), a first PD (PD11), a second PD (PD12), and a third PD (PD13) configured to form the first inverter, wherein drains of PU1, PD11, PD12, and PD13 are electrically connected to form a first drain node;

a second PU (PU2), a fourth PD (PD21), a fifth PD (PD22), and a sixth PD (PD23) configured to form the second inverter, wherein drains of PU2, PD21, PD22, and PD23 are electrically connected to form a second drain node;

a first PG (PG1) and second PG (PG2) configured to form a first port, wherein:

a first drain of PG1 is electrically connected to a bit-line of the first port,

a second drain of PG2 is electrically connected to a bit-line bar of the first port,

a first source of PG1 is electrically connected to the first drain node, and

a second source of PG2 is electrically connected to the second drain node; and

a third PG (PG3) and fourth PG (PG4) configured to form a second port, wherein:

a third drain of PG3 is electrically connected to a bit-line of the second port,

a fourth drain of PG4 is electrically connected to a bit-line bar of the second port,

a third source of PG3 is electrically connected to the first drain node, and

a fourth source of PG4 is electrically connected to the second drain node.

~~7~~6. A static random access memory (SRAM) cell comprising:

a first set of fin field-effect transistors (FinFETs) having two pull-up devices (PUs) and a first number of pull-down devices (PDs), wherein the two pull-up devices (PUs) and

the pull-down devices (PDs) are configured to form first and second cross-coupled inverters; ~~and~~

a second set of FinFETs having a second number of pass-gate devices (PGs), wherein the pass-gate devices (PGs) are configured to form at least two ports, wherein the first number is greater than the second number;

word lines connected to gates of the PGs, respectively;

bit lines connected to drains of the PGs, respectively; and

two Vss lines and a Vdd line, wherein the two Vss lines, the Vdd line, and the bit lines are formed in a first metal layer and oriented in a first direction, and the word lines are formed in a second metal layer over the first metal layer and oriented in a second direction different from the first direction, the word lines comprise a write word line and a read word line; and

a read port, wherein the read port includes at least two PDs in parallel and at least two PGs in parallel.

~~8~~7. The SRAM cell of claim ~~7~~6, wherein the first set and second set of FinFETs include at least 12 FinFETs.

~~9~~8. The SRAM cell of claim ~~7~~6, wherein a ratio between the first number and the second number is equal to one of 3:2, 2:1, or 5:4.

~~10~~9. The SRAM cell of claim ~~7~~6, wherein the first and second sets of FinFETs are formed on a plurality of fin active regions.

~~11~~10. The SRAM cell of claim ~~7~~6, wherein

the first inverter includes a first subset of the PDs, wherein drains of the first set of the PDs are electrically connected together through one of silicide, long contact line, and combinations thereof; and

the second inverter includes a second subset of the PDs, wherein drains of the second set of the PDs are electrically connected together through one of silicide, long contact line, and combination thereof.

~~12~~11. The SRAM cell of claim ~~7~~6, ~~further comprising:~~

~~word lines connected to gates of the PGs, respectively; and~~

~~bit lines connected to drains of the PGs, respectively,~~ wherein a ratio between a first length of the word lines and a second length of the bit lines is greater than about 3.5:1.

~~13. The SRAM cell of claim 12, further comprising two Vss lines and a Vdd line, wherein the two Vss lines, the Vdd line, and the bit lines are formed in a first metal layer and oriented in a first direction, and the word lines are formed in a second metal layer over the first metal layer and oriented in a second direction different from the first direction.~~

~~14~~12. The SRAM cell of claim ~~13~~6, wherein at least one of the Vdd line and the Vss lines is configured between two bit-lines for noise shielding.

~~15~~13. The SRAM cell of claim ~~7~~6, further comprising at least four Vss lines.

~~16~~14. A dual port static random access memory (SRAM) cell comprising:

a first inverter having a first pull-up transistor (PU1) and a first group of pull-down transistors (PDs);

a second inverter having a second pull-up transistor (PU2) and a second group of PDs, the second inverter being cross-coupled with the first inverter;

a first group of pass-gate transistors (PGs) coupled with the first and second inverters to form a first port; and

a second group of PGs coupled with the first and second inverters to form a second port;

wherein each of the PDs and PGs includes an n-type fin field-effect transistor (nFinFET) and each of the pull-up transistors includes a p-type fin field-effect transistor (pFinFET), and wherein there are more PDs than PGs in the SRAM cell;

a first metal layer providing local interconnection to the first and second inverters, the first metal layer including:

a first Vss line and a second Vss line;

a Vdd line positioned between the first and second Vss lines;

a first constant voltage line and a second constant voltage line; and

a first bit line and a second bit line, wherein the first and second Vss lines, the Vdd line, the first and second constant voltage lines, and the first and second bit lines are oriented in a first direction;

a second metal layer formed over the first metal layer, the second metal layer including a first word line and a second word line oriented in a second direction that is different from the first direction, wherein the first word line is a write word line and the second word line is a read word line; and

a read port, wherein the read port includes at least two PDs in parallel and at least two PGs in parallel.

~~17~~15. The SRAM cell of claim ~~16~~14, wherein

the first group of PDs includes 5 nFinFETs, wherein drains of the first group of PDs are connected through one of silicide and long contact line;

the second group of PDs includes 5 nFinFETs, wherein drains of the second group of PDs are connected through one of silicide and long contact line;

the first group of PGs includes 4 nFinFETs; and

the second group of PGs includes 4 nFinFETs.

~~18~~16. The SRAM cell of claim ~~16~~14, wherein

the first group of PDs includes PD11, PD12, and PD13;

the second group of PDs includes PD21, PD22, and PD23;

the first group of PGs includes PG1 and PG2;

the second group of PGs includes PG3 and PG4; and

wherein the PD12 and PG1 are formed in a first continuous fin active region, and the PD22 and PG4 are formed in a second continuous fin active region.

~~19~~17. The SRAM cell of claim ~~16~~14, wherein:

the first group of PDs includes 6 nFinFETs formed on first four long fin active regions and first two short fin active regions;

the second group of PDs includes 6 nFinFETs formed on second four long fin

active regions and second two short fin active regions;

the first group of PGs includes 4 nFinFETs;

the second group of PGs includes 4 nFinFETs; and

wherein each of the first and second groups of PGs is formed on one of the first and second four long fin active regions.

~~20~~18. The SRAM cell of claim ~~16~~14, wherein:

the first group of PDs includes 4 nFinFETs formed on two fin active regions;

the second group of PDs includes 4 nFinFETs formed on another two fin active regions;

the first group of PGs includes PG1 and PG2;

the second group of PGs includes PG3 and PG4; and

wherein the PG1 and PG3 are formed in a first continuous fin active region, and the PG2 and PG4 are formed in a second continuous fin active region.