

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
13 March 2003 (13.03.2003)

PCT

(10) International Publication Number
WO 03/020998 A2

(51) International Patent Classification⁷: **C23C 14/18**,
14/34, H01L 27/24

(21) International Application Number: PCT/US02/27526

(22) International Filing Date: 30 August 2002 (30.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/943,426 30 August 2001 (30.08.2001) US

(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 South Federal Way, P.O. Box 6, Boise, ID 83707-0006
(US).

(72) Inventors: **LI, Jiutao**; 5325 E. Branchwood Drive, Boise,
ID 83716 (US). **MCTEER, Allen**; 3550 N. Summerside
Way, Meridian, ID 83642 (US).

(74) Agent: **THRONSON, Mark, J.**; Dickstein, Shapiro,
Morin & Oshinsky LLP, 2101 L Street, NW, Washington,
DC 20037-1526 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG,
SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC,
VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK,
TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished
upon receipt of that report*

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: INTEGRATED CIRCUIT DEVICE AND FABRICATION USING METAL-DOPED CHALCOGENIDE MATERIALS

(57) Abstract: Methods of forming metal-doped chalcogenide layers and devices containing such doped chalcogenide layers include using a plasma to induce diffusion of metal into a chalcogenide layer concurrently with metal deposition. The plasma contains at least one noble gas of low atomic weight, such as neon or helium. The plasma has a sputter yield sufficient to sputter a metal target and a UV component of its emitted spectrum sufficient to induce diffusion of the sputtered metal into the chalcogenide layer. Using such methods, a conductive layer can be formed on the doped chalcogenide layer (in situ.) In integrated circuit devices, such as non-volatile chalcogenide memory devices, doping of the chalcogenide layer concurrently with metal deposition and formation of a conductive layer (in situ) with the doping of the chalcogenide layer reduces contamination concerns and physical damage resulting from moving the device substrate from tool to tool, thus facilitating improved device reliability.a



WO 03/020998 A2