NAND-STRUCTURED AND AMORPHOUS SILICON BASED READ-ONLY MEMORY DEVICE AND METHOD OF FABRICATING THE SAME

ABSTRACT

A NAND-structure and amorphous-silicon based ROM device is provided. This ROM device is of the type including an array of MOSFET memory cells that are constructed based on a silicon-on-insulator (SOI) structure, so as to isolate the source/drain regions from the underlying substrate to prevent the occurrence of leakage current therebetween. Further, the SOI structure prevents occurrence of breakdown at the diode junction between the source/drain regions and the substrate for increased operating voltage. In this ROM device, the source/drain regions for the MOSFET memory cells are formed from the intrinsic amorphous-silicon, instead of highly-doped polysilicon, so that the fabrication process for the ROM device is significantly simplified.

Fig. 2H