

1/22

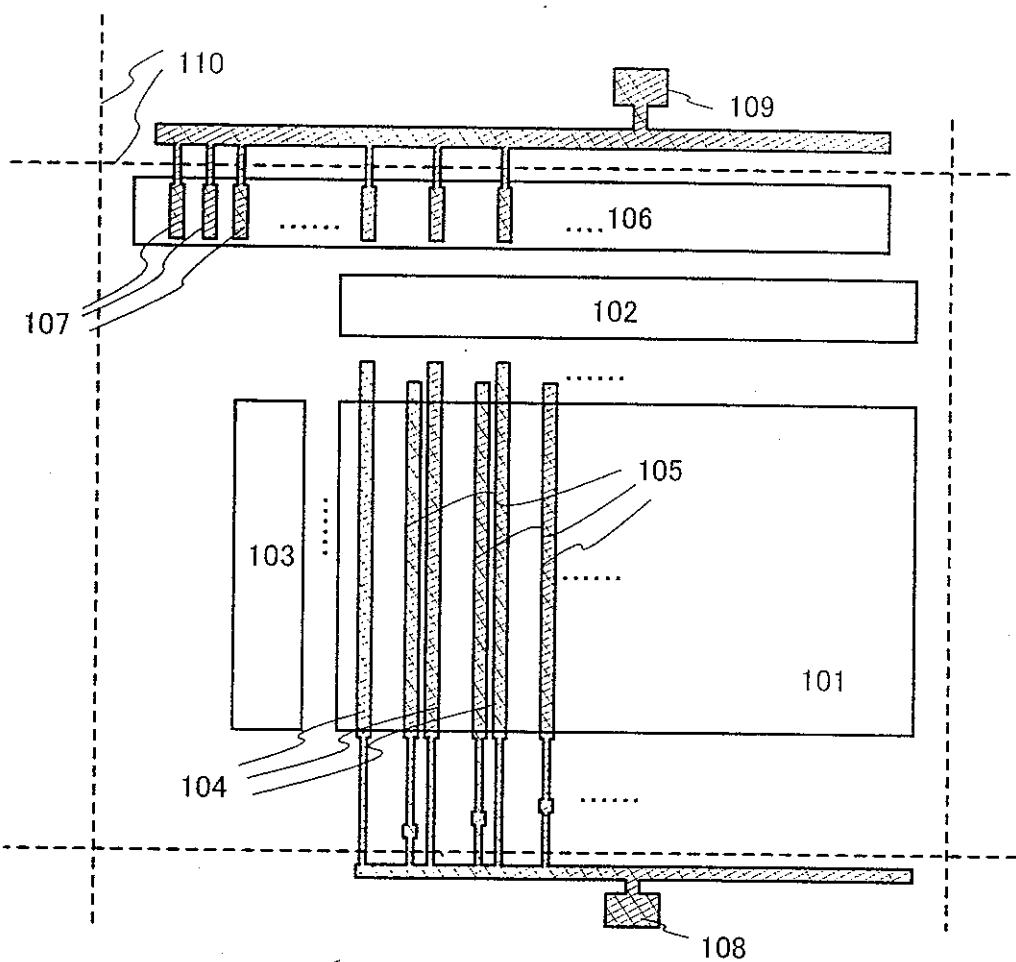


Fig. 1

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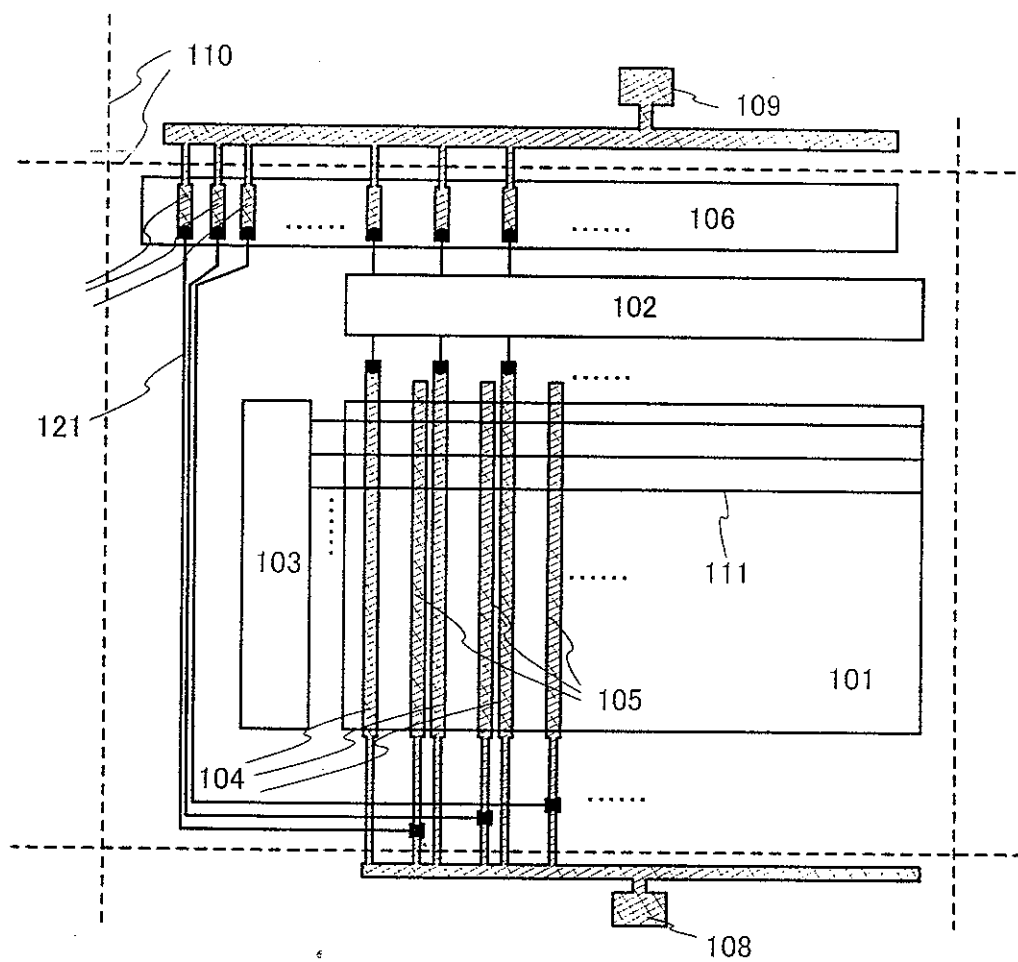


Fig. 2

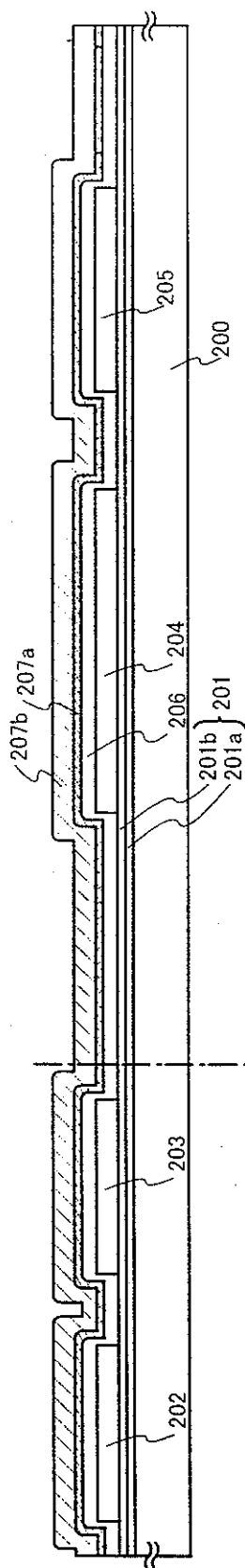
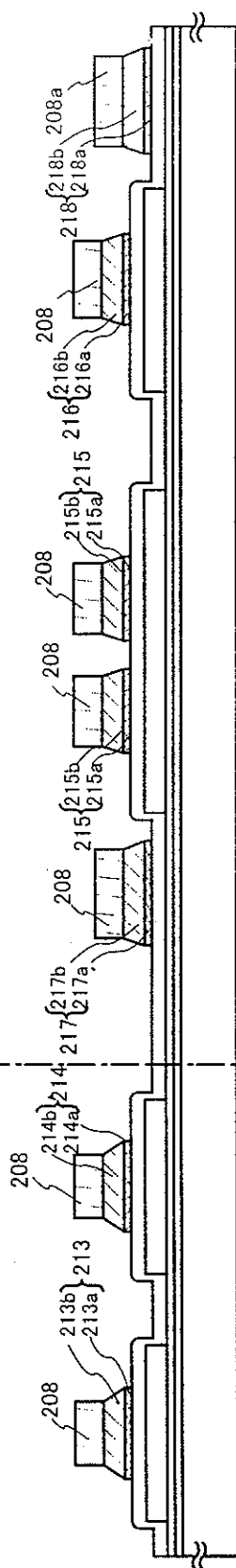
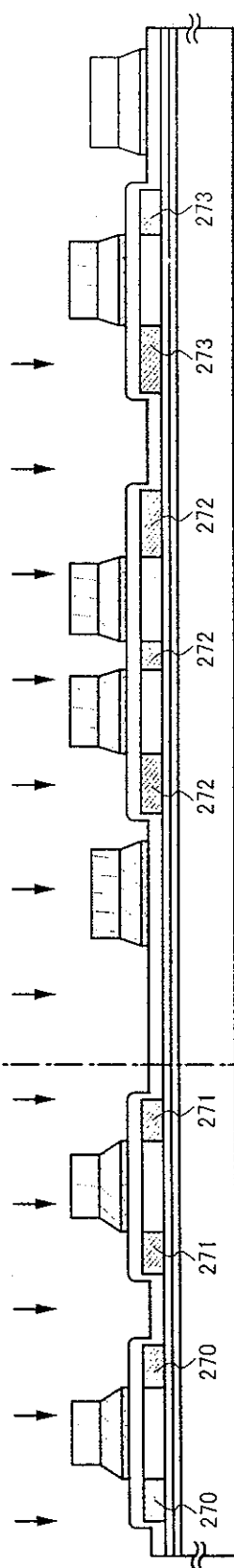


Fig. 3A



3. Fi bu



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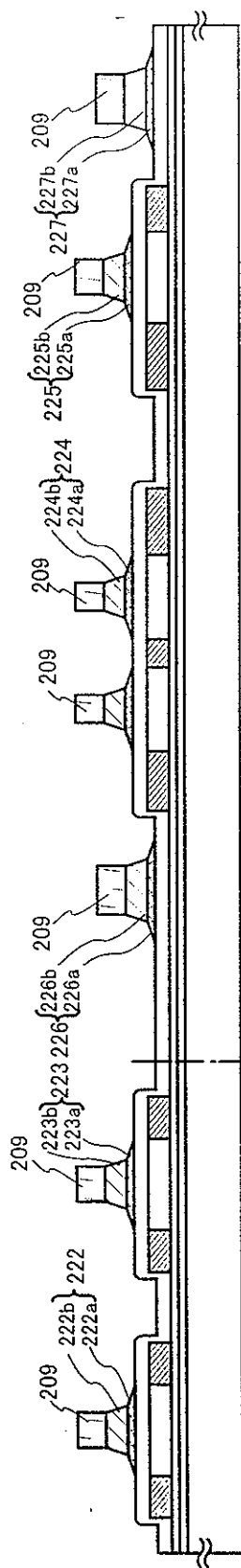


Fig. 4A

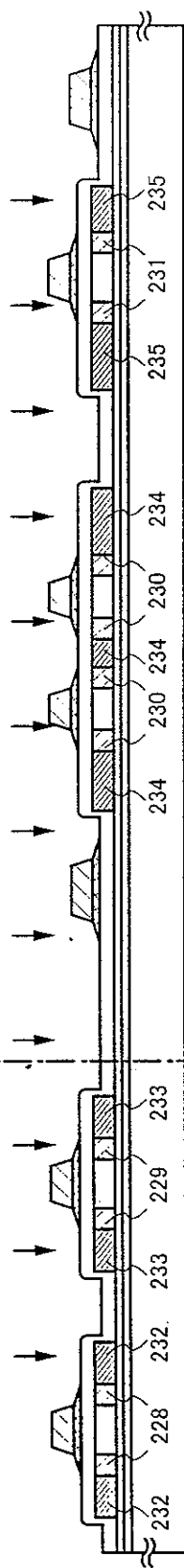


Fig. 4B

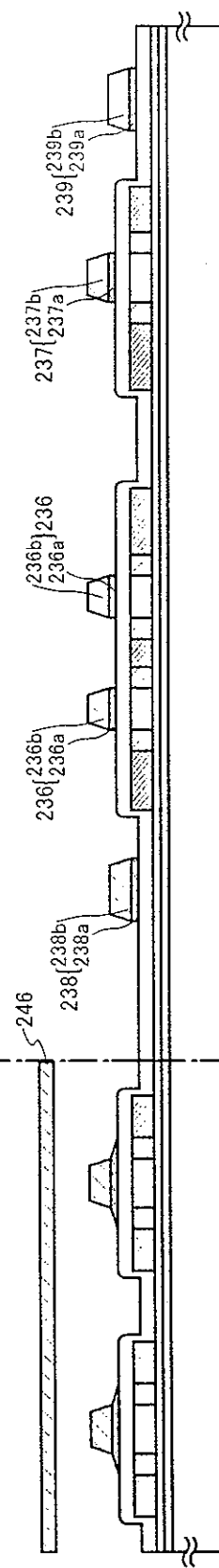


Fig. 4C

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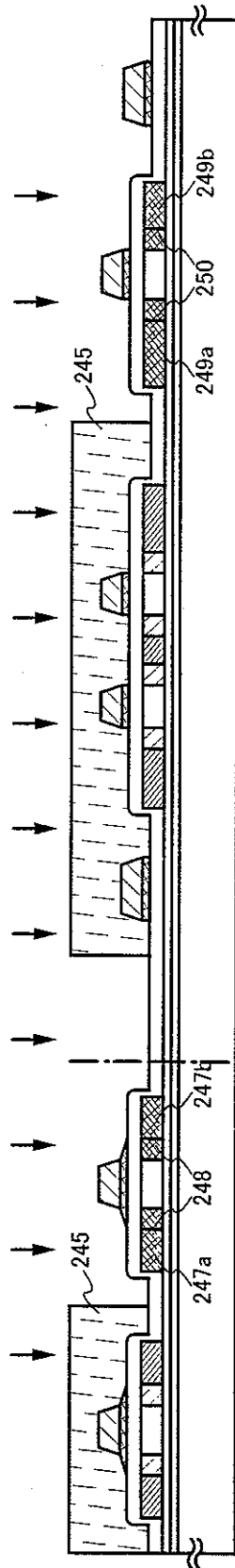


Fig. 5A

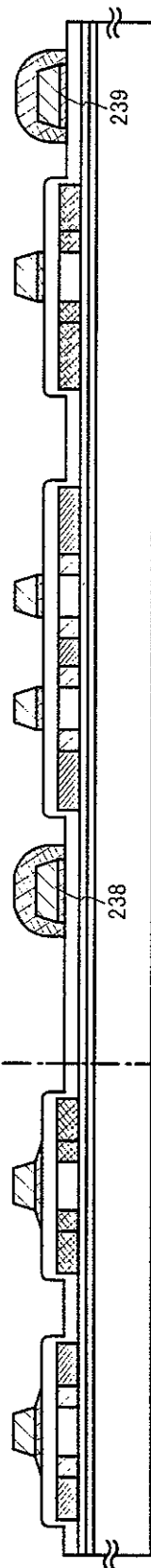


Fig. 5B

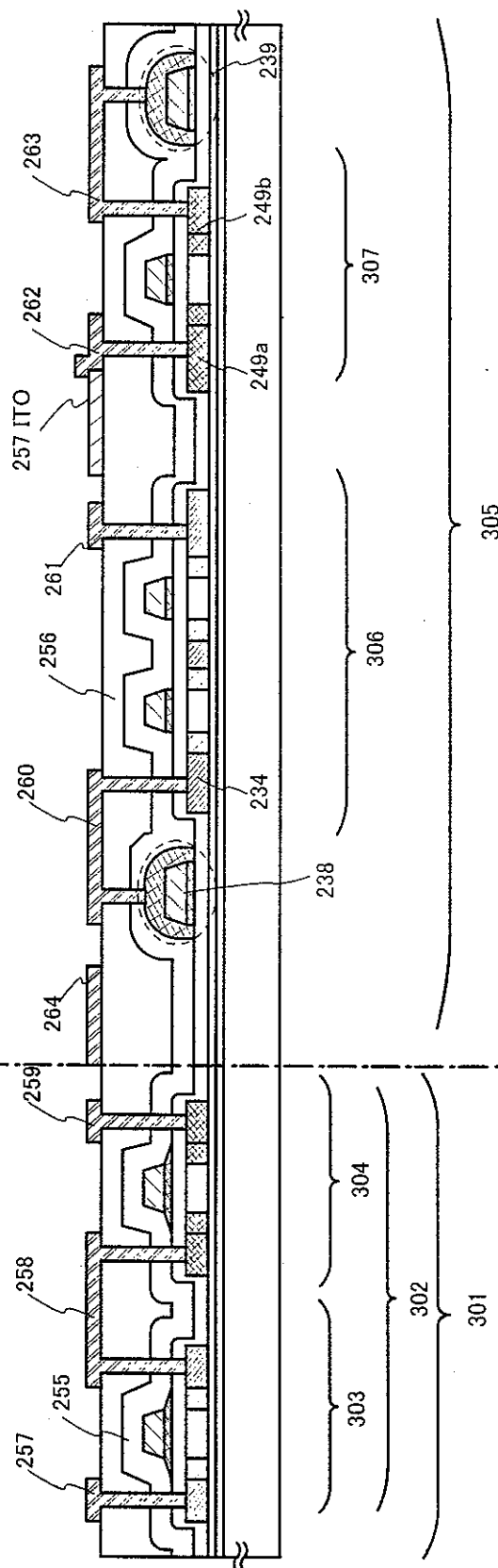


Fig. 5C

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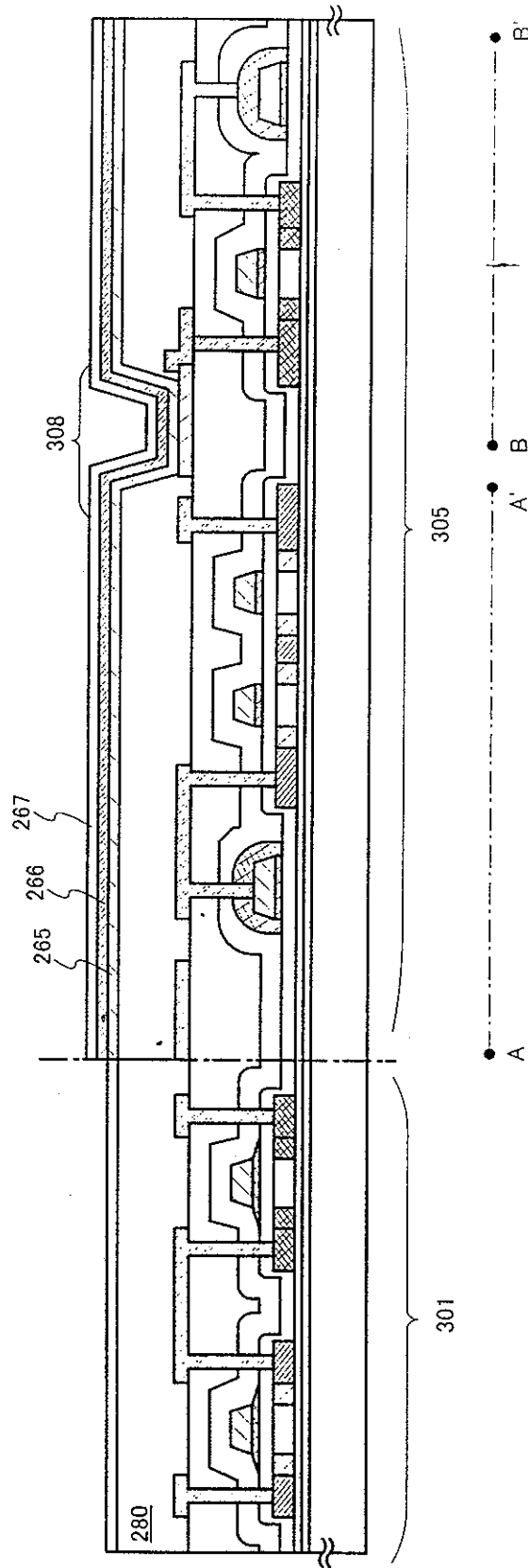


Fig. 6

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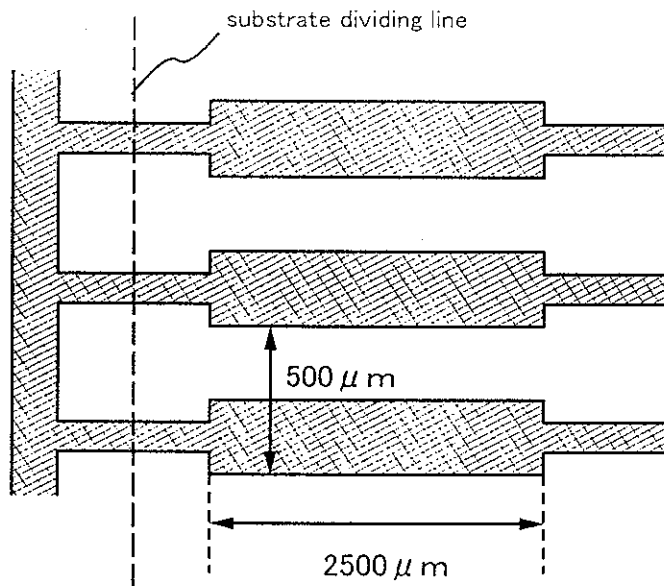


Fig. 7A

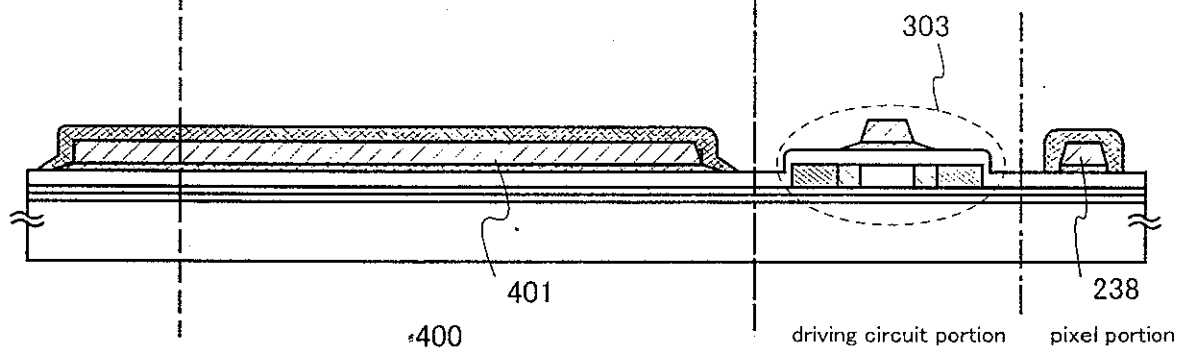


Fig. 7B

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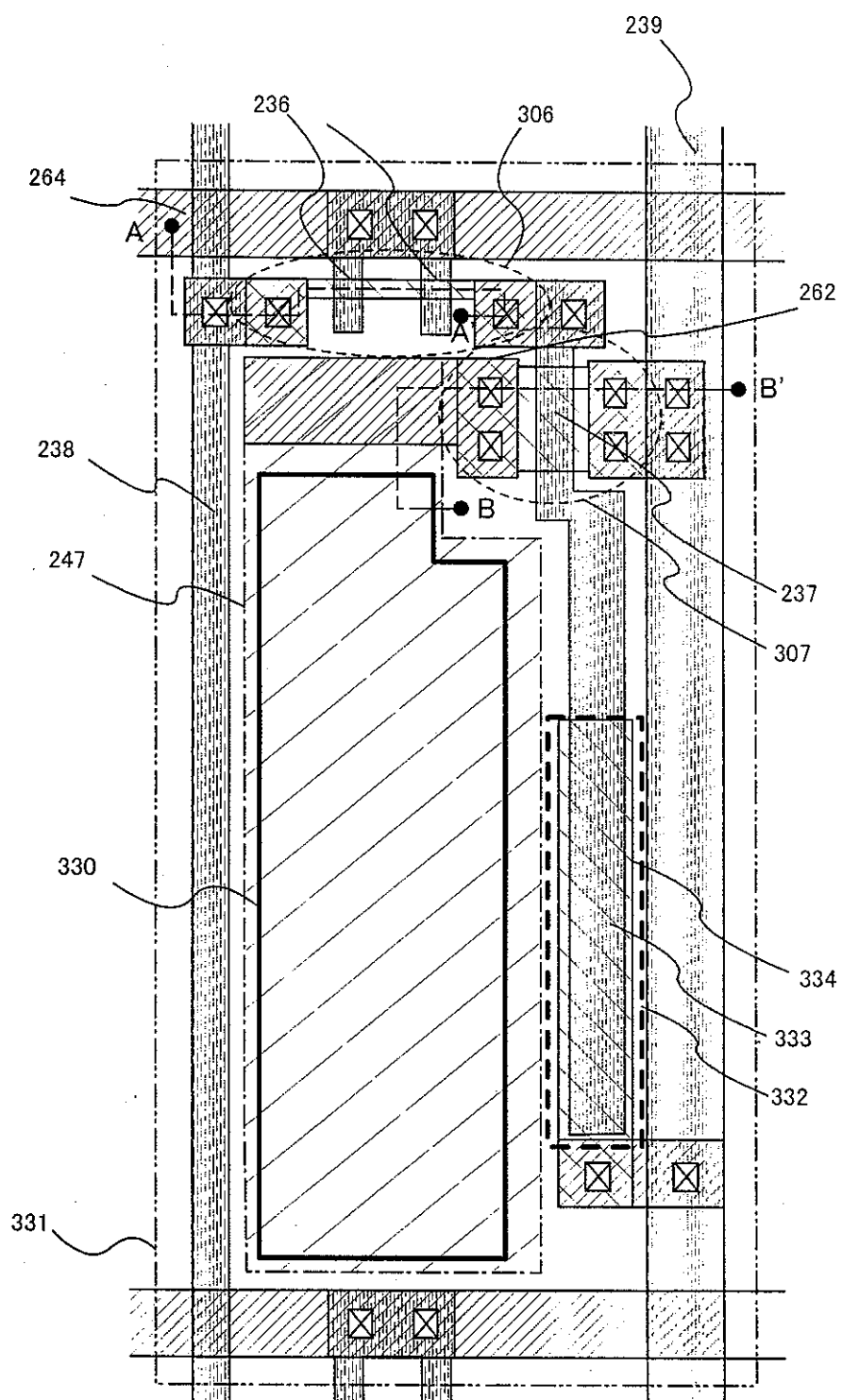


Fig. 8

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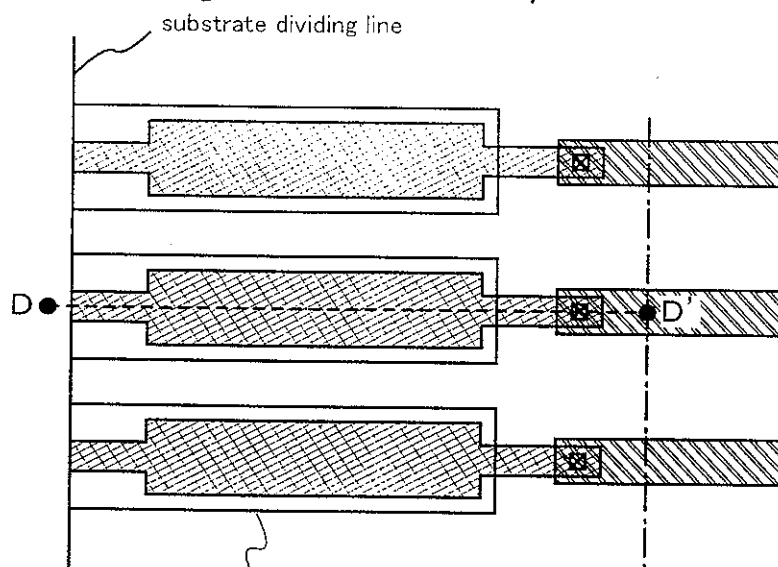


Fig. 9A

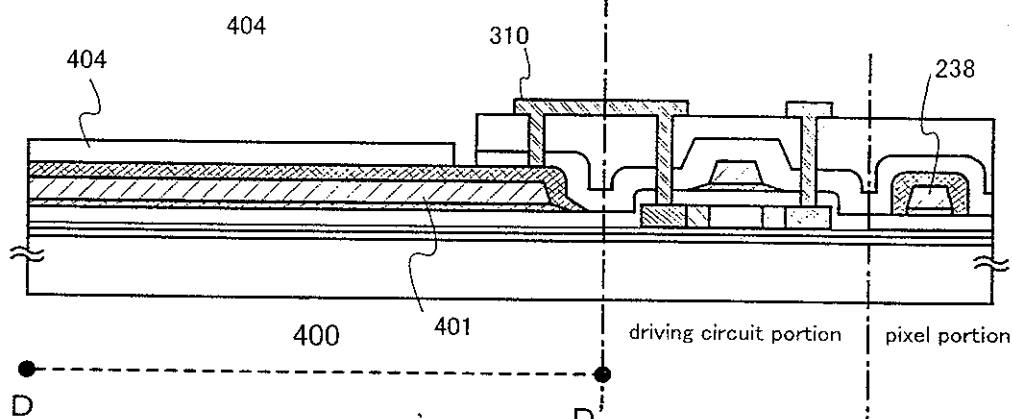


Fig. 9B

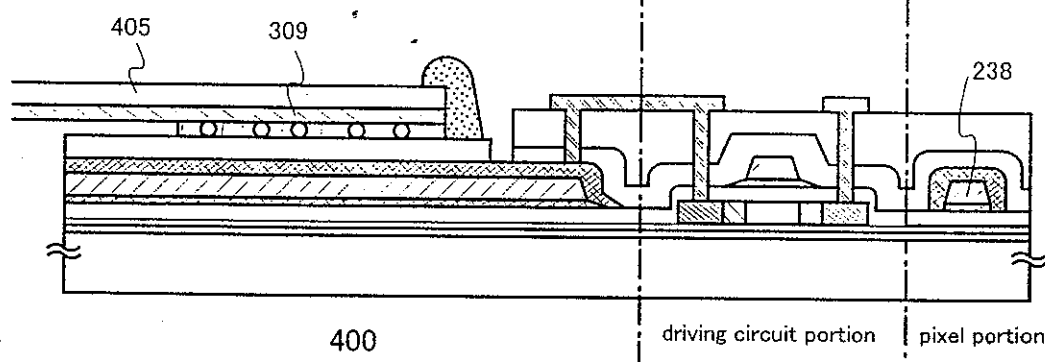


Fig. 9C

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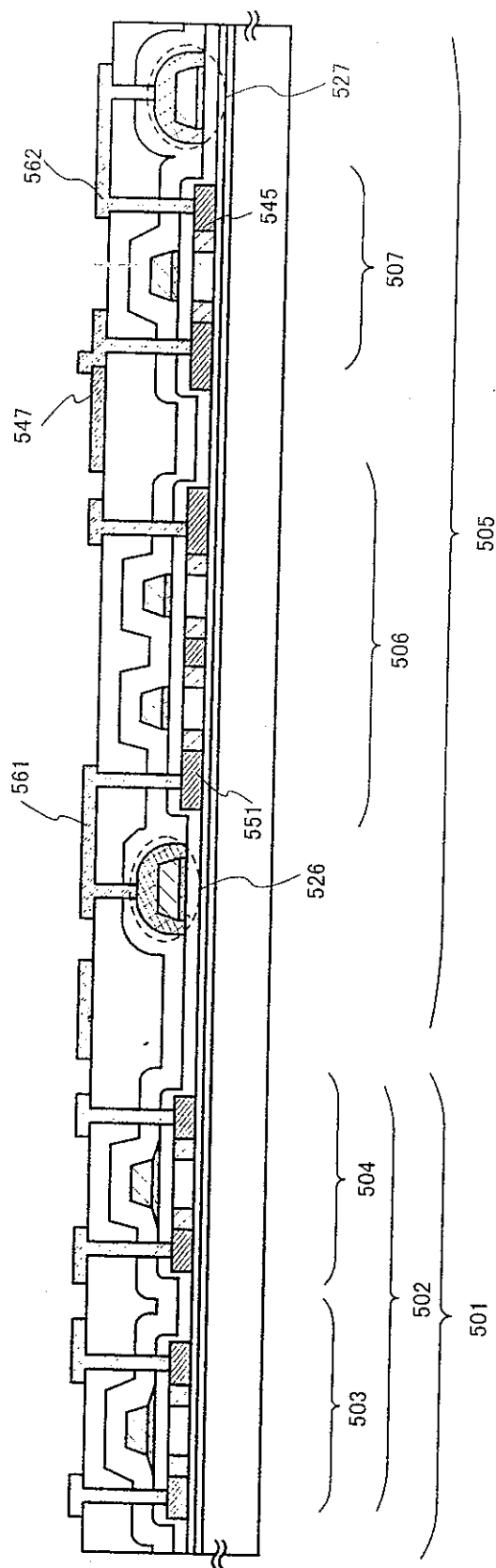


Fig. 10

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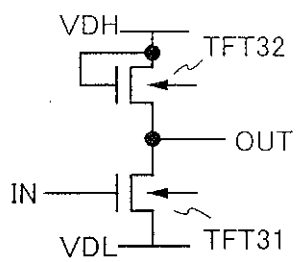


Fig. 11A EEMOS circuit

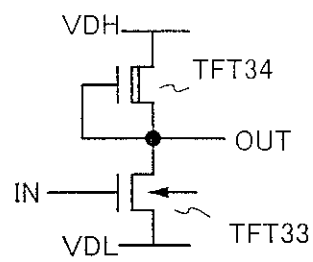


Fig. 11B EDMOS circuit

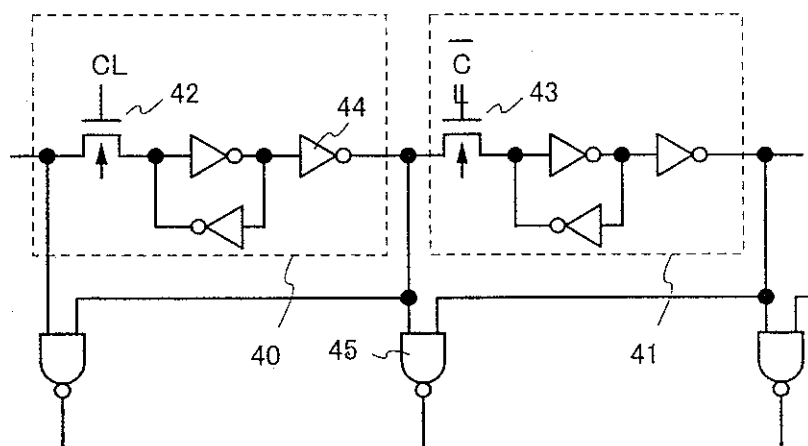


Fig. 12A

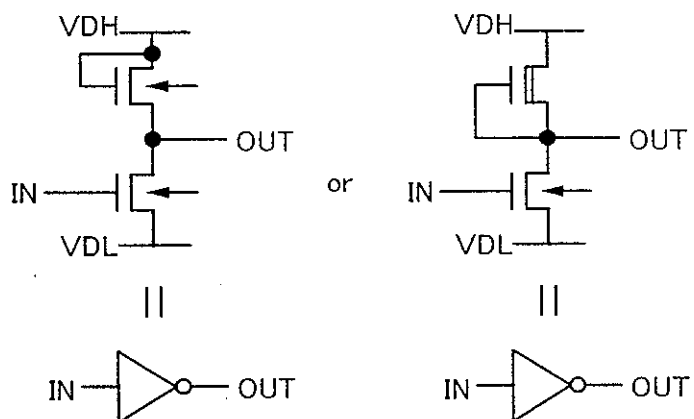


Fig. 12B

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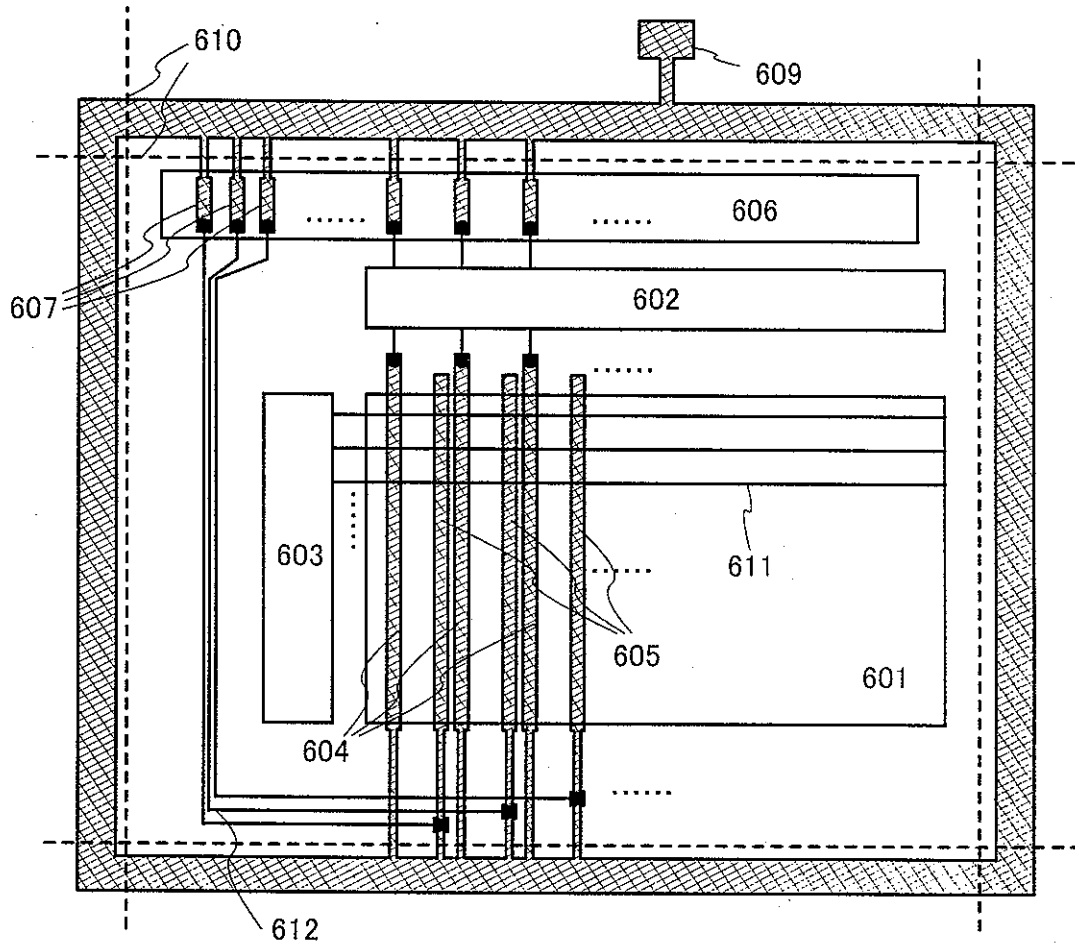


Fig. 13

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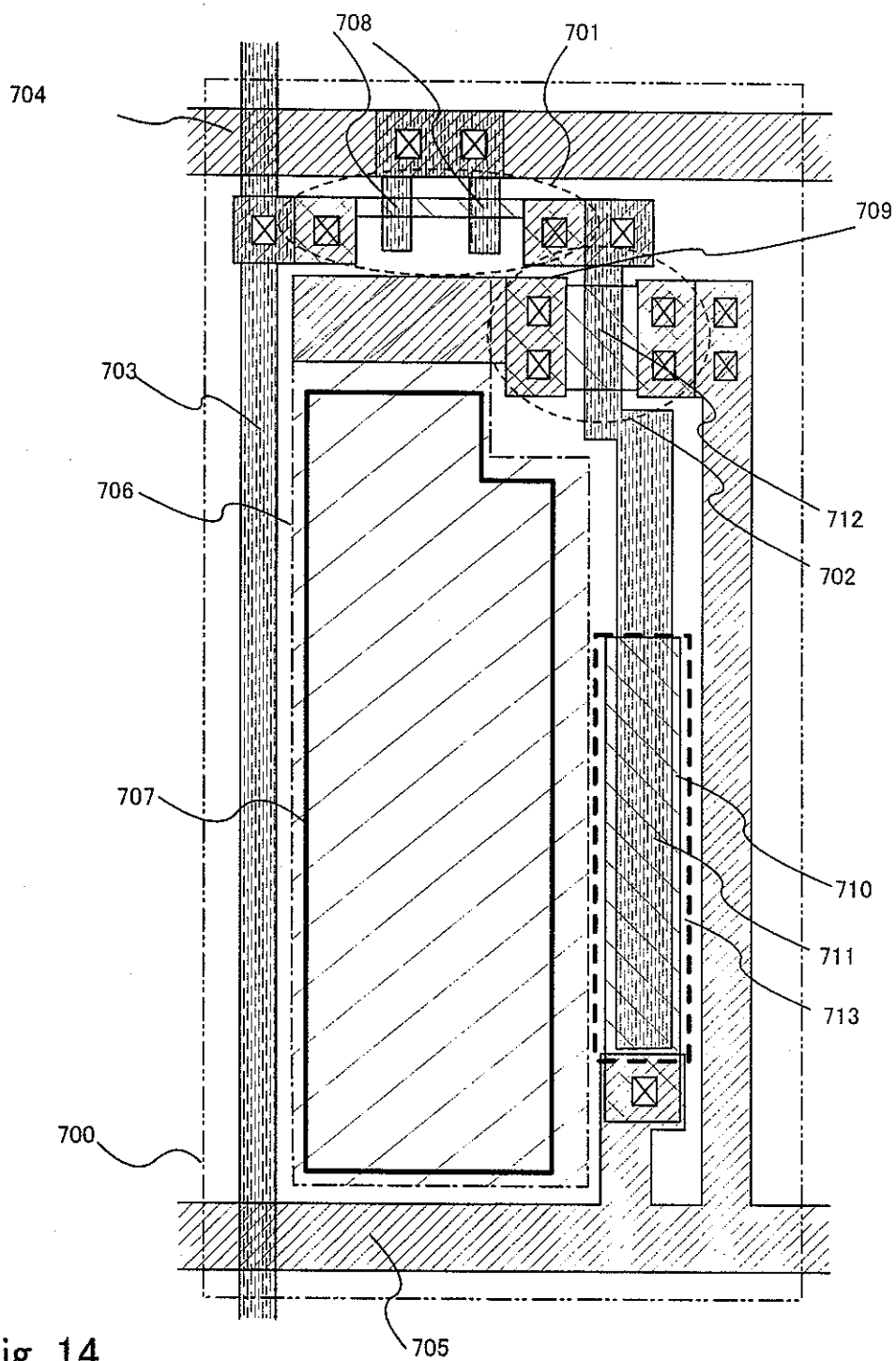
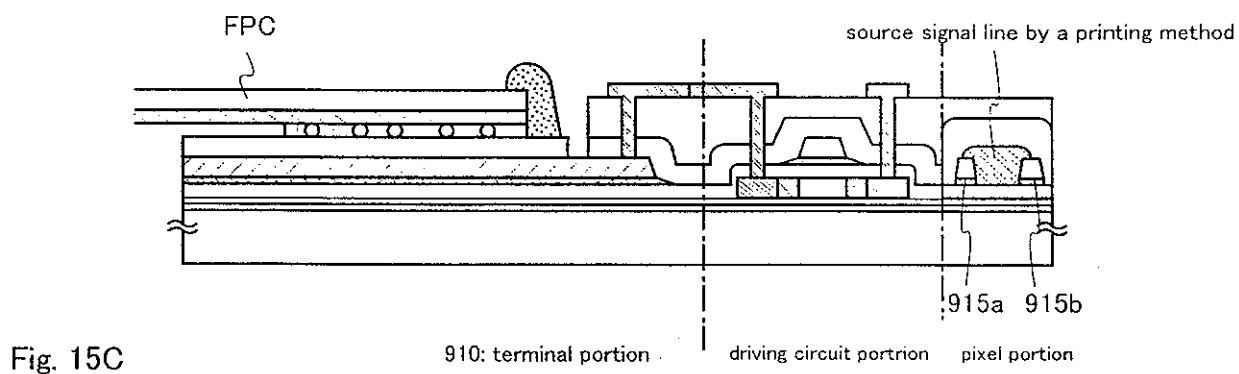
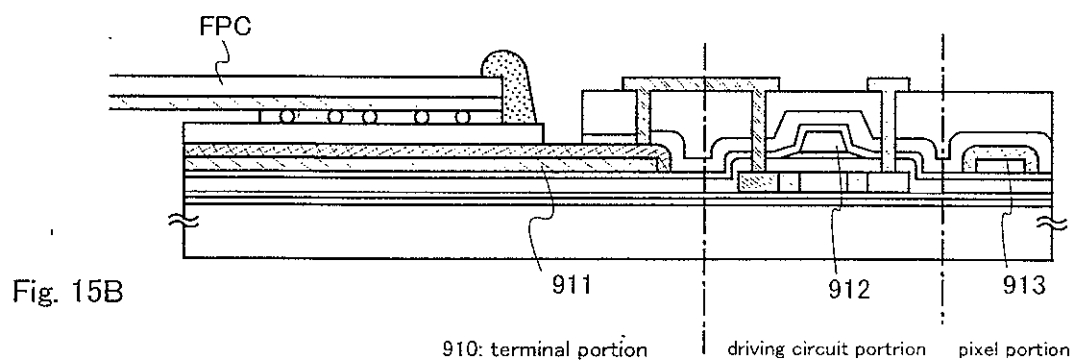
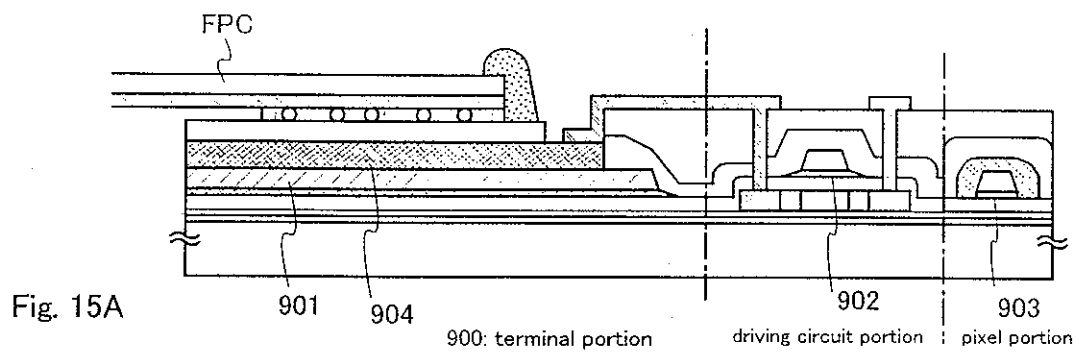


Fig. 14

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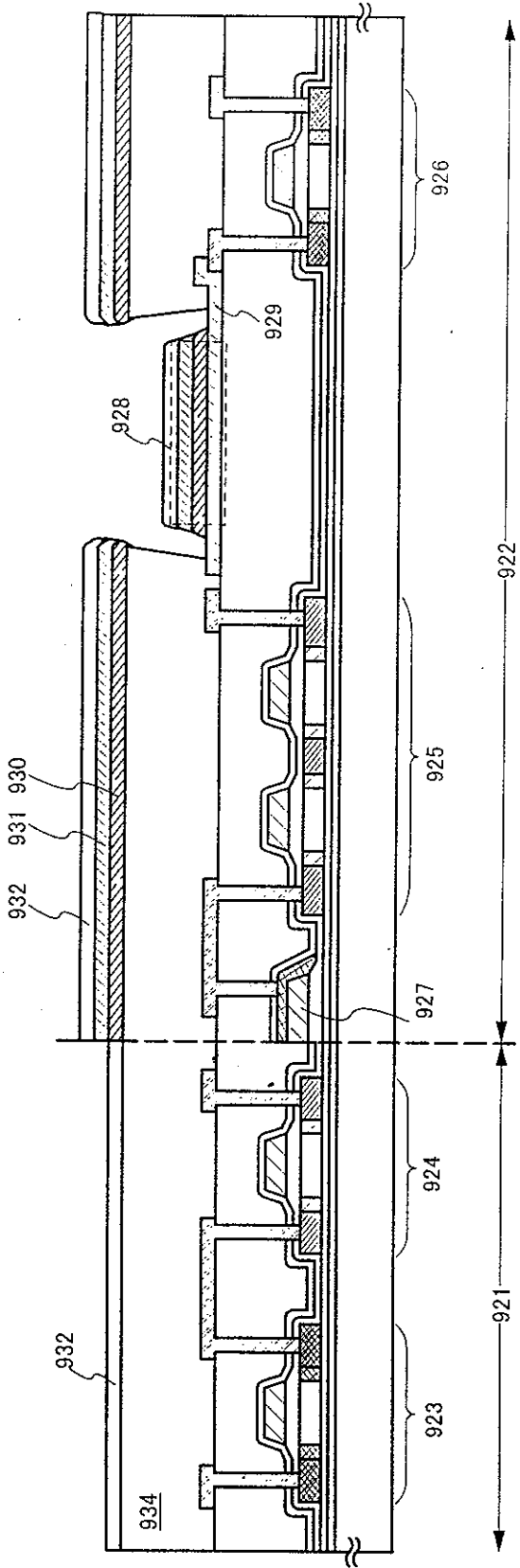


Fig. 16

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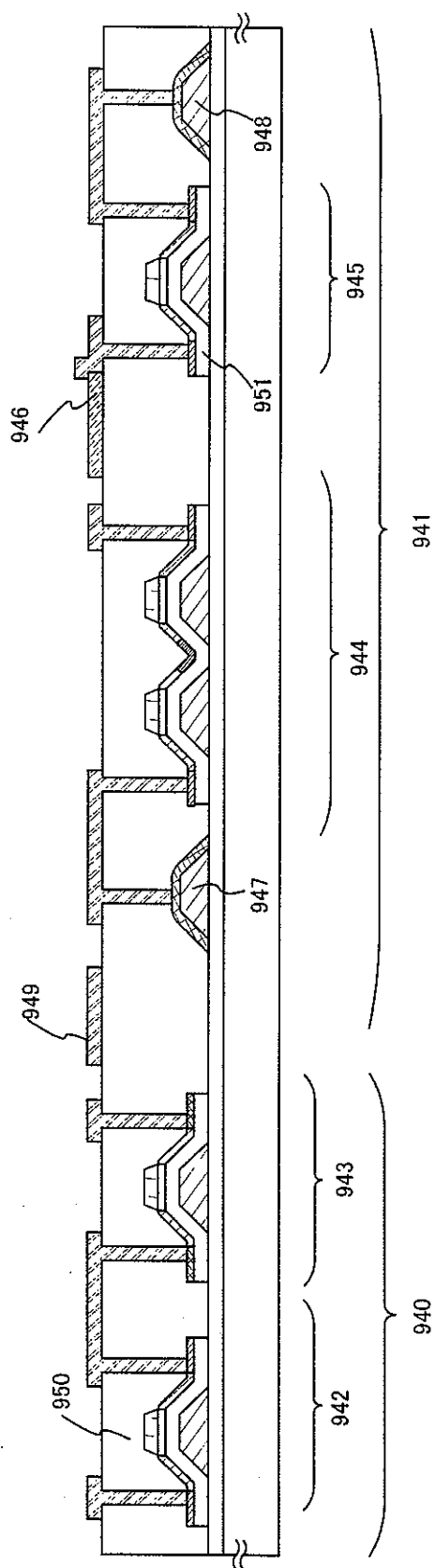


Fig. 17

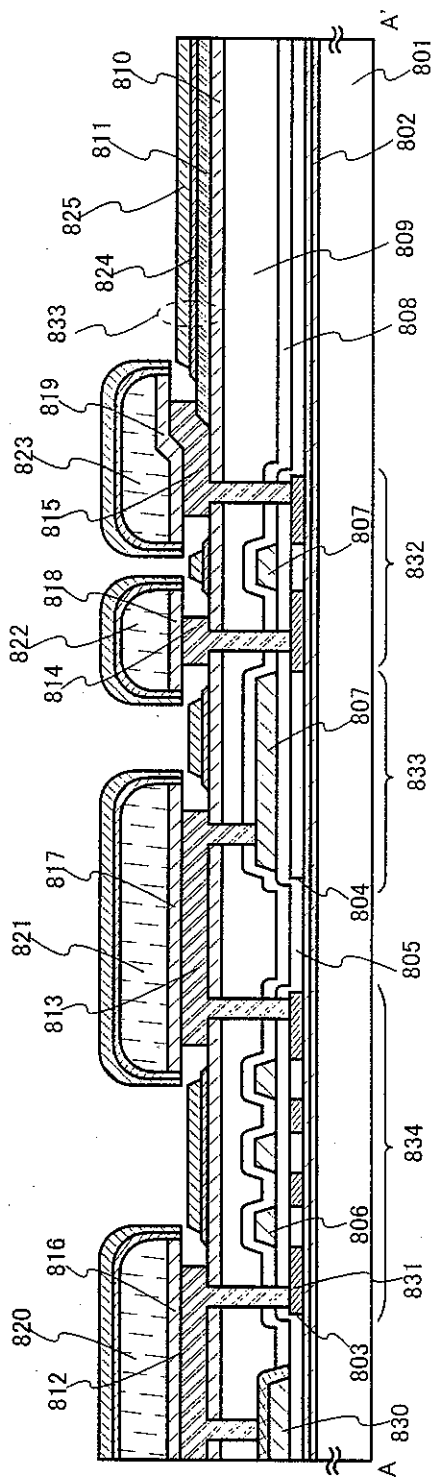


Fig. 18

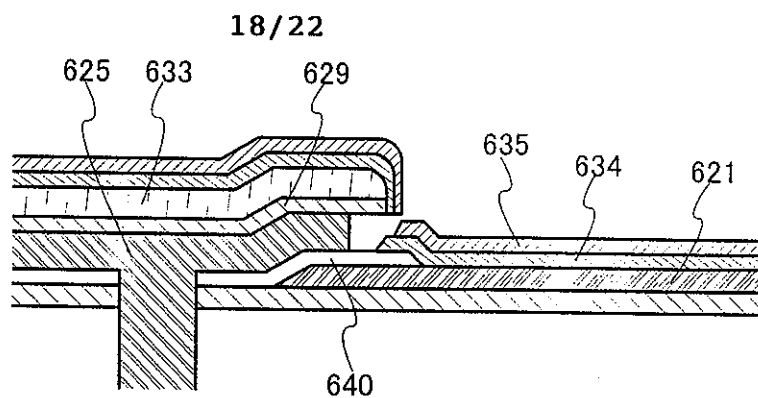


Fig. 19

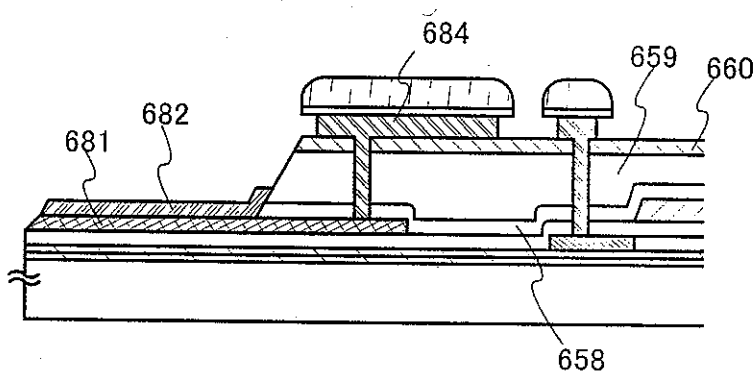


Fig. 20A

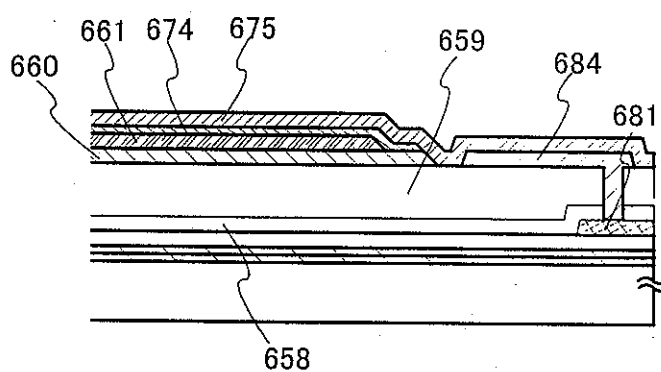


Fig. 20B

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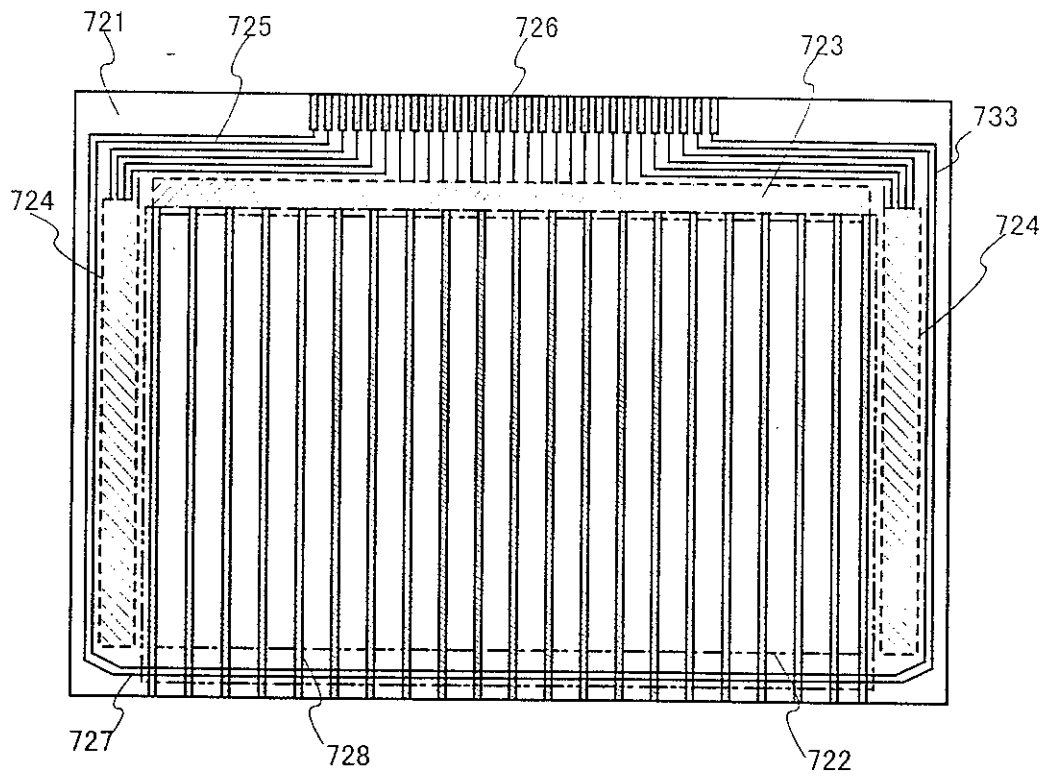


Fig. 21

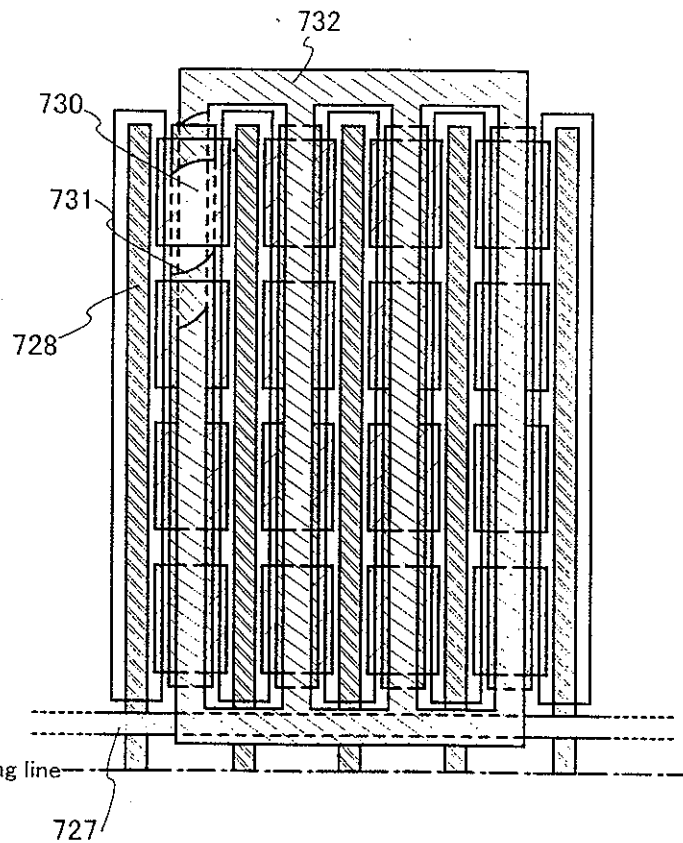


Fig. 22

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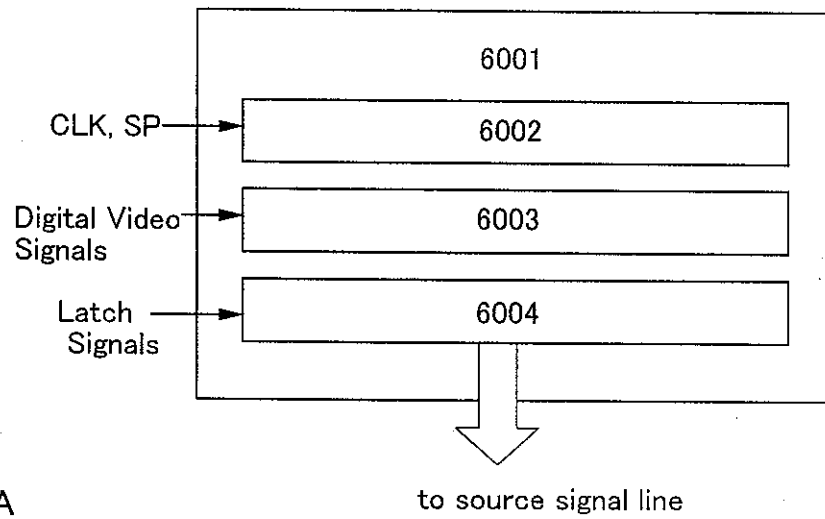


Fig. 23A

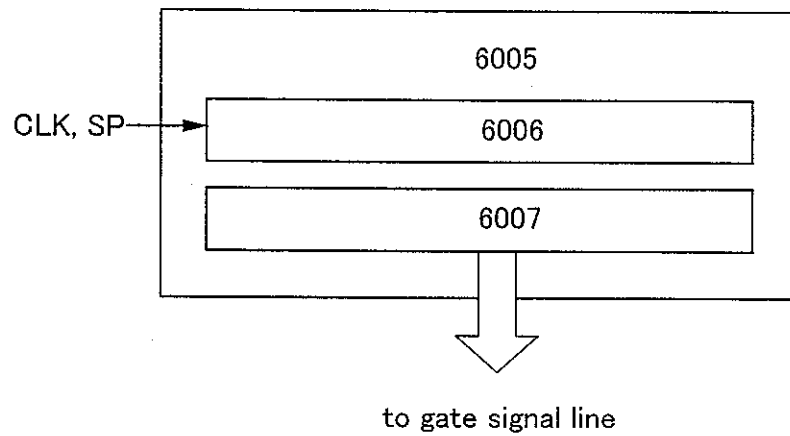


Fig. 23B

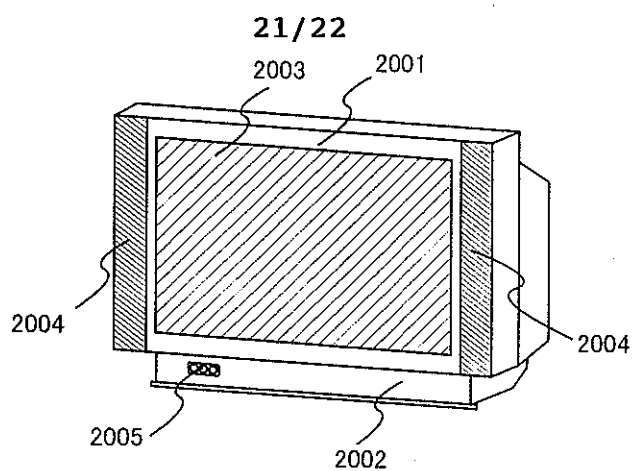


Fig. 24A

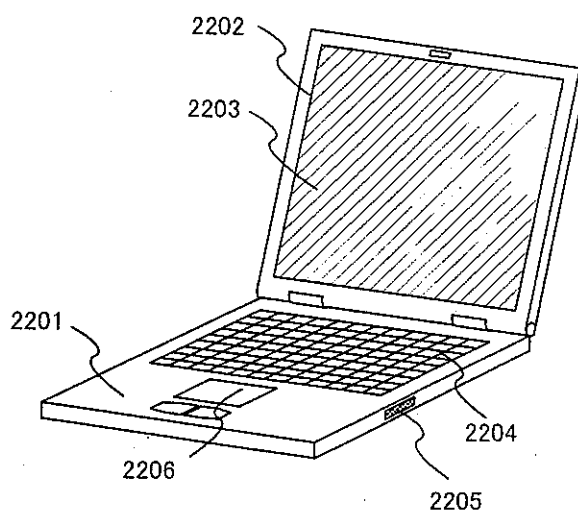


Fig. 24B

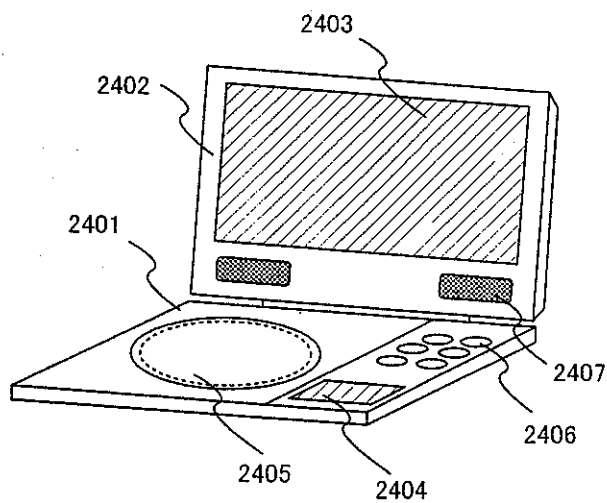


Fig. 24C

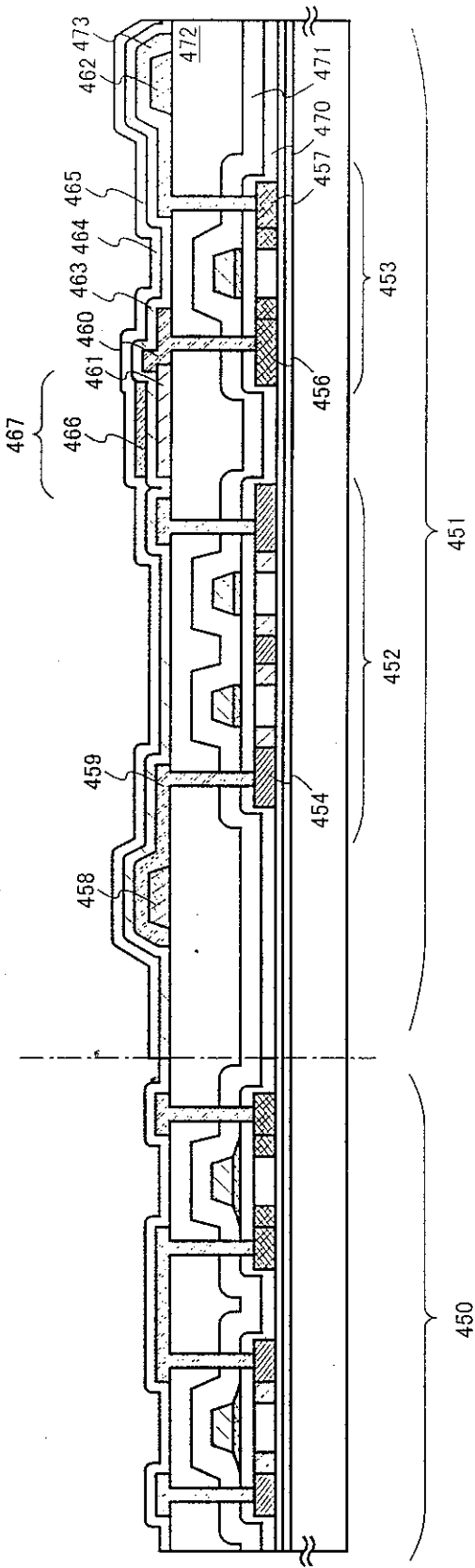


Fig. 25