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TITLE: POLY-ALUMINUM EXCHANGE FOR ALUMINUM FILL OF HIGH ASPECT RATIO SHAPES

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

The present invention relates generally to the manufacture of integrated circuit (IC) chips and, more specifically, the present invention relates to a method of filling high aspect ratio grooves with a conductive material to form sub-lithographic lines and other interconnect metallurgy.

2. BACKGROUND ART

In the present era of very large scale integration and ultra large scale integration, new techniques are continuously being developed to more efficiently utilize the space within semiconductor devices while maintaining or improving present production efficiency.

As IC dimensions continue to shrink, many techniques have been developed to create features that are as small as possible. To this end, advances have been made in the printing process, for example, reduction in the wavelength of light used for the exposure energy and new tools being developed, overlay techniques such as dual damascene, to reduce the criticality of the feature size and alignment problems, and planarization of the surfaces prior to printing to increase yield. However, these methods are

reaching their limits. Therefore, alternative cell types and layouts are being explored.

With the tendency towards higher densities in semi-conductor devices, it is difficult to reduce the vertical geometric size in the same ratio as that of the horizontal direction, therefore, there is a large increase of the aspect ratio. The high aspect ratio causes shadowing effects of the step, therefore, it is difficult to achieve a complete fill of the contact hole with many materials. As shown in FIG. 1, a metal fill of a contact hole in a dielectric layer 12 to a substrate 10 typically results in a void 18 in the metal layer 16. Because of this problem it has been difficult to reduce the pitch of the interconnect wiring in the various metal layers, thereby making it impossible to further scale the design layout. Methods have been suggested for the implementation of high aspect ratio line fills, such as that disclosed in U.S. Patent No. 5,318,923, issued June 7, 1994 to Park and assigned to Samsung Electronics Co. Ltd., however, these methods do not necessarily fill these high aspect ratio holes reliably and completely. Thus, there is a need to provide interconnect wiring in high aspect ratio slots in order to decrease the pitch without adding costly processing steps.

In order to fill high aspect ratio slots, it is known that certain materials and methods may be utilized. For example, chemical vapor deposition (CVD) of polysilicon (polySi) is a well established process that completely fills aspect ratios in excess

of 100:1 in trench dynamic random access memory (DRAM) technology.

Additionally, it is a well known phenomenon that whenever aluminum and silicon are in contact and are subjected to even moderate anneal temperatures, the aluminum will diffuse into the silicon crystal structure and some silicon may migrate into the aluminum. This phenomenon has been taken advantage of in using aluminum as the dopant to form P-type diffusions, as shown in U.S. Patent No. 4,199,386, issued Apr. 22, 1980 to Rosnowski et al., and assigned to RCA Corp; U.S. Patent No. 4,050,967, issued Sept. 27, 1977 to Rosnowski et al. and assigned to RCA Corp.; and U.S. Patent No. 4,154,632, issued May 15, 1979 to Mochizuki et al. and assigned to Hitachi, Ltd. However, it has been more of a problem than a benefit in the semiconductor interconnect metallurgy, as shown in U.S. Patent No. 3,382,568, issued May 14, 1963, to Kulper, and assigned to International Business Machines Corporation. All of the patents cited herein are hereby incorporated by this reference.

Thus, there exists a need to create high aspect ratio interconnect metallurgy, easily and quickly with known processes, not requiring any additional tool development to implement.

SUMMARY OF THE INVENTION

The present invention provides a method for filling high aspect ratio slots to form interconnect metallurgy. The process

basically comprises the steps of: providing a substrate having a surface; (b) forming a recess in the surface of the substrate; (c) depositing a material having good high aspect ratio filling characteristics in the recess; (d) depositing a conductor that is highly soluble in the material on the substrate; and (e) annealing the substrate to cause the conductor to dissolve into the material. In this manner, an extremely small shape of conducting material running where a normal active and passing wordline would otherwise go, thereby reducing design constraints, may be created.

It is an advantage of the present invention that sub-lithographic lines may be created with existing technologies and tools, in an efficient manner.

Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention, the drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For an understanding of the nature and advantages of the present invention, reference should be made to the following detailed description taken in connection with the accompanying drawings wherein:

FIG. 1 is a cross-sectional schematic of a high aspect ratio feature in interconnect metallurgy resulting from the prior art method of filling high aspect ratio features;

FIG. 2 is a cross-sectional schematic of a first step in the method of the present invention;

FIG. 3 is a cross-sectional schematic of a second step in the method of the present invention; and

FIG. 4 is a cross-sectional schematic of a third step in the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While this invention is susceptible to embodiment in many different forms, there is shown in the drawings and will be described in detail, a preferred embodiment of the invention. It should be understood, however, that the present disclosure is to be considered as an exemplification of the principles of this invention and is not intended to limit the invention to the embodiment illustrated.

As shown in FIG. 2, a substrate 110 is shown in cross-section having a relatively thick layer of a dielectric material 112 on an upper surface of the substrate. The dielectric is typically an inorganic insulative material such as silicon dioxide or silicon nitride or organic insulator such as polyimide. The layer of dielectric material 112 also includes a groove, slot, trench or other high aspect ratio feature 114. The slot 114 is formed by any one of the methods that are well known in the art, typically photolithography image and RIE etch. The slot is filled with a material, which fills high aspect ratio trenches without void formation, and which is readily annealed

with a conductor, preferably polysilicon. The polysilicon 116 is typically chemical vapor deposited (CVD) to fill the slot and will also tend to coat the surface of the dielectric layer 112, typically a silicon oxide or nitride. In order to form a planar surface, the polysilicon is removed, preferably by polishing, specifically by a chemical mechanical polish (CMP) process so that the upper surface of the polysilicon in the groove 114 is planar with the surface of the dielectric layer 112.

Next, sputter cleaning or an argon plasma etch is used to assure the surface is free of contaminants and to clean the surface by removing the native oxide from the polysilicon surface, thereby allowing for good contact. As shown in FIG. 3, a layer of aluminum metal 120 is then deposited onto the planarized surface. The aluminum metal is <u>in situ</u> sputter deposited in an aluminum deposition tool. The entire structure is then annealed in either a vertical or horizontal tube furnace in an anneal ambient of flowing nitrogen by heating to a temperature in excess of about 500°C. The preferred temperatures were in the range of about 525°C to about 575°C. The structure is subjected to the anneal for approximately 60 minutes, however the amount of time may vary depending on the temperature and the materials chosen.

As shown in FIG. 4, the excess aluminum that remains on the surface after the anneal step is removed preferably by CMP polishing back to the previously planarized surface. In this manner, a sub-lithographic line 130 is formed, embedded in the

layer of dielectric material 112. It is estimated that the silicon-aluminum alloy in the groove would have a conductivity that is reduced by about 30% as compared to pure aluminum fill.

While the invention has been particularly shown and described with reference to preferred exemplary embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

CLAIMS

Accordingly, what is claimed is:

1. A method for forming interconnect metallurgy for semiconductors comprising the steps of:

(a) providing a substrate having a surface;

(b) forming a recess in the surface of the substrate;

(c) depositing a material in the recess;

(d) depositing a conductor that is highly exchangeable in the material on the material; and

(e) annealing the substrate to cause the conductor to be exchanged into the material.

2. The method of claim 1, further comprising the step, between step (c) and step (d), of: removing the material back to form a planar surface with the substrate.

3. The method of claim 2, wherein the removal is by chemically-mechanically polishing.

4. The method of claim 1, further comprising the step of, between step (c) and step (d): sputter cleaning the surface of the substrate and the material.

5. The method of claim 4, wherein the material to be deposited in the recess is a material which fills high aspect ratio features and in which the conductor will exchange.

6. The method of claim 5, wherein the material is polysilicon.

7. The method of claim 2, wherein the conductor is aluminum.

8. The method of claim 1, further comprising the step, after step (e) of:

(f) planarizing the substrate surface and a surface of the groove.

9. The method of claim 4, wherein the sputter cleaning is an argon plasma etch process.

10. The method of claim 1, wherein the deposition of the conductor is an in situ sputter of aluminum.

11. The method of claim 1, wherein the anneal step (e) is conducted in a vertical tube furnace at a temperature in the range of about 525°C to about 575°C for approximately 60 minutes.

12. The method of claim 1, wherein the anneal step (e) is conducted in a horizontal tube furnace at a temperature in the range of about 525°C to about 575°C for approximately 60 minutes.

13. The method of claim 1, wherein the substrate is a dielectric layer on a surface of a wafer.

14. A method for forming a conductive, sub-lithographic line comprising the steps of:

(a) providing a substrate having a high aspect ratio recess therein;

(b) depositing a material which fills high aspect ratio features without void formation;

(c) planarizing the material back to the substrate;

(d) cleaning the material;

(e) depositing a conductor that is highly exchangeable into the material on the material and the substrate; and

(f) annealing the substrate to cause the conductor to be exchanged into the material.

15. The method of claim 14, further comprising the step, after step (f), of:

chemically-mechanically polishing the conductor back to the substrate.

16. The method of claim 14, wherein the deposition of the conductor is an <u>in situ</u> sputter of aluminum.

17. The method of claim 14, wherein the conductor is aluminum and wherein the material which fills high aspect ratio areas without void formation is polysilicon.

18. The method of claim 14, wherein the substrate is a dielectric material on the surface of a wafer.

19. A method for filling a high aspect ratio shape with a conductive material comprising the steps of:

(a) providing a substrate;

(b) depositing a layer of dielectric material on a surface of the substrate;

(c) forming a high aspect ratio recess through the layer of dielectric material;

(d) depositing a layer of polysilicon on a surface of the dielectric layer and in the recess;

(e) polishing the layer of polysilicon back to the surface of the dielectric layer;

(f) sputter cleaning the layer of polysilicon, thereby forming a clean polysilicon surface;

(g) depositing a layer of aluminum on the surface of the dielectric layer and the clean polysilicon surface;

(h) annealing the substrate in a furnace to cause the aluminum to dissolve into the polysilicon; and

(i) chemically-mechanically polishing the layer of aluminum back to the surface of the dielectric layer.

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ABSTRACT

A method for forming interconnect metallurgy for semi-conductors comprising the steps of: (a) providing a substrate (110) having a surface; (b) forming a recess (114) in the surface of the substrate; (c) depositing a material in the recess (116); (d) depositing a conductor (120) that is highly soluble in the material on the substrate; and (e) annealing the substrate to cause the conductor to exchange into the material is disclosed. The method takes advantage of the high aspect ratio filling properties of polysilicon as known for deep trench applications and combines that with known processes for forming silicon-aluminum alloys to form a wordline spacer structure in order to decrease the amount of space necessary for a unit cell.

Fig. 2

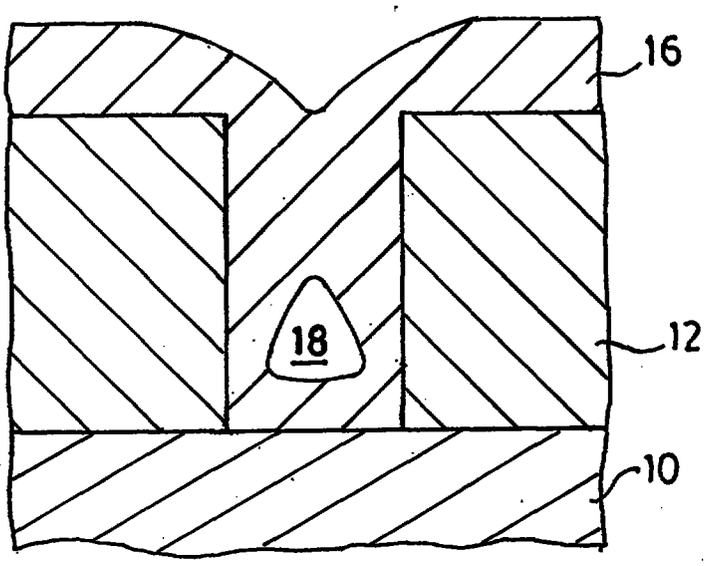


FIG. 1
PRIOR ART

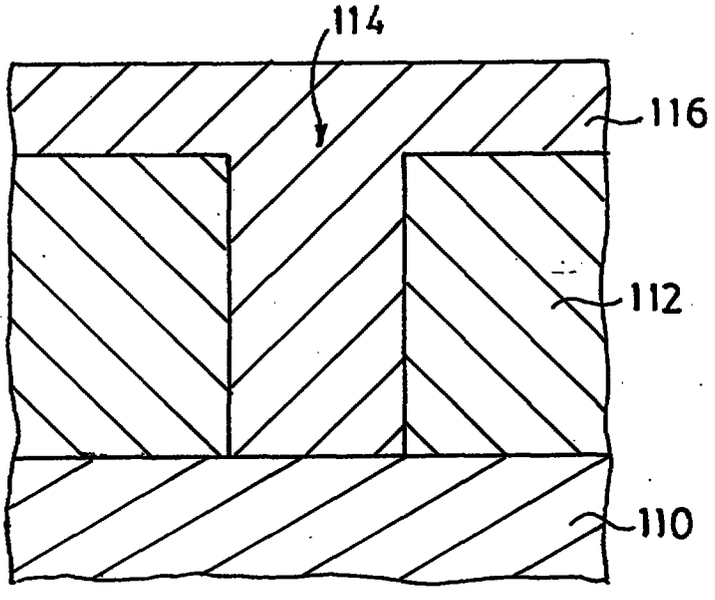


FIG. 2

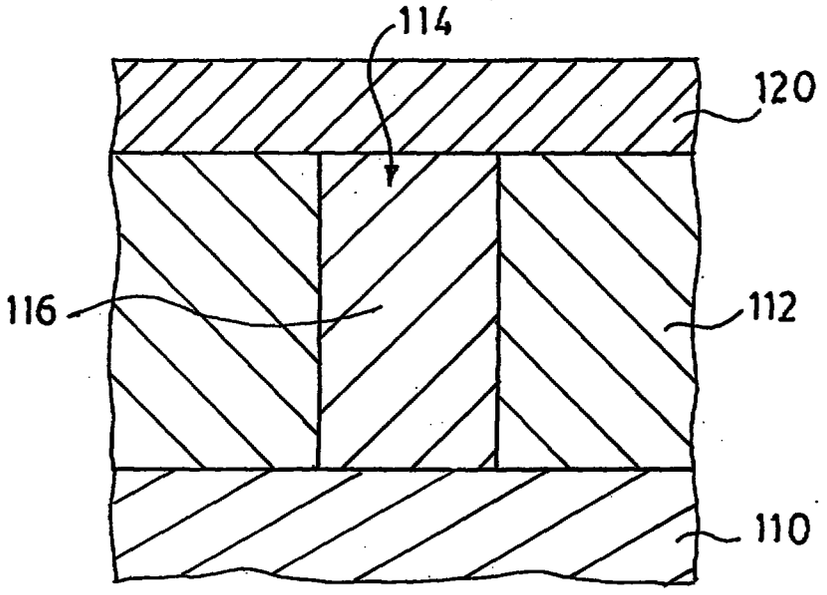


FIG. 3

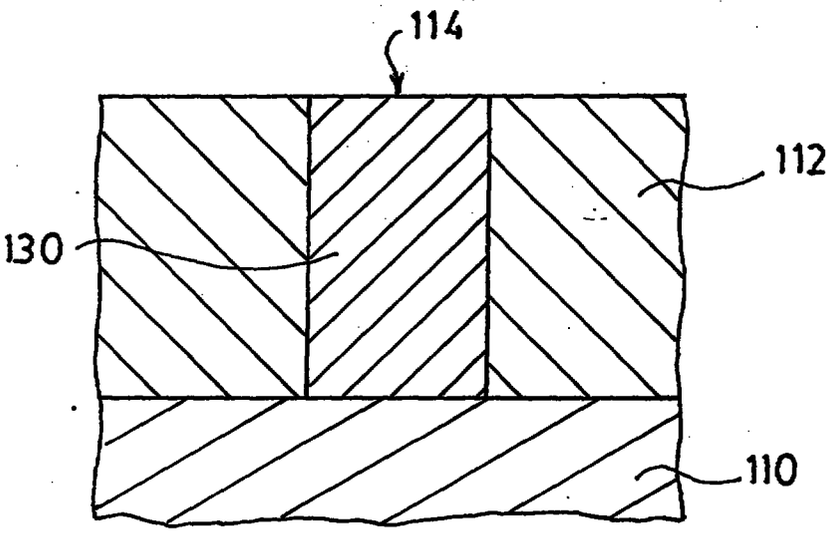


FIG. 4