CLAIMS

1. Hybrid processor system (1) for use on board a telecommunications multi-beam satellite, wherein said telecommunications multi-beam satellite is controllable by a network control centre via one or more control channels, and is designed to link ground terminals by:

providing uplink and downlink traffic channels on several satellite beams;

routing atomic switched information blocks from the uplink traffic channels to the downlink traffic channels; and

exchanging signaling data with the ground terminals on one or more uplink signaling channels and one or more downlink signaling channels;

wherein all the atomic switched information blocks have one and the same given time duration and one and the same given baseband bandwidth;

wherein each uplink traffic channel has a respective uplink bandwidth including respective uplink frequencies, and carries, at said respective uplink frequencies, respective atomic switched information blocks in respective uplink time slots organized into respective uplink time frames forming respective uplink time superframes;

wherein each downlink traffic channel has a respective downlink bandwidth including respective downlink frequencies, and carries, at said respective downlink frequencies, respective atomic switched information blocks in respective downlink time slots organized into respective downlink time frames forming respective downlink time superframes;

wherein said hybrid processor system (1) comprises:

a burst switching processor (11); and

an on-board processor controller (12);

wherein said on-board processor controller (12) is configured to:

store service information items indicative of

said given time duration and said given baseband bandwidth of the atomic switched information blocks,

the respective uplink bandwidth, the respective uplink frequencies, a respective time length of the respective uplink time slots, and respective structure features of the respective uplink time frames and superframes of each uplink channel,

the respective downlink bandwidth, the respective downlink frequencies, a respective time length of the respective downlink time slots, and respective structure features of the respective downlink time frames and superframes of each downlink channel, and

quality of service and priority rules for serving the ground terminals;

extract, from incoming signaling data received on the uplink signaling channel(s), capacity requests sent by the ground terminals, wherein the capacity requests are extracted by the on-board processor controller (12) by demodulating and decoding the incoming signaling data;

assign to each pair or set of ground terminals to be linked respective frequency, space and time resources on the basis of the stored service information items and of all the capacity requests received from the ground terminals, wherein said respective frequency, space and time resources includes

one or more respective uplink frequencies of one or more respective uplink channels provided on one or more respective satellite beams,

one or more respective uplink time slots in one or more respective uplink time frames in one or more uplink time superframes of said one or

more respective uplink channels,

one or more respective downlink frequencies of one or more respective downlink channels provided on said one or more respective satellite beams, and

one or more respective downlink time slots in one or more respective downlink time frames in one or more downlink time superframes of said one or more respective downlink channels;

generate resource assignment messages indicative of the frequency and time resources assigned to the ground terminals;

generate outgoing signaling data to be transmitted to the ground terminals on the downlink signaling channel(s), wherein the outgoing signaling data are generated by the on-board processor controller (12) by encoding and modulating the resource assignment messages;

generate a routing map on the basis of the frequency, space and time resources assigned to the ground terminals;

generate switching commands based on the routing map;

extract, from control data received on the control channel(s), control messages sent by the network control centre, wherein the control messages are extracted by the on-board processor controller (12) by demodulating, decoding and decrypting the control data; and

update the stored service information items on the basis of the control messages;

wherein the burst switching processor (11) is configured to route the atomic switched information blocks on the basis of the switching commands generated by the on-board processor controller (12);

whereby:

the on-board processor controller (12) is configured to operate in a regenerative way with respect to the signaling data, and is reconfigurable by the network control centre;

and

the burst switching processor (11) is configured to operate in a digital transparent way with respect to the atomic switched information blocks, and is operable by the on-board processor controller (12) to route the atomic switched information blocks in frequency, space and time domains.

2. The hybrid processor system of claim 1, wherein the burst switching processor (11) comprises a five-stage Clos switching network (111) including a first three-stage Clos network (111a) and, in cascade, a second three-stage Clos network (111b) designed for, respectively, copy and unicast functions;

wherein said five-stage Clos switching network (111) includes an inner intermediate stage shared by said first (111a) and second (111b) three-stage Clos networks;

and wherein the on-board processor controller (12) is configured to generate the switching commands by implementing a self-routing algorithm (8) including:

generating, on the basis of the routing map, a matrix representing the five-stage Clos switching network (111); and

processing said matrix so as to produce a non-blocking routing configuration for said five-stage Clos switching network (111).

3. The hybrid processor system of claim 2, wherein the five-stage Clos switching network (111) has a TSTST architecture, and wherein the on-board processor controller (12) is configured to implement the self-routing algorithm (8) to manage the inner intermediate T stage and the last S and T stages of said five-stage Clos switching network (111).

4. The hybrid processor system according to claim 2, wherein the on-board processor controller (12) is configured to generate the switching commands by

implementing also a rank-based algorithm, an interval splitting algorithm and a looping algorithm.

5. The hybrid processor system according to claim 1, wherein the burst switching processor (11) comprises a channelization analysis section (113) configured to perform fractional rate decimation and a channelization synthesis section (114) configured to perform fractional rate interpolation.

6. The hybrid processor system of claim 5, wherein the burst switching processor (11) further comprises input signal conditioning means (112) configured to apply an analog-to-digital conversion to incoming analog traffic signals received on the uplink traffic channels, thereby producing incoming digital traffic signals;

wherein the channelization analysis section (113) is connected to the input signal conditioning means (112) to apply the fractional rate decimation to the incoming digital traffic signals, thereby producing incoming atomic switched information blocks;

wherein the burst switching processor (11) further comprises a five-stage Clos switching network (111), that is connected between the channelization analysis section (113) and the channelization synthesis section (114), and that is configured to carry out a switching of the incoming atomic switched information blocks on the basis of the switching commands generated by the on-board processor controller (12), thereby producing outgoing atomic switched information blocks;

wherein the channelization synthesis section (114) is configured to apply the fractional rate interpolation to the outgoing atomic switched information blocks, thereby producing outgoing digital traffic signals;

and wherein the burst switching processor (11) further comprises output signal conditioning means (115) configured to apply a digital-to-analog conversion (DAC) to the

outgoing digital traffic signals, thereby producing outgoing analog traffic signals to be transmitted on the downlink traffic channels.

7. The hybrid processor system according to claim 1, wherein the on-board processor controller (12) is further configured to:

mark the capacity requests received from the ground terminals by assigning to each capacity request

a respective timestamp on the basis of a respective time of arrival of said capacity request, and

a respective priority level on the basis of the stored service information items indicative of the quality of service and priority rules for serving the ground terminal that has sent said capacity request; and

assign the frequency and time resources to the ground terminals on the basis of the marked capacity requests.

8. The hybrid processor system according to claim 1, wherein the service information items are also indicative of connection features related to the ground terminals.

9. Satellite for telecommunications, that is controllable by a network control centre via one or more control channels and is designed to link ground terminals by:

providing uplink and downlink traffic channels on several satellite beams;

routing atomic switched information blocks from the uplink traffic channels to the downlink traffic channels; and

exchanging signaling data with the ground terminals on one or more uplink signaling channels and one or more downlink signaling channels;

wherein all the atomic switched information blocks have one and the same given time duration and one and the same given baseband bandwidth;

wherein each uplink traffic channel has a respective uplink bandwidth including respective uplink frequencies, and carries, at said respective uplink frequencies, respective atomic switched information blocks in respective uplink time slots organized into respective uplink time frames forming respective uplink time superframes;

wherein each downlink traffic channel has a respective downlink bandwidth including respective downlink frequencies, and carries, at said respective downlink frequencies, respective atomic switched information blocks in respective downlink time slots organized into respective downlink time frames forming respective downlink time superframes;

and wherein said satellite comprises the hybrid processor system (1) as claimed in claim 1.