FIG. 1A

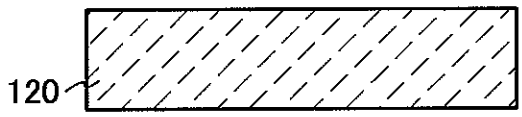


FIG. 1B

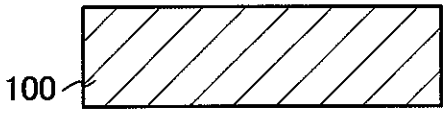


FIG. 1C

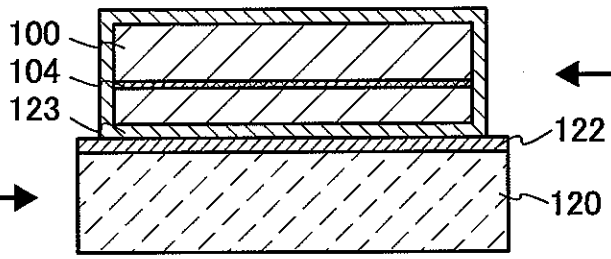


FIG. 1D

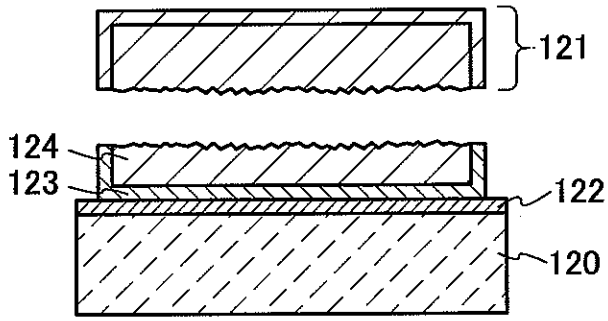


FIG. 1E

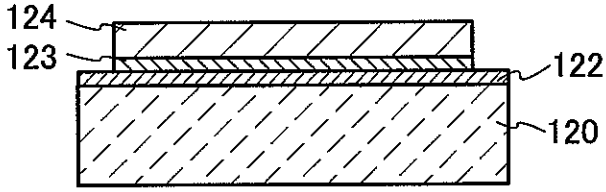


FIG. 2A

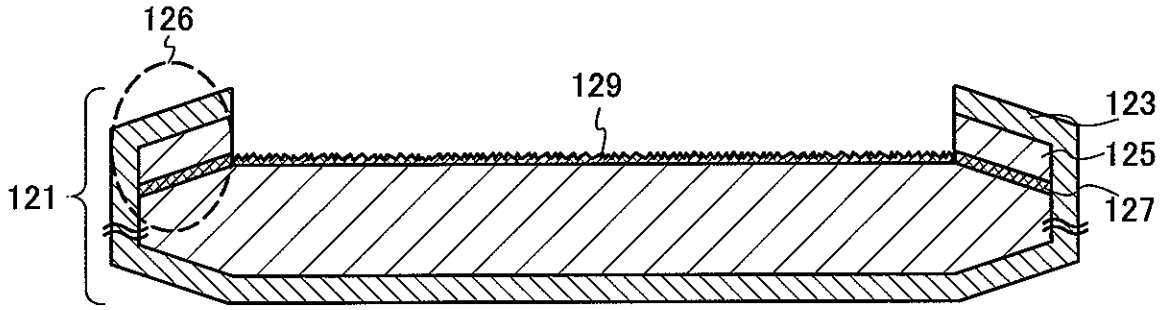


FIG. 2B

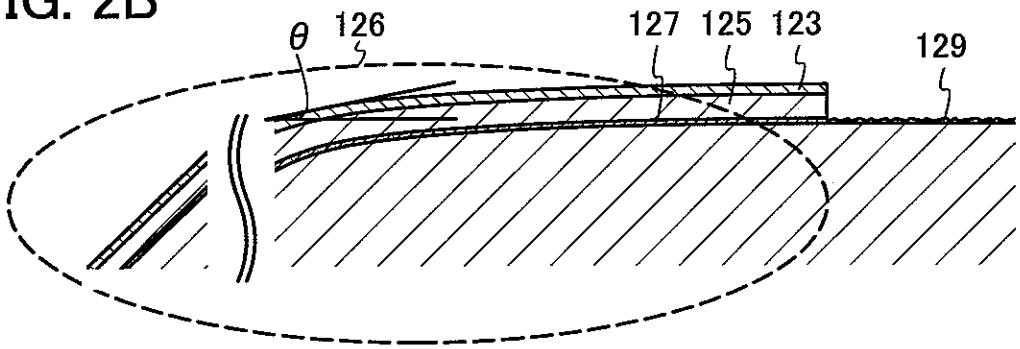


FIG. 2C

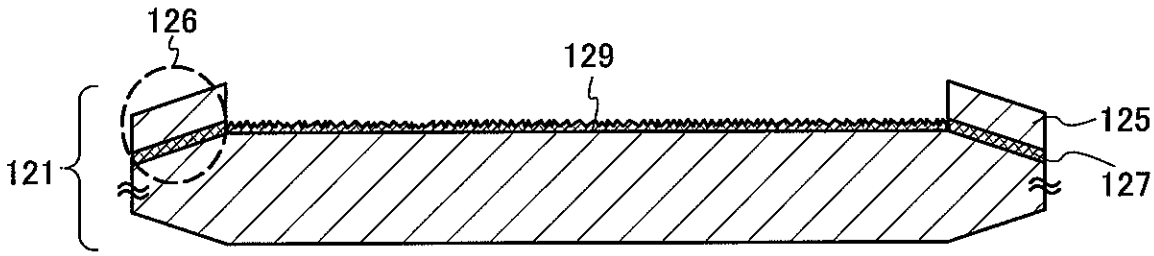


FIG. 2D

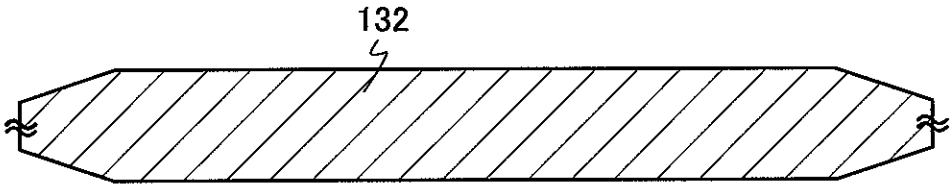


FIG. 3A

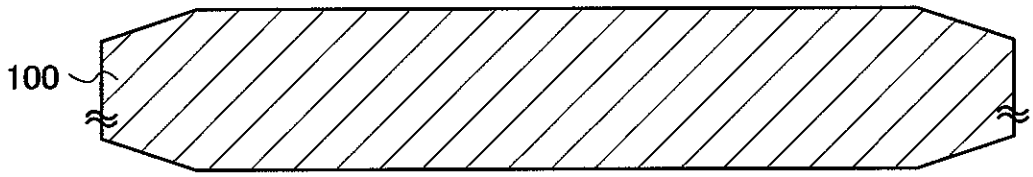


FIG. 3B

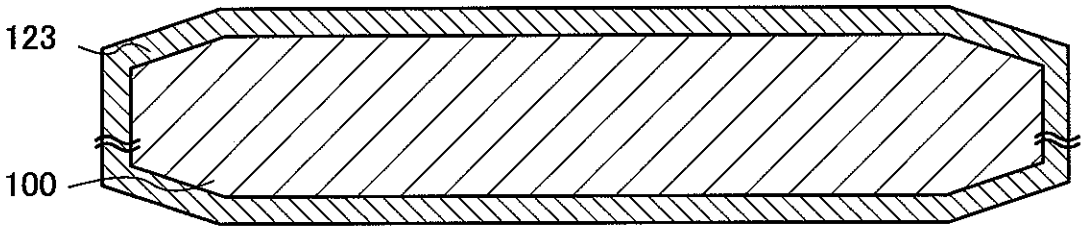


FIG. 3C

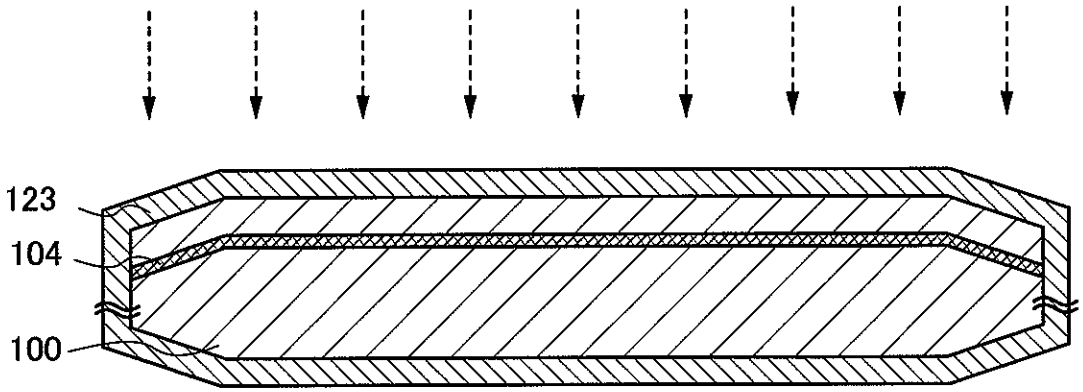


FIG. 4A

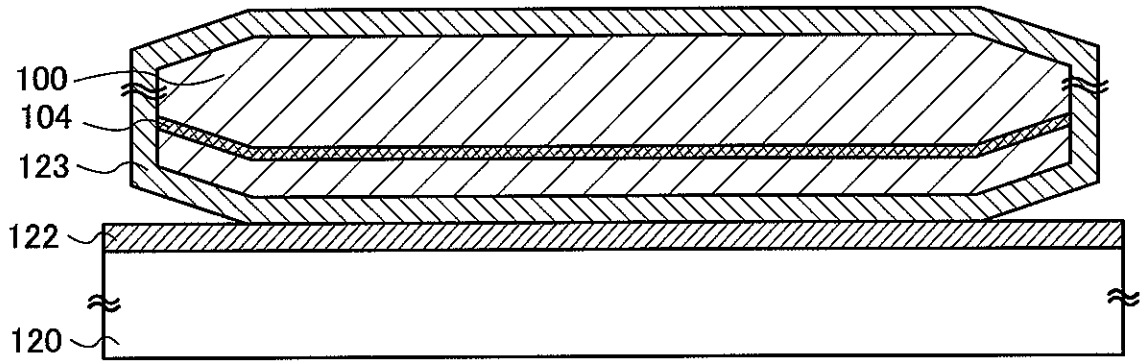


FIG. 4B

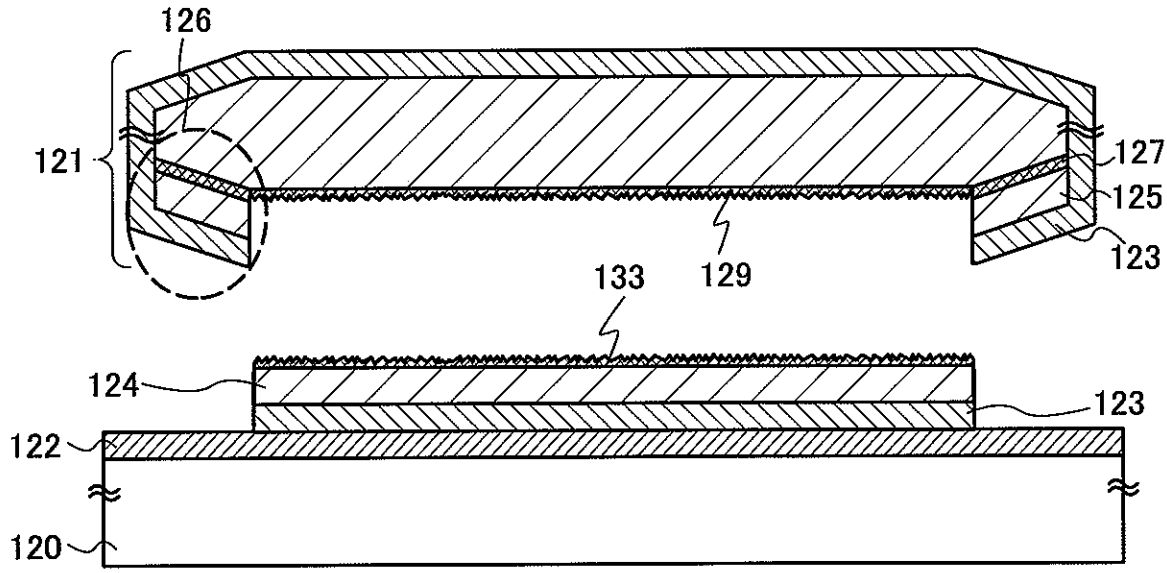


FIG. 4C

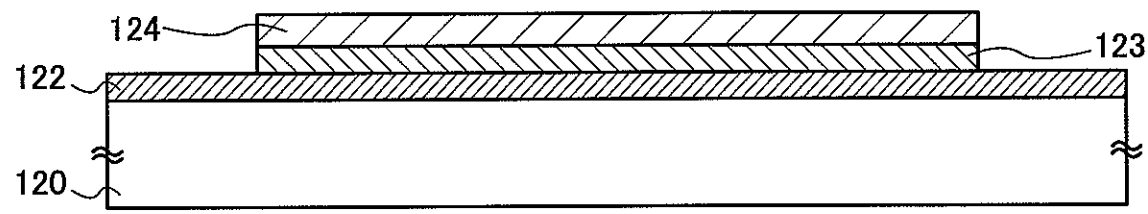


FIG. 5

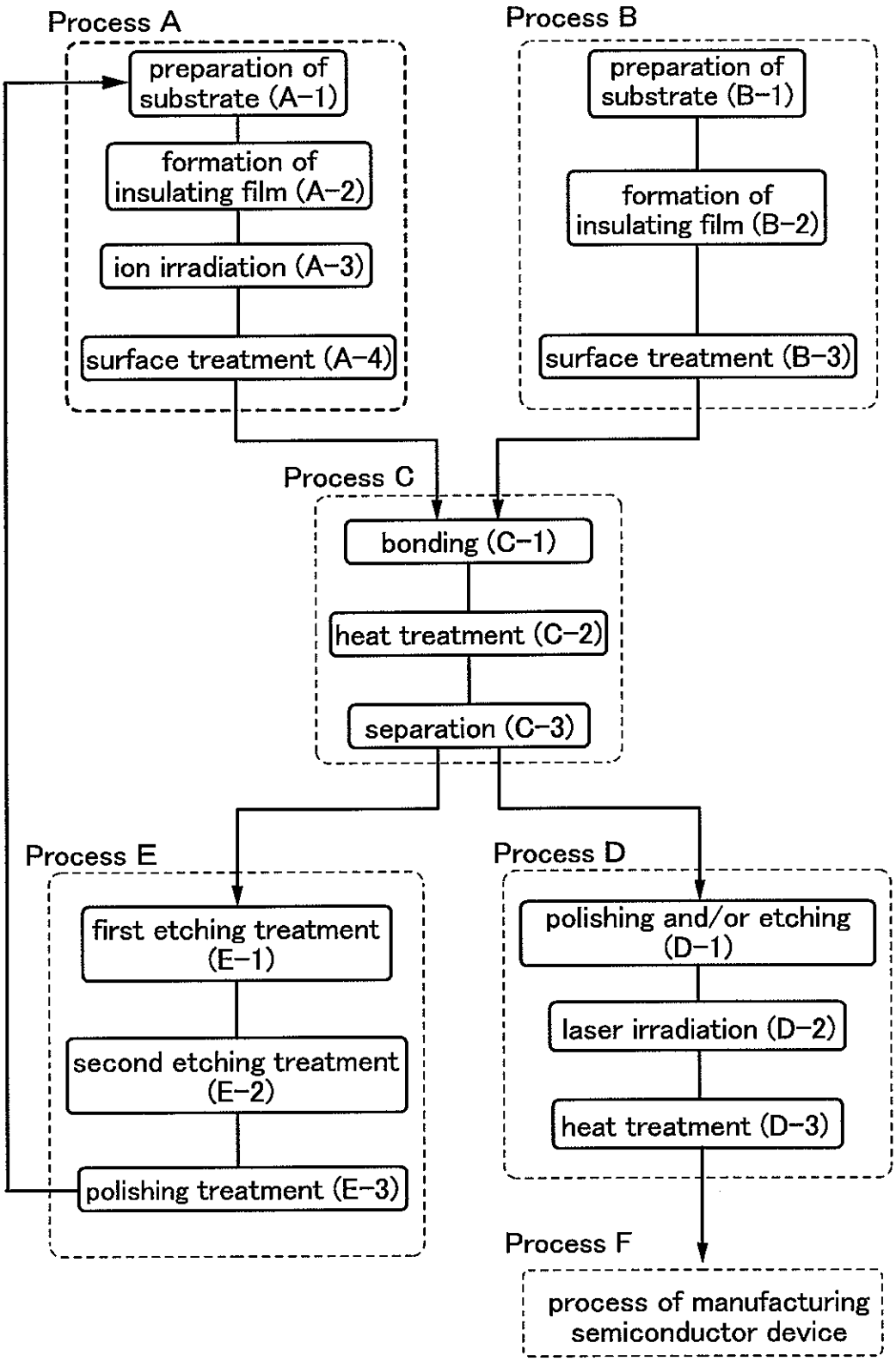

Process A
preparation of substrate (A-1)
formation of insulating film (A-2)
ion irradiation (A-3)
surface treatment (A-4)
Process B
preparation of substrate (B-1)
formation of insulating film (B-2)
surface treatment (B-3)
Process C
bonding (C-1)
heat treatment (C-2)
separation (C-3)
Process E
first etching treatment (E-1)
second etching treatment (E-2)
polishing treatment (E-3)
Process D
polishing and/or etching (D-1)
laser irradiation (D-2)
heat treatment (D-3)
Process F
process of manufacturing semiconductor device

FIG. 6

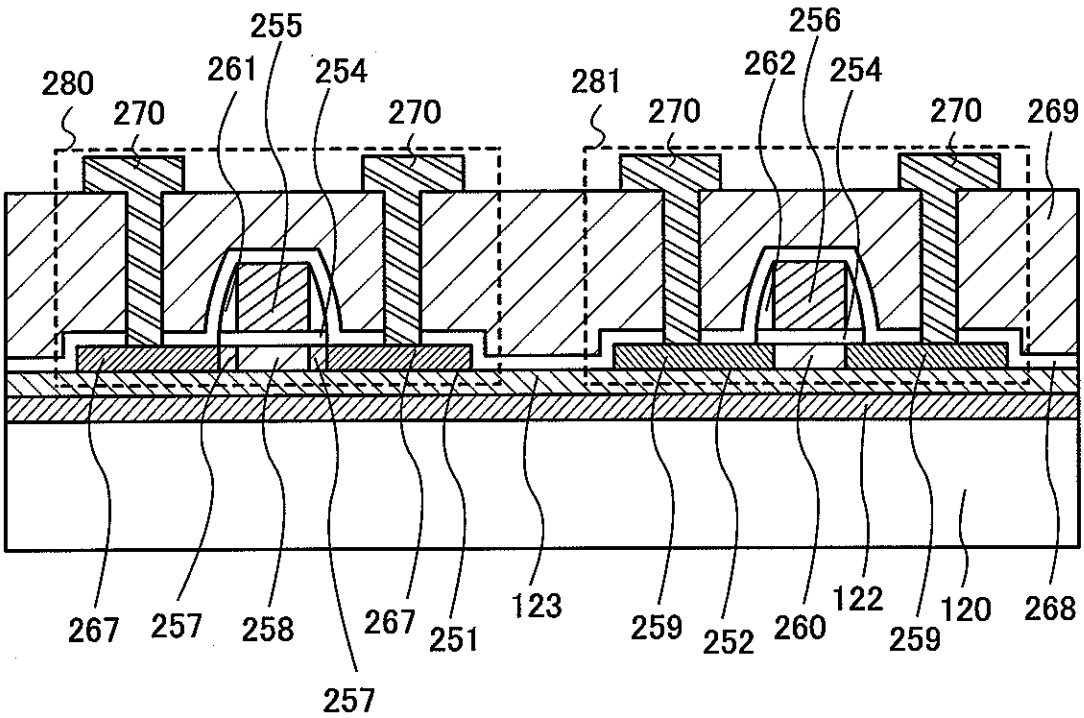

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120
268

FIG. 7A1

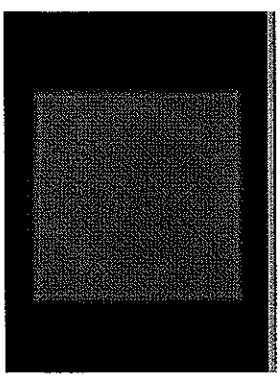


FIG. 7A2

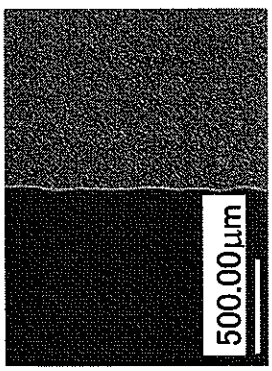


FIG. 7B1

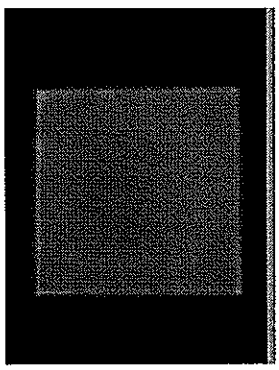


FIG. 7B2

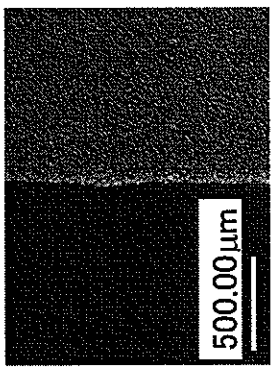


FIG. 7C1

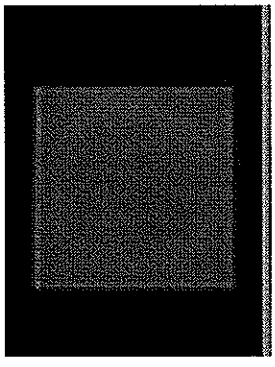


FIG. 7C2

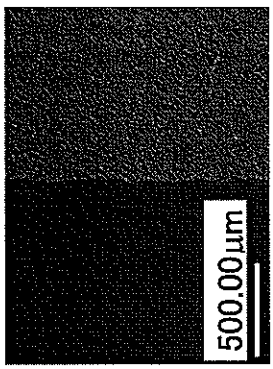


FIG. 7D1

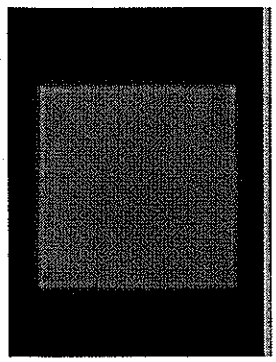


FIG. 7D2

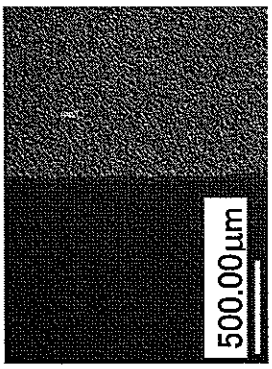


FIG. 7E1

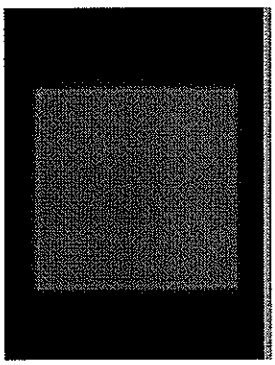


FIG. 7E2

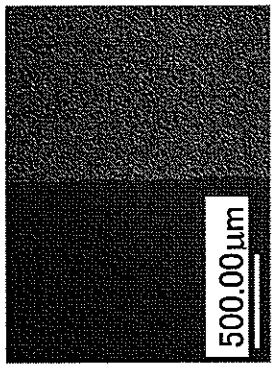


FIG. 8A1

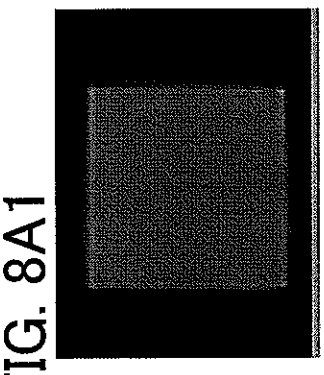


FIG. 8A2

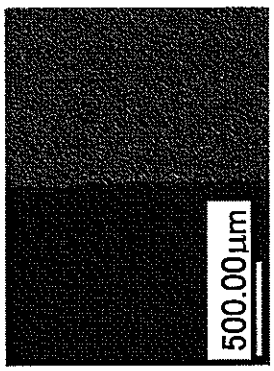


FIG. 8B1

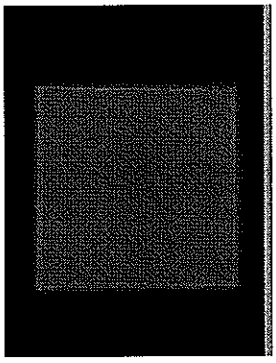


FIG. 8B2

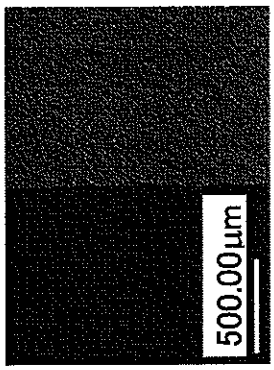


FIG. 8C1

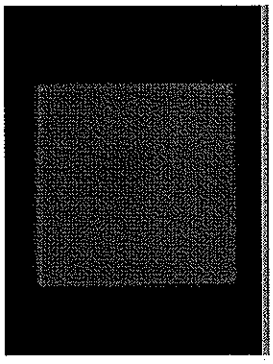


FIG. 8C2

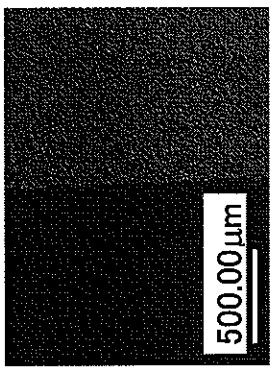


FIG. 8D1

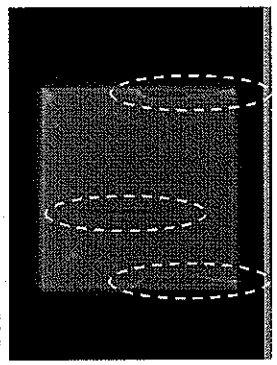


FIG. 8D2

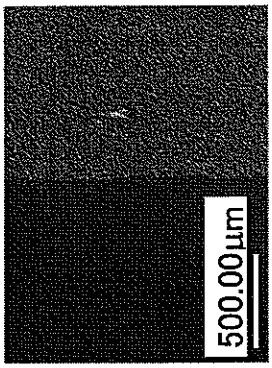


FIG. 8E1

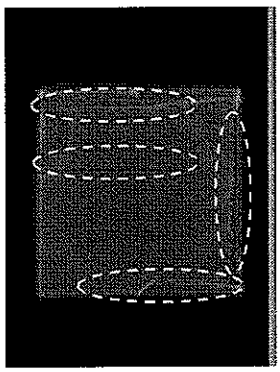


FIG. 8E2

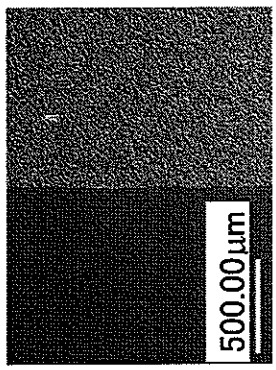
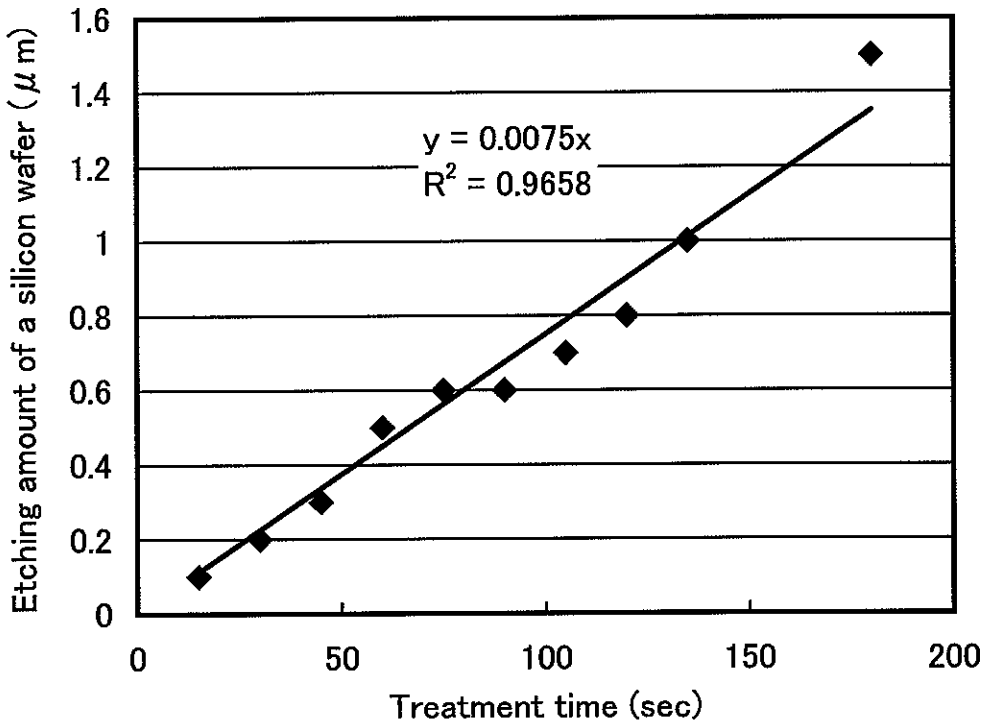


FIG. 9


Etching amount of a silicon wafer (μm)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
y = 0.0075x
R2 = 0.9658
0
50
100
150
200
Treatment time (sec)