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(54) LOGIC SYSTEM

(71) We, TELETYPE CORPORATION, of 5555 Touhy Avenue, Skokie, Cook County, State of Illinois, United States of America, a Corporation organised under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a logic system.

Digital circuitry has played an important role in the growth of electronic industries. As the cost of equipment for performing digital operations is reduced, digital circuits replace more and more analog circuits and find new applications previously not contemplated.

Developments enabling the fabrication of large scale integrated logic circuit arrays have reduced the potential cost of digital equipment. Thousands of devices can be created on a semiconductor substrate which previously was employed for one device. As the size of semiconductor devices is reduced and their packing density is thereby increased, the electrical and thermal parameters which affect the design of such circuitry are altered. For example, as the size of a MOSFET device is reduced, the minimum obtainable source-to-drain impedance is increased. As components are placed more closely together, stray capacity is reduced and average allowable power dissipation for each device is reduced. Further, because of the compact arrangement, bringing excess leads to the circuitry increases the complexity thereof.

New circuit configurations have been developed to take these new parameters into account, providing circuits more suitable for large scale integration. One approach to implementing logical functions in MOSFET integrated circuits involves a logic network including a plurality of FET devices to provide either an open or short circuit depending upon the logical state thereof in series with an FET load device. The series circuit is connected between two reference voltage levels. A gating FET device connects the junction of the logic network and the load FET to drive another logic stage or a load device, either of which may include a capacitor. The gating FET is periodically enabled to transfer the logical level at the junction of the load FET and the logic network to the capacitor.

This configuration suffers from several disadvantages. The source-to-drain impedance of the load FET must bear a known relationship to the impedance of the logic network in its ON and OFF states. This places a constraint on the parameters of the FET devices used therein and lowers the yield, since each device must have parameters within a limited range. Further, when the logic network is in its ON state, current is continuously flowing in the load device and the logic network, therefore dissipating power. Also, all devices cannot be minimum size devices due to the impedance relationships and therefore layout efficiency is sacrificed. Finally, two power supply leads must be brought to the circuit decreasing layout efficiency.

United States Patent No. 3,365,707 discloses a dynamically clocked logic circuit in which a logic circuit as above described is modified by gating the load FET as well as the gating FET. In this arrangement current flows only during the gating process. Therefore, the power dissipation in the circuit is reduced. Standby current still flows, however, during gating and the other disadvantages still remain.

Another type of logic circuit employing large scale integrated circuits includes a gated load transistor in series with a second gating transistor also in series with a logic network. The series chain is connected between two voltage levels. The gated load transistor is pulsed to charge an output capacitor. After the output capacitor is charged, the load transistor is turned OFF

and the second gating transistor is pulsed to discharge the capacitor if the logic network provides a short. In this way, an open circuit logic network leaves the voltage on the capacitor while the shorted logic circuit discharges it. In this circuit, no standing current is required, minimizing the power dissipated in performing logic functions. The impedance values of the various FET devices may vary over a wide range without affecting circuit operation. This arrangement, however, still requires two FET's in addition to the logic network. Power supply leads must still be brought to the circuit. This circuit also requires two clocking pulses as opposed to one for each stage of logic.

According to the invention there is provided a logic system comprising first and second capacitive means, first means responsive to a clock signal for periodically passing current in one direction only to charge the second capacitive means, second means responsive to the charge state of the first capacitive means for selectively passing current to discharge the second capacitive means, the charge remaining on the second capacitive means at a predetermined time after the first means ceases to conduct depending on the value of the charge state of the first capacitive means, and third means responsive to the clock signal for periodically connecting a data input to the first capactive means, the charge (if any) on the first capacitive means being isolated from the data input after each such periodic connection.

The invention will now be described, by way of example, with reference to the accompanying drawing which is a diagram of a logic circuit embodying the present invention.

Referring now to the drawing, the logic circuit shown provides both a gated data signal and its complement. The data signal applied to a first electrode 33 of a field effect transistor 34 is periodically sampled by a clocking signal such as signal ϕ_1. The signal ϕ_1 is applied to the gate 36 of field effect transistor 34 by leads 37 and 38 to pass the information from the data signal to capacitor 39 when the signal ϕ_1 goes negative. The signal ϕ_1 is also applied to common electrodes 41 and 42 of parallel connected field effect transistors 43 and 44, respectively, and the gate 46 of field effect transistor 43. The field effect transistor 43 is thereby turned on when ϕ_1 goes negative charging capacitor 47 to the negative level thereof. When the clocking signal ϕ_1 returns to ground field effect transistor 43 is turned off. The state of field effect transistor 44 is controlled by the signal stored on capacitor 39. If a negative signal appears on capacitor 39, field effect transistor 44 is turned on discharging the capacitor 47 through field effect transistor 44 to the ground level of the signal ϕ_1. If, on the other hand, a ground signal is present on the capacitor 39, the field effect transistor 44 remains in an OFF condition so that the negative signal remains on the capacitor 47. Thus, the signal appearing on the capacitor 47 is always the complement of the signal on capacitor 39 a fixed time after the signal ϕ_1 returns to ground.

In an integrated circuit structure, the capacitances 39 and 47 may be distributive, and would typically be about 2×10^{-12} farads.

Although the gating devices have been shown as switched FETs, simple diodes may be employed to perform the gating function.

As will be appreciated, all power for circuit operation is extracted from the clock signal provided. It should be further noted that no standing current flows in the circuit, The only current flowing is that required to charge and discharge the capacitors 39 and 47.

While the dynamically clocked logic system described herein has general applicability for use in various data-processing and logic systems, one particular application in which it may be employed advantageously is disclosed in U.S. Patent No. 3,618,050.

WHAT WE CLAIM IS:—

1. A logic system comprising first and second capacitive means, first means responsive to a clock signal for periodically passing current in one direction only to charge the second capacitive means, second means responsive to the charge state of the first capacitive means for selectively passing current to discharge the second capacitive means, the charge remaining on the second capacitive means at a predetermined time after the first means ceases to conduct depending on the value of the charge state of the first capacitive means, and third means responsive to the clock signal for periodically connecting a data input to the first capacitive means, the charge (if any) on the first capacitive means being isolated from the data input after each such periodic connection.

2. A system as claimed in claim 1 wherein the first, second and third means each comprises a field effect transistor.

3. A system as claimed in claim 1 or 2 constructed in integrated circuit form, the first and second capacitances being distributive.

4. A logic system adapted and arranged to operate substantially as herein described with reference to the accompanying drawing.

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