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PATENT SPECIFICATION

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(54) GAIN CONTROLLED AMPLIFIER CIRCUIT

(71) We, R.C.A. CORPORATION, formerly RADIO CORPORATION OF AMERICA, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to gain controlled amplifier circuits with particular reference to automatic gain control bias circuits in field-effect transistor amplifiers.

Multiple gate field-effect transistors, such as tetrode MOS transistors are field-effect transistors having two or more gate electrodes in addition to the source and drain electrodes. These devices have attractive characteristics for many circuit applications. Some of these characteristics are (1) high input impedance, (2) good cross-modulation performance, (3) low noise, (4) simplified direct coupling capability, and (5) compatibility with integrated circuit techniques.

It has been recognised, in part due to the cross-modulation performance, that semiconductor circuit structure multiple gate field-effect transistors are well suited for automatic gain controlled high frequency amplifiers.

Since there is often a substantial variation in drain current from one field-effect transistor to the next for a given gate bias voltage, it is desirable to provide a resistor in series with the source electrode to provide DC generation and thereby reduce variation in drain current of production units. The provision of this resistor in the source electrode circuit, however, creates a situation where the voltage between the gate electrodes and the source electrode vary as the current through the device changes.

A gain controlled amplifier circuit according to the present invention includes a semiconductor device such as multiple gate field-effect transistor having a source electrode, a drain electrode, and a plurality of gate electrodes. Input signals are applied to a first of the plurality of gate electrodes and a gain controlling potential is applied to a second gate electrode. A resistor interconnects the source electrode and a reference potential. Circuit means apply a portion of the gain controlling potential also to the first gate electrode, whereby the voltage between it and the source electrode can be maintained relatively constant with changing device current.

A fuller understanding of the invention may be obtained from the following detailed description of a specific embodiment thereof, when taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a schematic circuit diagram of an automatic gain controlled tetrode field-effect transistor amplifier embodying the present invention; and

FIGURE 2 is a schematic circuit diagram of the bias arrangement shown in FIGURE 1 modified to permit the use of a gain controlling potential of one polarity.

Reference is now made to FIGURE 1. A tetrode MOS field-effect transistor 10 having a drain electrode 12, a source electrode 14, a first gate electrode 16 and a second gate electrode 18 is connected as a high frequency automatic gain controlled amplifier. Input signals to the amplifier are applied at an input terminal 20 and passed through a DC blocking capacitor 22 to the first gate electrode 16. A gain controlling potential is applied to an automatic gain control input terminal 24 which is directly connected to the second gate electrode 18 by a decoupling resistor 27. High frequency signals appearing at the gain control terminal 24 are shorted to a ground 26 by a bypass capacitor 28.

The application of gain controlling voltages to the second gate electrode 18 as

[Price 25p]

opposed to the first gate electrode 16 provides the advantages of an improved remote cut-off characteristic, and improved cross modulation performance. In addition, in available tetrode insulated gate field-effect transistors, the first gate electrode cannot with stand the normal range of gain controlling voltages required to achieve the necessary gain control range. However, the second gate electrode has a thicker oxide insulating barrier and can handle the larger range of automatic gain controlling voltages.

Two resistors 30 and 32 are connected in series between the second gate electrode 18 and a terminal 34 which is connected to a reference potential shown as the ground 26. The junction of the serially connected resistors 30 and 32 is connected to the first gate electrode 16 to apply a portion of the gain controlling potential at the gain control terminal 24, to the first gate electrode 16. In this manner any voltage change at the gain control terminal 24 with respect to the ground will result in a change in voltage at the junction of the resistors 30-32 with respect to the ground and hence at the first gate electrode 16. Two capacitors 31 and 33 interconnect the second gate electrode 18 and the first gate electrode 16, respectively, with the ground 26. The capacitor 31 shorts high frequency signals appearing at the second gate electrode to the ground 26. Capacitor 33, in conjunction with other capacitances, aids in the tuning of an input resonant circuit, not shown, which is to be connected to the amplifier input terminal 20.

Because there is often substantial variation in the drain current from one field-effect transistor to the next, it is desirable to provide DC degeneration and thereby reduce variations in the drain current of production units. Thus, a resistor 36, which is bypassed at input signal frequencies by a capacitor 38, interconnects the source electrode 14 and the grounded terminal 34 to provide the desired DC degeneration. The inclusion of the resistor 36, however, causes the voltage at the source electrode to vary as the drain current changes. That is the I_DR_{36} voltage drop varies as the drain current I_D changes in response to changes in the AGC potential.

If the serially connected resistor 30 was omitted, a change in the drain current caused by a change in the gain controlling potential applied at the terminal 24 would cause a change in voltage between the first gate electrode 16 and the source electrode 14. This change in the first gate electrode to source electrode voltage would move the operating point of the transistor 10, if left uncompensated.

A source of positive operating potential for the transistor 10 is provided by a power supply, not shown, connected to a terminal 40. A tuned circuit 42 connects the source of potential at the terminal 40 to the drain electrode 12. Output signals are developed between terminals 44 and 44' which are connected to an inductor 46, coupled to the L-C circuit 42.

Under the condition of maximum gain, a positive gain controlling potential is applied to the terminal 24. As the potential at the terminal 24 decreases (becomes less positive), the drain current I_D also decreases with a resultant decrease in (less positive) voltage at the source electrode 14 (I_DR_{36}). This change in source potentail tends to increase the voltage difference betwen the first gate elctrode and the source electrode. However, because a portion of the change in the negative going gain controlling potential is applied to the first gate electrode 16 the change in voltage between the first gate electrode and the source electrode is minimized. In this manner, the bias arrangement tends to keep the first gate electrode to source electrode voltage constant as the automatic gain controlling potential varies, and, hence, the operating point of the transistor 10 tends to remain constant as the automatic gain controlling potential applied to the second gate electrode 18 changes.

Reference is now made to the circuit shown in FIGURE 2 which is similar to that described above. The main difference in the circuit of FIGURE 2 is the addition of two resistors 48 and 50 which permit the use of a gain controlling potential of one polarity as is often desired.

The resistors 48 and 50 are serially connected between the source of operating potential at the terminal 40 and the ground 26. The junction of the resistors is connected to the terminal 34 and provides a positive reference voltage at that terminal. The entire circuit is thus raised above the ground potential to a desired level which will permit the use of a gain controlling potential of one polarity, which in the present instance is positive.

A particular set of values for the embodiments shown in the drawings which has provided satisfactory operation are set forth below. It will be appreciated that these values are by way of example only.

FIGURE 1

Transistor 10	RCA 3N140
Capacitor 22	27 picafarads
Capacitor 28	1,000 picafarads
Capacitor 31	1,000 picafarads
Capacitor 33	10 picafarads
Capacitor 38	1,000 picafarads
Resistor 27	100 ohms
Resistor 30	820,000 ohms
Resistor 32	270,000 ohms
Resistor 36	270 ohms
B+(terminal 40)	+15 volts

With the above values for the various

circuit elements, an automatic gain controlling voltage, which can be a function of the strength of the amplifier input signal, ranging from +8 volts to −3 volts resulted in a 50db reduction in the gain of the amplifier.

FIGURE 2

Transistor 10	RCA 3N140	
Capacitor 22	1,000	picafarads
Capacitor 28	1,000	pcafarads
Capacitor 38	1,000	pcafarads
Resistor 30	820,000	ohms
Resistor 32	330,000	ohms
Resistor 36	180	ohms
Resistor 48	500	ohms
Resistor 50	100	ohms
B+(terminal 40)	+18	volts

It is to be understood that a P-channel semiconductor circuit structure could be utilized in place of the N-channel device shown, with corresponding changes in the polarity of the operating potential and bias potential source.

Attention is drawn to our copending application No. 58806 of 1968 ,Serial No. 1,242,859).

WHAT WE CLAIM IS:—

1. An amplifier circuit comprising: a semiconductor device having a source electrode, a drain electrode, and a plurality of gate electrodes; means for applying input signals to a first of said plurality of gate electrodes; means for applying a gain controlling potential to a second of said plurality of gate electrodes, a resistor connected to said source electrode such that changes in the gain controlling potential tend to change the current through said resistor and hence the voltage between said source and said first gate electrode, and circuit means for applying a portion of said gain controlling potential to said first gate electrode.

2. An amplifier circuit as defined in Claim 1 wherein said circuit means includes a resistor interconnecting said first and second gate electrodes.

3. An amplifier circuit as defined in Claim 1 or Claim 2 wherein said first gate electrode is physically closer to said source electrode than said second gate electrode.

4. An amplifier circuit as defined in any preceding Claim, with means for establishing a reference potential at the remote end of said resistor connected to said source electrode so that said gain controlling potential is of one polarity throughout its range.

5. An amplifier circuit substantially as hereindescribed with reference to FIGURE 1 of the accompanying drawings.

6. An amplifier circuit substantially as herein described with reference to FIGURE 2 of the accompanying drawings.

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London, W.1.
Agent for the Applicant.

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