

SEMICONDUCTOR MEMORY DEVICE HAVING ELECTRICALLY FLOATING BODY TRANSISTOR, AND HAVING BOTH VOLATILE AND NON-VOLATILE FUNCTIONALITY AND METHOD

Abstract

A semiconductor memory cell includes a floating body region configured to be charged to a level indicative of a state of the memory cell; a first region in electrical contact with said floating body region; a second region in electrical contact with said floating body region and spaced apart from said first region; and a gate positioned between said first and second regions. The cell may be a multi-level cell. Arrays of memory cells are disclosed for making a memory device. Methods of operating memory cells are also provided.

[Figure 1]