CLAIMS

1. An apparatus, comprising: a first circuit; a second circuit; a power gating circuit configured to generate a first load current through the first circuit and a second load current through the second circuit; and a current sensor configured to generate a first signal related to the first load current and the second load current, wherein the current sensor includes a first ring oscillator, wherein the first ring oscillator comprises: a first set of one or more inverters coupled to a first node between the power gating circuit and the first circuit, and a second set of one or more inverters coupled to a second node between the power gating circuit and the second circuit, wherein the one or more inverters of the first set are cascaded with the one or more inverters of the second set to form at least a portion of a single ring of inverters.

2. The apparatus of claim 1, wherein the first ring oscillator is configured to generate a second signal with a first frequency related to a first voltage difference between a first rail voltage at a first voltage rail and a first voltage at the first node, and a second voltage difference between the first rail voltage and a second voltage at the second node, wherein the first signal is based on the second signal.

3. The apparatus of claim 2, wherein the power gating circuit comprises: a first set of one or more transistors coupled between the first voltage rail and the first node, wherein the first set of one or more transistors is configured to generate the first load current through the first circuit based on a control signal; and a second set of one or more transistors coupled between the first voltage rail and the second node, wherein the second set of one or more transistors is configured to generate a second load current through the second circuit based on the control signal.

4. The apparatus of claim 3, wherein the first and second sets of transistors each comprise a p-channel metal oxide semiconductor (PMOS) field effect transistor (FET).

5. The apparatus of claim 3, wherein the first and second sets of transistors each comprise an n-channel metal oxide semiconductor (NMOS) field effect transistor (FET).

6. The apparatus of claim 2, wherein the current sensor comprises a second ring oscillator configured to generate a third signal with a second frequency related to a third voltage difference between the first rail voltage and a second rail voltage, wherein the first signal is based on the third signal.

7. The apparatus of claim 6, wherein the current sensor further comprises: a first frequency-to-code (FTC) converter configured to generate a first digital signal related to the first frequency; a second frequency-to-code (FTC) converter configured to generate a second digital signal related to the second frequency; and a subtractor configured to generate the first signal based on a difference between the first digital signal and the second digital signal.

8. The apparatus of claim 2, wherein the current sensor further comprises a frequency-to-code (FTC) converter configured to generate a first digital signal related to the first frequency.

9. The apparatus of claim 8, wherein the frequency-to-code (FTC) converter comprises: an n-bit counter coupled to an input of one of the inverters; a set of 1-bit counters coupled to inputs of the remaining inverters, respectively; an n-bit flip-flop configured to latch an output of the n-bit counter based on a clock signal; and a set of 1-bit flip-flops configured to latch outputs of the 1-bit counters based on the clock signal, respectively.

10. An apparatus, comprising: a first circuit; a second circuit; a power gating circuit configured to generate a first load current through the first circuit and a second load current through the second circuit; and a current sensor configured to generate a first signal related to the first load current and the second load current, wherein the current sensor includes a first ring oscillator comprising: a first set of one or more inverters coupled to a first node between the power gating circuit and the first circuit, and a second set of one or more inverters coupled to a second node between the power gating circuit and the second circuit; wherein the first ring oscillator is configured to generate a second signal with a first frequency related to a first voltage difference between a first rail voltage at a first voltage rail and a first voltage at the first node, and a second voltage difference between the first rail voltage and a second voltage at the second node, wherein the first signal is based on the second signal; wherein the current sensor further comprises a frequency-to-code (FTC) converter configured to generate a first digital signal related to the first frequency; wherein the FTC converter comprises: an n-bit counter coupled to an input of one of the inverters; a set of 1-bit counters coupled to inputs of the remaining inverters, respectively; an n-bit flip-flop configured to latch an output of the n-bit counter based on a clock signal; a set of 1-bit flip-flops configured to latch outputs of the 1-bit counters based on the clock signal, respectively; a multiplier configured to generate a coarse digital value related to the first frequency by multiplying by an integer number to the latched output of the n-bit flip-flip; a set of exclusive-OR gates to collectively generate a fine digital value of the first frequency, the set of exclusive-OR gates including respective first inputs coupled to a least significant bit of the n-bit flip-flop and respective second inputs configured to receive the latched outputs of the 1-bit flip-flop, respectively; and an adder to add the coarse digital value to the fine digital value to generate the second signal.

11. A method, comprising: generating a first load current through a first circuit and a power gating circuit; generating a second load current through a second circuit and the power gating circuit; and generating a first signal related to the first load current and the second load current, wherein generating the first signal comprises: applying a first voltage at a first node between the first circuit and the power gating circuit to a first set of one or more inverters of a first ring oscillator; and applying a second voltage at a second node between the second circuit and the power gating circuit to a second set of one or more inverters of the first ring oscillator, wherein the one or more inverters of the first set are cascaded with the one or more inverters of the second set to form at least a portion of a single ring of inverters.

12. The method of claim 11, wherein generating the first signal comprises the first ring oscillator generating a second signal with a first frequency related to a first voltage difference between a first rail voltage at a first voltage rail and the first voltage, and a second voltage difference between the first rail voltage and the second voltage.

13. The method of claim 12, wherein generating the first load current comprises: turning on a first set of one or more transistors coupled between the first voltage rail and the first node based on a control signal; and turning on a second set of one or more transistors coupled between the first voltage rail and the second node based on the control signal.

14. The method of claim 13, wherein the first and second sets of transistors each comprise a p-channel metal oxide semiconductor (PMOS) field effect transistor (FET).

15. The method of claim 13, wherein the first and second sets of transistors each comprise an n-channel metal oxide semiconductor (NMOS) field effect transistor (FET).

16. The method of claim 12, wherein generating the first signal comprises a second ring oscillator generating a third signal with a second frequency related to a third voltage difference between the first rail voltage and a second rail voltage.

17. The method of claim 16, wherein generating the first signal further comprises: generating a first digital signal related to the first frequency; generating a second digital signal related to the second frequency; and generating a difference between the first digital signal and the second digital signal, wherein the first signal is based on the difference.

18. The method of claim 12, wherein generating the first signal comprises generating a first digital signal related to the first frequency.

19. An apparatus, comprising: means for generating a first load current through a first circuit; means for generating a second load current through a second circuit; and means for generating a first signal related to the first load current and the second load current, wherein the means for generating the first signal comprises: means for applying a first voltage at a first node between the first circuit and the means for generating the first load current to a first set of one or more inverters of a means for generating a second signal; and means for applying a second voltage at a second node between the second circuit and the means for generating the second load current to a second set of one or more inverters of the means for generating the second signal, wherein the one or more inverters of the first set are cascaded with the one or more inverters of the second set to form at least a portion of a single ring of inverters.

20. The apparatus of claim 19, wherein the means for generating the second signal comprises means for generating the second signal with a first frequency related to a first voltage difference between a first rail voltage at a first voltage rail and the first voltage, and a second voltage difference between the first rail voltage and the second voltage.

21. The apparatus of claim 20, wherein the means for generating the first load current comprises: means for turning on a first set of one or more transistors coupled between the first voltage rail and the first node based on a control signal; and means for turning on a second set of one or more transistors coupled between the first voltage rail and the second node based on the control signal.

22. The method of claim 21, wherein the first and second sets of transistors each comprise a p-channel metal oxide semiconductor (PMOS) field effect transistor (FET).

23. The method of claim 21, wherein the first and second sets of transistors each comprise an n-channel metal oxide semiconductor (NMOS) field effect transistor (FET).

24. The method of claim 20, wherein the means for generating the first signal comprises means for generating a third signal with a second frequency related to a third voltage difference between the first rail voltage and a second rail voltage.

25. The apparatus of claim 24, wherein the means for generating the first signal further comprises: means for generating a first digital signal related to the first frequency; means for

generating a second digital signal related to the second frequency; and means for generating a difference between the first digital signal and the second digital signal, wherein the first signal is based on the difference.

26. The apparatus of claim 20, wherein the means for generating the first signal comprises means for generating a first digital signal related to the first frequency.