CLAIMS

1. A holding circuit comprising:

a first input terminal;

a second input terminal;

a third input terminal;

a first output terminal;

a first switch;

a second switch;

a third switch;

a capacitor; and

a node,

wherein the first switch is configured to control conduction between the node and the first input terminal,

wherein the second switch is configured to control conduction between the node and the first output terminal,

wherein the third switch is configured to control conduction between the second input terminal and the first output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to the third input terminal, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

2. The holding circuit according to claim 1, wherein the third switch is a transistor comprising an oxide semiconductor layer.

3. The holding circuit according to claim 1, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

4. The holding circuit according to claim 1, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

5. A semiconductor device comprising:

the holding circuit according to claim 1; and

a circuit comprising:

a fourth input terminal;

a fifth input terminal;

a second output terminal;

a selection circuit; and

a sequential circuit,

wherein the selection circuit is configured to control conduction between an input terminal of the sequential circuit and one of the fourth input terminal and the fifth input terminal,

wherein the second output terminal is electrically connected to an output terminal of the sequential circuit,

wherein the first output terminal of the holding circuit is electrically connected to the fifth input terminal, and

wherein the first input terminal of the holding circuit is electrically connected to the fourth input terminal, the second output terminal, or an internal node of the sequential circuit.

6. The semiconductor device according to claim 5, wherein one of the first input terminal and the first output terminal is electrically connected to one of a buffer circuit and an inverter circuit.

7. The semiconductor device according to claim 5, wherein the circuit comprises a transistor comprising silicon.

8. The semiconductor device according to claim 5 comprising:

a CPU core.

9. An electronic device comprising:

the semiconductor device according to claim 5; and

one of a housing, a microphone, a speaker, a display portion, and an operation key.

10. A method for driving a holding circuit comprising a first input terminal, a second input terminal, a third input terminal, an output terminal, a first switch, a second switch, a third switch, a capacitor, and a node, comprising a first processing comprising the steps of:

turning off the first switch and turning on the second switch and the third switch;

inputting a first potential to the second input terminal; and

inputting a second potential to the third input terminal,

wherein a first terminal of the first switch is electrically connected to the first input terminal,

wherein a second terminal of the first switch is electrically connected to the node,

wherein a first terminal of the second switch is electrically connected to the node,

wherein a second terminal of the second switch is electrically connected to the output terminal,

wherein a first terminal of the third switch is electrically connected to the second input terminal,

wherein a second terminal of the third switch is electrically connected to the output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to the third input terminal, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

11. The method according to claim 10, wherein the third switch is a transistor comprising an oxide semiconductor layer.

12. The method according to claim 10, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

13. The method according to claim 10, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

14. The method according to claim 10, wherein the first potential is capable of making a logic level of the node low.

15. The method according to claim 10 comprising:

a second processing after the first processing; and

a third processing after the second processing,

wherein the second processing comprises the steps of:

turning on the first switch and turning off the second switch and the third switch; and

inputting a third potential that is higher than the second potential to the third input terminal, and

wherein the third processing comprises the steps of:

turning off the first switch, the second switch, and the third switch; and

inputting the third potential to the third input terminal.

16. The method according to claim 10 comprising:

a second processing after the first processing; and

a third processing after the second processing,

wherein the second processing comprises the steps of:

turning off the first switch and turning on the second switch and the third switch; and

inputting a third potential that is higher than the second potential to the third input terminal, and

wherein the third processing comprises the steps of:

turning off the first switch, the second switch, and the third switch; and

inputting the third potential to the third input terminal.

17. The method according to claim 16 comprising:

a fourth processing after the third processing,

wherein the fourth processing comprises the steps of:

turning off the first switch and the third switch;

turning on the second switch; and

inputting the third potential to the third input terminal.

18. A semiconductor device comprising:

a holding circuit comprising:

a first switch;

a second switch;

a third switch;

a capacitor; and

a node,

a circuit, an input terminal of the circuit being electrically connected to an output terminal of the holding circuit, comprising:

a sequential circuit; and

a selection circuit electrically connected between the input terminal of the circuit and the sequential circuit,

wherein a first terminal of the first switch is electrically connected to a first input terminal of the holding circuit,

wherein a second terminal of the first switch is electrically connected to the node,

wherein a first terminal of the second switch is electrically connected to the node,

wherein a second terminal of the second switch is electrically connected to the output terminal,

wherein a first terminal of the third switch is electrically connected to a second input terminal of the holding circuit,

wherein a second terminal of the third switch is electrically connected to the output terminal,

wherein a first terminal of the capacitor is electrically connected to the node,

wherein a second terminal of the capacitor is electrically connected to a third input terminal of the holding circuit, and

wherein the first switch and the second switch are each a transistor comprising an oxide semiconductor layer.

19. The semiconductor device according to claim 18, wherein the third switch is a transistor comprising an oxide semiconductor layer.

20. The semiconductor device according to claim 18, wherein the oxide semiconductor layer comprises indium, gallium, and zinc.

21. The semiconductor device according to claim 18, wherein the oxide semiconductor layer has a crystal part with c-axis alignment.

22. The semiconductor device according to claim 18, wherein the circuit comprises a transistor comprising silicon.

23. The semiconductor device according to claim 18, wherein the first input terminal of the holding circuit is electrically connected to the input terminal of the circuit, an output terminal of the circuit, or an internal node of the sequential circuit.

24. The semiconductor device according to claim 18, wherein one of the first input terminal and the output terminal is electrically connected to one of a buffer circuit and an inverter circuit.

25. The semiconductor device according to claim 18 comprising:

a CPU core.

26. An electronic device comprising:

the semiconductor device according to claim 18; and

one of a housing, a microphone, a speaker, a display portion, and an operation key.