Description

Title of Invention: POWER CONVERTER

Technical Field

[0001] The present invention relates to a power converter including a power buffer circuit.

Background Art

[0002] A full-wave rectifying circuit is typically used to obtain a DC voltage from a single-phase AC voltage input from a single-phase AC power supply. An output from the full-wave rectifying circuit, however, has power pulsations having a frequency twice the frequency of the single-phase AC voltage. To reduce the power pulsations, a power buffer circuit for buffering a power is thus required between an output of the full-wave rectifying circuit and a load. A capacitive element, for example, referred to as a smoothing capacitor is required for buffering a power.

[0003] Non-patent Document 1 discloses a technique for connecting a buffer capacitor to a smoothing capacitor via a current-reversible chopper to absorb a pulsating power. This technique reduces the electrostatic capacitance of the smoothing capacitor and further allows voltage ripples at the buffer side to greatly reduce the total electrostatic capacitance required for smoothing.

[0004] Non-patent Document 2 and Patent Document 1 disclose a technique for connecting a buffer capacitor to a DC link via a switching element while removing the smoothing capacitor of Non-patent Document 1. A direct conversion circuit is described that generates a voltage source by this technique and generates a high-frequency link along with a power supply voltage.

[0005] Non-patent Document 3 further discloses a technique for converting an input waveform into a sinusoidal waveform and increasing efficiency.

Strategy of single-to-three Phase Power Converter with Active Buffer and Charge Circuit", the 2010 Annual Meeting of IEEJ, 4-057 (2010).

Non-patent Document 3: Ohnuma, Itoh, "Comparison between a Boost Chopper and an Active Buffer as a Single to Three Phase Converter", 2011 Annual Meeting of IEEJ, 4-042 (2011).

Non-patent Document 4: Ohnuma, Itoh, "Control Strategy of Single Phase to Three Phase Power Converter Using an Active Snubber", 2008 IEEJ Industry Applications Society Conference, 1-20 (2008).

Summary of Invention

Problem to be Solved by Invention

[0011] Patent Document 3 proposes a technique for generating a voltage across a DC link using the voltage at the power supply and the voltage at the power buffer circuit. This can increase the voltage across the DC link. In view of the breakdown voltage of a capacitor used in the power buffer circuit, however, the voltage of the power buffer circuit is desirably adjusted to be not greater than 1.2 times the crest value of the power supply voltage. When the voltage of the power buffer circuit is set to such a value, the power buffer circuit mainly covers the power. In this case, the power supplied from the full-wave rectifying circuit to the inverter is an auxiliary power, and there is a trade-off between boosting the voltage across the DC link and obtaining high efficiency characteristics that are a feature of the direct power converter.

[0012] Embodiments of the present application seek to provide a technique for increasing the voltage across a DC link without increasing the power covered by a power buffer circuit.

Means for Solving the Problem

half of a period of the single-phase AC voltage.

[0015] In a second aspect of the power converter according to the present invention, in the first aspect, the rectifying duty takes any one smaller value of an absolute value ($|\sin(\omega t)|$) of a sine value of the phase and a value (1 - dc) obtained by subtracting the discharge duty (dc) from 1.

[0016] In a third aspect of the power converter according to the present invention, in the first aspect, the rectifying duty takes a value (1- dc) obtained by subtracting the discharge duty (dc) from 1.

[0017] In a fourth aspect of the power converter according to the present invention, in any one of the first to third aspects, a ratio (Vc/Vm) of the both-end voltage (Vc) to the crest value (Vm) is 1 or more and 1.2 or less.

[0018] In a fifth aspect of the power converter according to the present invention, in any one of the first to fourth aspects, the inverter (5) performs DC-AC conversion with a minimum value of the DC voltage (Vdc) as an upper limit.

[0019] In a sixth aspect of the power converter according to the present invention, in any one of the first to fourth aspects, the DC voltage varies with a quarter of the period of the single-phase AC voltage as a fundamental period.

[0020] In a seventh aspect of the power converter according to the present invention, in any one of the first to fourth aspects, the DC voltage varies in a pair of sections that are not adjacent to each other among sections equally dividing the period of the single-phase AC voltage into four and is constant in the other pair of sections.

Effects of the Invention

[0021] The DC voltage (Vdc) varies in a period in which the discharge duty (dc) varies. This increases a crest value/both-end voltage (Vm/Vc) that affects the discharge duty (dc) (i.e., reduces the both-end voltage (Vc)) to increase the DC voltage (Vdc). In other

words, the both-end voltage (Vc) that is required for obtaining a desired DC voltage (Vdc) is reduced, thus reducing a breakdown voltage required for the capacitor (C4).

[0022] The objects, features, aspects, and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0023] FIG. 1 is a block diagram showing a configuration of a direct power converter according to an embodiment;

FIG. 2 is a block diagram showing a power balance in the direct power converter according to the embodiment;

FIG. 3 is a circuit diagram showing an equivalent circuit of a circuit shown in FIG. 1;

FIG. 4 is a graph showing an operation of the direct power converter when a basic setting of duty is adopted;

FIG. 5 is a graph showing a voltage utilization ratio to a voltage ratio when the basic setting of duty is adopted;

FIG. 6 is a graph showing an operation of the direct power converter when the technique described in Patent Document 3 is used;

FIG. 7 is a graph showing an operation of the direct power converter when a first modification of duty is adopted;

FIG. 8 is a graph showing a rectifying duty, a discharge duty, and a zero duty when the first modification of duty is adopted and when a second modification of duty is adopted;

FIGs. 9 and 10 are graphs showing the validity of an approximation;

FIG. 11 is a graph showing the dependence of voltage utilization ratio on phase when the second modification of duty is adopted;

FIG. 12 is a graph showing the dependence of voltage utilization ratio on phase when the first modification of duty is adopted;

FIG. 13 is a graph showing the dependence of voltage utilization ratio on phase when the basic setting of duty is adopted;

FIG. 14 is a graph showing the dependence of a voltage utilization ratio R on a voltage ratio α;

FIG. 15 is a graph showing the dependence of duties on phase when the basic setting of duty is used;

FIG. 16 is a graph showing the dependence of duties on phase when the first modification of duty is used and when the second modification is used;

FIG. 17 is a graph showing an operation of the direct power converter when the first modification of duty is adopted;

FIG. 18 is a graph showing an operation of the direct power converter when the basic setting of duty is adopted;

FIG. 19 is a graph showing a ratio between two types of powers;

FIG. 20 is a graph showing an operation of a switch of an equivalent circuit and an operation of a switching element of an inverter;

FIG. 21 is a circuit diagram showing a first modification;

FIG. 22 is a graph showing an operation of the direct power converter according to a second modification; and

FIG. 23 is a graph showing an operation of the direct power converter according to a third modification.

the operations of the switches Sc and Sl, which are generated based on duties drec, dc, dz, and dl (for example, see Patent Document 1).

[0041] B. Control Method

(b-1) Basic Concept of Power Reduction

An instantaneous input power Pin input to the converter 3 is expressed by Formula (1) below with an input power factor being 1. Note that a crest value Vm and a power supply angular velocity ω of the single-phase AC voltage Vin, a crest value Im of the AC input current Iin, and a time t are introduced. A product ωt of the power supply angular velocity ω and the time t represents a phase of the single-phase AC voltage Vin. An AC waveform is understood as the product of a sine value of the phase ωt of the AC waveform and a crest value.

[0042]

$$\begin{aligned} Pin &= Vm \cdot Im \cdot \sin^2(\omega t) \\ &= \frac{1}{2} Vm \cdot Im - \frac{1}{2} Vm \cdot Im \cdot \cos(2\omega t) \quad \cdots (1) \end{aligned}$$

[0043] The instantaneous input power Pin has an AC component $(-1/2) \cdot Vm \cdot Im \cdot \cos(2\omega t)$ (hereinafter, also referred to as an "AC component Pin^") shown by the second term of the right-hand side of Formula (1). The instantaneous input power Pin is thus hereinafter also referred to as a pulsating power Pin.

[0044] The power converter shown in FIG. 1 can be understood as follows:

[0045] The DC link 7 includes the DC power supply lines LH and LL;

The converter 3 receives the single-phase AC voltage Vin and outputs the pulsating power Pin;

The power buffer circuit 4 receives a charge power Pl from the DC link 7 and outputs a discharge power Pc to the DC link 7; and

The inverter 5 receives, from the DC link 7, an input power Pdc (= Pin + Pc - Pl)

[0051]

$$Pl = \frac{1}{2} \cdot Vm \cdot Im \cdot \sin^2(\omega t) \quad \ldots(2)$$

[0052]

$$Pc = \frac{1}{2} \cdot Vm \cdot Im \cdot \cos^2(\omega t)$$
$$= \frac{1}{2} \cdot Vm \cdot Im \cdot \cos(2\omega t) + Pl \quad \ldots(3)$$

[0053] This means that the charge power Pl is a half power of the pulsating power Pin, and the discharge power Pc is a power obtained by subtracting the AC component Pin^ from the charge power Pl.

[0054] The charge power Pl can be understood as a power (1/2)·Pin distributed from the pulsating power Pin to the power buffer circuit 4 via the DC link 7 at a distribution ratio of 1/2.

[0055] From Formulas (2) and (3) and Pbuf = Pc - Pl, the buffering power Pbuf is also expressed by Formula (4).

[0056]

$$Pbuf = \frac{1}{2} \cdot Vm \cdot Im \cdot \cos(2\omega t) \quad \ldots(4)$$

[0057] It is obvious that the charge power Pl and the discharge power Pc are different from those in the quarter-period control described above.

[0058] Discharge is dominant over charge in a period (hereinafter, also referred to as a "discharge dominant period") in which Pc > Pl (i.e., Pbuf > 0), and charge is dominant over discharge in a period (hereinafter, also referred to as a "charge dominant period") in which Pc < Pl (i.e., Pbuf < 0). As can be understood from Formulas (2) and (3), a period in which $(n+1/4)\pi \leq \omega t \leq (n+3/4)\pi$ is the charge dominant period, and a period in which

$(n+3/4)\pi \leq \omega t \leq (n+5/4)\pi$ is the discharge dominant period (n is an integer: the same applies to the description below).

[0059] The voltage utilization ratio can be set up to 1 by determining the charge power Pl and the discharge power Pc as described above, which will be described below.

[0060] (b-3) Distribution of Current

This section will describe a technique for setting a current irec1 flowing from the converter 3 to the inverter 5 out of a current irec output from the converter 3 to a half of the current irec.

[0061] The rectified voltage Vrec expressed by Formula (5) is applied to the output side of the converter 3.

[0062]

$$Vrec = |Vin| = Vm \cdot |\sin(\omega t)| \quad \cdots(5)$$

[0063] Formula (6) below holds as Prec = Pin - Pl.

[0064]

$$Prec = \frac{1}{2} \cdot Vm \cdot Im \cdot \sin^2(\omega t) = |Vin| \cdot irec1 \quad \cdots(6)$$

[0065] The current irec1 is thus expressed by Formula (7) below.

[0066]

$$irec1 = \frac{1}{2} \cdot Im \cdot |\sin(\omega t)| \quad \cdots(7)$$

[0067] Formula (1) is based on the premise that the input current Iin is expressed by $Im \cdot \sin(\omega t)$, that is, has a sinusoidal waveform, and thus, the current il satisfies Formula (8) below. As can be seen from FIG. 2, this is because the current irec output from the converter 3 is equal to the sum of the current irec1 and the current il.

[0068]

$$il = \frac{1}{2} \cdot Im \cdot |\sin(\omega t)| \quad \cdots(8)$$

[0069] When a discharge current ic flowing from the capacitor C4 to the inverter 5 is introduced, the discharge power Pc output from the power buffer circuit 4 is expressed by a product Vc·ic. In order for the discharge power Pc to satisfy Formula (3), thus, it suffices that the discharge current ic satisfies Formula (9) below.

[0070]

$$ic = \frac{Pc}{Vc} = \frac{Vm \cdot Im}{2Vc} \cdot \cos^2(\omega t) \quad \cdots(9)$$

[0071] FIG. 3 shows an equivalent circuit of the circuit shown in FIG. 1. The equivalent circuit is introduced in Patent Document 1, for example. In the equivalent circuit, the current irec1 is equivalently expressed as a current irec1 passing through a switch Srec when this switch is conductive. Similarly, the discharge current ic is equivalently expressed as a current ic passing through the switch Sc when this switch is conductive.

[0072] A current flowing through the inverter 5 to the inductive load 6 when the output terminals Pu, Pv, and Pw are connected in common to any one of the DC power supply lines LH and LL in the inverter 5 is also equivalently expressed as a zero-phase current iz flowing through a switch Sz when this switch is conductive.

[0073] FIG. 3 also shows the reactor L4, the diode D40, and the switch Sl constituting the charge circuit 4b, and additionally shows the current il flowing through the reactor L4.

[0074] In the thus obtained equivalent circuit, Formula (10) below holds by introducing the duties drec, dc, and dz at which the switches Srec, Sc, and Sz are respectively conductive and a DC current Idc input into the inverter 5.

[0075]

$$\begin{bmatrix} irec \\ ic \\ iz \end{bmatrix} = \begin{bmatrix} drec & 1 \\ dc & 0 \\ dz & 0 \end{bmatrix} \cdot \begin{bmatrix} Idc \\ il \end{bmatrix} \quad \cdots(10)$$

[0076] The currents irec1, ic, and iz are respectively obtained by multiplying the DC current Idc by the duties drec, dc, and dz, and are accordingly average values in switching cycles of the respective switches Srec, Sc, and Sz.

[0077] The DC current Idc is the sum of the currents irec1, ic, and iz conducted by the respective switches Srec, Sc, and Sz, and thus, the following formula holds. Note that $0 \leq drec \leq 1$, $0 \leq dc \leq 1$, and $0 \leq dz \leq 1$.

[0078]

$$drec + dc + dz = 1 \quad \cdots(11)$$

[0079] The duties drec, dc, and dz can thus be considered as current distribution ratios of the DC current Idc to the respective currents irec1, ic, and iz. The duty drec may hereinafter also be referred to as a rectifying duty drec because it is a duty at which a period in which the converter 3 is connected to the DC link 7 and allows a current to flow through the inverter 5 is set. The duty dc may hereinafter also be referred to as a discharge duty dc because it is a duty at which the capacitor C4 discharges. The duty dz may hereinafter also be referred to as a zero duty dz because the duty dz is a duty at which the zero-phase current iz always flows through the inverter 5 regardless of a voltage output from the inverter 5.

[0080] The rectifying duty drec and the discharge duty dc are respectively set by Formulas (12) and (13) below from Formulas (7), (9), and (10).

[0081]

$$drec = \frac{1}{2} \cdot \frac{Im}{Idc} \cdot |\sin(\omega t)| \quad \cdots(12)$$

[0082]

$$dc = \frac{Vm}{2Vc} \cdot \frac{Im}{Idc} \cdot \cos^2(\omega t) \quad \cdots(13)$$

[0083] That is to say, Formulas (7), (9), (12), and (13) are used to meet the demand for power balance, and Formula (8) is used to further meet the demand for making the input current Iin be a sinusoidal waveform and satisfaction of Formula (1) on which the above-mentioned formulas are based.

[0084] When the converter 3 uses a diode bridge, the converter 3 cannot be actively switched at the rectifying duty drec expressed by Formula (12). By switching the inverter 5 and the switch Sc respectively in accordance with the zero duty dz and the discharge duty dc determined by Formulas (11), (12), and (13), the current irec1 expressed by Formula (7) can be obtained.

[0085] The inverter 5 cannot use the DC voltage at the DC link 7 in a period in which the zero-phase current iz flows. The DC voltage used in power supply to the inverter 5 in the DC link 7 is thus important in power conversion. In other words, the instantaneous DC voltage that is not used by the inverter 5 in power conversion is not important also in the consideration of a voltage utilization ratio. The DC voltage Vdc that is important in power conversion can thus be expressed as follows:

[0086]

$$Vdc = Vrec \cdot drec + Vc \cdot dc + 0 \cdot dz \quad \cdots(14)$$

[0087] On the other hand, the DC voltage Vdc can be understood as a voltage applied to the DC link 7 as an average of the maximum value of a voltage that the inverter 5 can output, in a period in which switching of the switches Sc and Sl and the inverter 5 is controlled. This is because though the inverter 5 can contribute to the voltage across the DC link 7 at a ratio, zero duty dz, the inverter 5 is insulated from any one of the DC

power supply lines LL and LH of the DC link 7 in the period corresponding to the zero duty dz.

[0088] The DC voltage Vdc is additionally shown in FIG. 3 as a voltage generated across a current source Idc (which flows the DC current Idc) representing the inverter 5 and a load thereof.

[0089] The input power Pdc input from the DC link 7 to the inverter 5 is the product of the DC voltage Vdc and the DC current Idc. Since the inverter 5 obtains, from the DC link 7, the input power Pdc (= Pin + Pc - Pl) obtained by subtracting the charge power Pl from the sum of the pulsating power Pin and the discharge power Pc, Formula (15) below holds.

[0090]

$$\begin{aligned} Idc &= \frac{Pin + Pc - Pl}{Vdc} \\ &= \frac{Vm \cdot Im}{2Vdc} \end{aligned} \quad \cdots(15)$$

[0091] Formulas (12) and (13) can be expressed as Formulas (16) and (17).

[0092]

$$\begin{aligned} drec &= \frac{Vdc}{Vm}\left|\sin(\omega t)\right| \\ &= \frac{Vdc}{Vrec} \cdot \sin^2(\omega t) \end{aligned} \quad \cdots(16)$$

[0093]

$$\begin{aligned} dc &= \frac{Vdc}{Vc} \cdot \cos^2(\omega t) \\ &= \frac{Vdc}{2Vc}(1 + \cos(2\omega t)) \end{aligned} \quad \cdots(17)$$

[0094] When the right-hand side of Formula (14) is calculated using Formulas (16) and (17), Formula (18) below is obtained, which matches the left-hand side of Formula (14).

[0095]

$$\begin{aligned} \text{drec}\cdot\text{Vrec}+\text{dc}\cdot\text{Vc} &= \text{Vdc}\left|\sin(\omega t)\right|\cdot\left|\sin(\omega t)\right|+\text{Vdc}\cdot\cos^2(\omega t) \\ &= \text{Vdc} \quad \ldots(18) \end{aligned}$$

[0096] In other words, it can be said that the rectifying duty drec and the discharge duty dc are respectively determined by Formulas (16) and (17) as a result of the determination of one DC voltage Vdc.

[0097] It is found from the forms of the functions of Formulas (16) and (17) or from the maximum values of the rectifying duty drec and the discharge duty dc being 1 that the DC voltage Vdc can be controlled at a constant value if $\text{Vdc} \leq \text{Vm}$ and $\text{Vdc} \leq \text{Vc}$. On this occasion, the rectifying duty drec can be determined by measuring a crest value Vm and designating one command value of the DC voltage Vdc.

[0098] The voltage utilization ratio can be expressed as a ratio R (= Vdc/Vm) of a DC voltage Vdc to a crest value Vm. Formulas (10), (11), and (14) reveal that the period in which the inverter 5 flows a zero-phase current is made shorter as the zero duty dz is made smaller, resulting in a longer period in which the voltage applied to the DC link voltage is used. This increases the voltage utilization ratio R.

[0099] Based on the premise that the input current Iin is expressed by $\text{Im}\cdot\sin(\omega t)$, that is, has a sinusoidal waveform, the current il depends on the DC current Idc and satisfies Formula (19) below. Herein, Formulas (7) and (15) are taken into account.

[0100]

$$\begin{aligned} \text{il} &= \text{Im}\cdot\left|\sin(\omega t)\right|-\text{drec}\cdot\text{Idc} \\ &= (\text{Im}-\frac{\text{Vdc}}{\text{Vm}}\cdot\text{Idc})\cdot\left|\sin(\omega t)\right| \\ &= \frac{\text{Im}}{2}\cdot\left|\sin(\omega t)\right| = \text{irecl} \qquad \cdots(19) \end{aligned}$$

[0101] That is to say, as in Formula (8), a half of the absolute value of the input current

[0108]

$$drec + dc = \frac{Vdc}{Vm} \cdot x + \frac{Vdc}{Vc} \cdot (1 - x^2) = 1 \quad \cdots(20)$$

[0109] Formula (21) is obtained by transforming Formula (20).

[0110]

$$Vdc = \frac{1}{\frac{x}{Vm} + \frac{1 - x^2}{Vc}} = \frac{Vm}{x + \frac{Vm}{Vc}(1 - x^2)} \quad \cdots(21)$$

[0111] The phase ωt providing a maximum value of the DC voltage Vdc provides a minimum value of a denominator of the right-hand side of Formula (21). Therefore, such a phase ωt is obtained as the phase ωt in which a value of Formula (22) indicating a derivative of the denominator is zero.

[0112]

$$\frac{d}{d(\omega t)}\left[|\sin(\omega t)| + \frac{Vm}{Vc}(1 - \sin^2(\omega t))\right] = \cos(\omega t) \cdot \left[1 - \frac{2Vm}{Vc}\sin(\omega t)\right] \quad \cdots(22)$$

[0113] In this case, $x = Vc/(2 \cdot Vm)$. For example, in the above-mentioned example, it is understood that the maximum value of the DC voltage Vdc that is constant is approximately 0.96 Vm because Vc = 1.5 Vm. Formula (15) reveals that the DC current Idc is $0.96/\sqrt{2}$ times the crest value Im.

[0114] The adoption of a distribution ratio 1/2 as described above can fix the respective duties in accordance with Formulas (11), (12), and (13) and set the DC voltage Vdc constant. Moreover, it is revealed that by reducing the zero duty dz, the voltage utilization ratio R is $\alpha/(1+\alpha \cdot \alpha/4)$ (α = Vc/Vm: hereinafter referred to as a "voltage ratio α") in Formula (21) by setting $x = Vc/(2 \cdot Vm)$.

[0115] The voltage utilization ratio $R=\alpha/(1+\alpha \cdot \alpha/4)$ is greater than the voltage utilization

[0138] During the period in which the zero duty dz is positive, for the first component drec·Vrec, a difference between the first component drec·Vrec obtained in the first modification of rectifying duty and the first component drec·Vrec obtained in the second modification of rectifying duty is small because the rectified voltage Vrec is also small. A difference in the DC voltage Vdc determined by Formula (14) is also small.

[0139] Even when the rectifying duty drec is set in the second modification of rectifying duty using the quantities used to obtain FIG. 7, a difference in waveform that is shown in the middle tier of FIG. 7 is not visually confirmed.

[0140] The DC voltage Vdc obtained by Formula (14) will now be described. Focusing on the second correction value of the rectifying duty drec being (1 - dc), from Formula (14), the DC voltage Vdc is calculated by Formula (23) below.

[0141]

$$\begin{aligned} Vdc &= (1-dc)\cdot Vrec + dc\cdot Vc \\ &= Vm\cdot|\sin(\omega t)| + \frac{Vm}{Vc}\cos^2(\omega t)\cdot(Vc - Vm\cdot|\sin(\omega t)|) \\ &= Vm\cdot|\sin(\omega t)| + Vm\cdot\cos^2(\omega t) - \frac{Vm^2}{Vc}\cos^2(\omega t)\cdot|\sin(\omega t)| \\ &= Vm + Vm\cdot|\sin(\omega t)|\cdot(1-|\sin(\omega t)| - \frac{1}{\alpha}\cos^2(\omega t)) \qquad \cdots(23) \end{aligned}$$

[0142] From the function form of Formula (23), an average value of the DC voltage Vdc is obtained by substituting a value $\pi/4$ into the phase ωt in Formula (23). For example, if 1.17 is adopted as the voltage ratio α, Vdc $\approx$ 0.952 Vm. An average voltage utilization ratio R is thus 0.952, revealing that it is higher than R = 0.87 shown in FIG. 5.

[0143] The conceivable reason why the voltage utilization ratio R can be increased as described above is that the pulsations of the DC voltage Vdc are allowed. Then, the behavior of the pulsations will be considered. A pulsating component ΔV of the DC voltage Vdc is expressed by Formula (24) below.

[0144]

$$\Delta V = Vdc - Vm$$
$$= Vm \cdot |\sin(\omega t)| \cdot (1 - |\sin(\omega t)| - \frac{1}{\alpha}\cos^2(\omega t)) \quad \ldots(24)$$

[0145] As described above, the voltage ratio α is desirably smaller in view of the breakdown voltage of the capacitor C4, and thus, the voltage ratio α is approximated to 1. Formula (24) is approximated by Formula (25) below.

[0146]

$$\Delta V \approx Vm \cdot |\sin(\omega t)| \cdot (-|\sin(\omega t)| + \sin^2(\omega t))$$
$$= Vm \cdot \frac{1 - \cos(2\omega t)}{2}(|\sin(\omega t)| - 1) \qquad \ldots(25)$$

[0147] Further, the approximate expression of Formula (26) is introduced.

[0148]

$$|\sin(\omega t)| \approx \sin^2(\omega t) \quad \ldots(26)$$

[0149] The pulsating component ΔV is thus approximated by Formula (27) from Formulas (25) and (26).

[0150]

$$\Delta V \approx Vm \cdot \frac{1 - \cos(2\omega t)}{2} \cdot (-1) \cdot \frac{1 + \cos(2\omega t)}{2}$$
$$= -\frac{Vm}{4} \cdot (1 - \cos^2(\omega t)) = \frac{Vm}{4} \cdot (\cos(4\omega t) - 1) \qquad \ldots(27)$$

[0151] It is revealed that the DC voltage Vdc pulsates at a frequency four times the frequency (hereinafter referred to as a "power supply frequency") of the single-phase AC voltage Vin in this manner.

[0152] FIGs. 9 and 10 are graphs showing the validity of the approximation from Formula (25) to Formula (27). In FIGs. 9 and 10, a waveform G1 indicates a function (1/2)(1-cos(2ωt)). In FIG. 9, a waveform G2 indicates a function (|sin(ωt)|-1), and a waveform G3 indicates a function (1/2)(1-cos(2ωt)) · (|sin(ωt)|-1). In FIG. 10, a

CLAIMS

1. A power converter comprising:

a DC link including a first power supply line and a second power supply line;

a converter that receives a single-phase AC voltage and outputs a pulsating power to said DC link;

an inverter that receives a power from said DC link and outputs an AC current ; and

a power buffer circuit that receives a charge power from said DC link and outputs a discharge power to said DC link,

wherein

an input power input to said inverter takes a value obtained, from said DC link, by subtracting said charge power from a sum of said pulsating power and said discharge power,

said charge power takes a value that is a half of said pulsating power,

said discharge power takes a value obtained by adding said charge power to an AC component of said pulsating power,

said converter applies a rectified voltage obtained by full-wave rectifying said single-phase AC voltage to said DC link while setting said first power supply line to have a higher potential than said second power supply line,

said power buffer circuit includes

a discharge circuit including a capacitor and a switch connected in series to said capacitor adjacent to said first power supply line between

said first power supply line and said second power supply line, and

a charge circuit that charges said capacitor,

a discharge duty that is a duty at which said switch is conductive takes a value obtained by dividing a product of a crest value of said single-phase AC voltage and a square of a cosine value of a phase of said single-phase AC voltage by a both-end voltage across said capacitor,

said converter is conductive at a rectifying duty, and

a DC voltage that is a sum of a product of said rectified voltage and said rectifying duty and a product of said both-end voltage and said discharge duty varies in a period that is a half of a period of said single-phase AC voltage.

2. The power converter according to claim 1, wherein said rectifying duty takes any one smaller value of an absolute value of a sine value of said phase and a value obtained by subtracting said discharge duty from 1.

3. The power converter according to claim 1, wherein said rectifying duty takes a value obtained by subtracting said discharge duty from 1.

4. The power converter according to any one of claims 1 to 3, wherein a ratio of said both-end voltage to said crest value is 1 or more and 1.2 or less.

5. The power converter according to any one of claims 1 to 3, wherein said inverter performs DC-AC conversion with a minimum value of said DC voltage as an upper limit.

6. The power converter according to claim 4, wherein said inverter performs DC-AC conversion with a minimum value of said DC voltage as an upper limit.

7. The power converter according to any one of claims 1 to 3, wherein said DC voltage varies with a quarter of said period of said single-phase AC voltage as a fundamental period.

8. The power converter according to claim 4, wherein said DC voltage varies with a quarter of said period of said single-phase AC voltage as a fundamental period.

9. The power converter according to any one of claims 1 to 3, wherein said DC voltage varies in a pair of sections that are not adjacent to each other among sections equally dividing said period of said single-phase AC voltage into four and is constant in the other pair of sections.

10. The power converter according to claim 4, wherein said DC voltage varies in a pair of sections that are not adjacent to each other among sections equally dividing said period of said single-phase AC voltage into four and is constant in the other pair of sections.