WHAT IS CLAIMED IS:

1. A memory controller configured to control a memory device, the memory controller comprising:

processing circuitry configured to,

translate, based on a first address translation scheme, a first address received from a host processor into a second address associated with the memory device, the first address translation scheme selected from among a plurality of address translation schemes based on memory resource utilization, and

evaluate the memory resource utilization of each of the plurality of address translation schemes based on a plurality of memory addresses generated using the plurality of address translation schemes such that the processing circuitry evaluates the memory resource utilization of each of the plurality of address translation schemes while translating the first address into the second address based on the first address translation scheme.

2. The memory controller of claim 1, wherein the processing circuitry is configured to calculate the memory resource utilization based on at least two of a first evaluation value, a second evaluation value, and a third evaluation value, and wherein

the first evaluation value, the second evaluation value, and the third evaluation value are calculated based on rank selection, bank selection, and row selection of the plurality of memory addresses, respectively, in each of the plurality of address translation schemes.

3. The memory controller of claim 2, wherein the processing circuitry is configured to calculate the memory resource utilization based on a sum of a first value and a second value, wherein

the first value is obtained by applying a first weight to the first evaluation value, and the second value is obtained by applying a second weight to the second evaluation value, the first weight being greater than the second weight.

4. The memory controller of any one of claims 1 to 3, wherein the processing circuitry is configured to,

evaluate the memory resource utilization of each of the plurality of address translation schemes during a first period associated with the first address translation scheme, and

perform the address translation based on a second address translation scheme during a second period, the second address translation scheme being selected based on the memory resource utilization of each of the plurality of address translation schemes calculated during the first period.

5. The memory controller of claim 4, wherein the processing circuitry is configured to change the address translation scheme from the first address translation scheme to the second address translation scheme in response to a reboot of the memory controller after the first period.

6. The memory controller of claim 4, wherein the processing circuitry is configured to change the address translation scheme from the first address translation scheme into the second address translation scheme in response to entering an idle period after the first period.

7. The memory controller of claim 1, wherein the processing circuitry is configured to,

perform the address translation using different address translation schemes to generate the plurality of memory addresses,

generate count values by counting ranks, banks, and rows associated with the plurality of memory addresses, the ranks, the banks, and the rows being selected by the plurality of memory addresses, and

calculate a utilization score indicating the memory resource utilization based on the count values.

8. The memory controller of claim 7, wherein the processing circuitry is configured to count the ranks, the banks, and the rows with respect to N memory addresses, where N is an integer of at least 2.

9. The memory controller of any one of claims 1 to 8, wherein the processing circuitry is configured to perform machine learning based on a plurality of first addresses to derive the plurality of address translation schemes time-sequentially, the plurality of first addresses being received from the host processor.

10. The memory controller of claim 9, wherein the processing circuitry is configured to derive the plurality of address translation schemes based on a change pattern of bits included in the plurality of first addresses.

11. An application processor comprising:

a host processor configured to provide an access request and a first address; and

a memory controller configured to,

perform address translation to translate, based on a first address translation scheme selected from a plurality of address translation schemes, the first address into a second address associated with a memory address,

calculate a resource utilization score indicating memory resource utilization of each of the plurality of address translation schemes while performing the address translation based on the first address translation scheme during a first time period, and

perform the address translation to translate, based on a second address translation scheme, the first address into the second address during a second time period such that the memory resource utilization of the second address translation scheme is highest among the plurality of address translation schemes during the first time period, the second time period being after the first time period.

12. The application processor of claim 11, wherein the memory controller is configured to,

recalculate the resource utilization score of each of the plurality of address translation schemes during the second time period, and

perform the address translation based on a third address translation scheme during a third time period after the second time period such that the memory resource utilization of the third address translation scheme is highest among the plurality of address translation

schemes during the second time period, the third time period being after the second time period.

13. The application processor of claim 11 or claim 12, wherein the memory controller is configured to calculate the resource utilization score of the plurality of address translation schemes based on a plurality of memory addresses generated according to the plurality of address translation schemes.

14. The application processor of any one of claims 11 to 13, wherein the memory controller is configured to calculate the resource utilization score based on a first evaluation value calculated according to rank selection, a second evaluation value calculated according to bank selection, and a third evaluation value calculated according to row selection.

15. The application processor of claim 11, wherein the memory controller is configured to,

perform the address translation using different ones of the plurality of address translation schemes to generate a plurality of memory addresses; and

calculate the resource utilization score of each of the plurality of address translation schemes based on the plurality of memory addresses.

16. The application processor of claim 15, wherein the memory controller is configured to,

generate count values by counting ranks, banks, and rows selected based on the plurality of memory addresses; and

calculate the resource utilization score based on the count values.

17. The application processor of any one of claims 11 to 16, wherein the memory controller is configured to,

compare resource utilization scores calculated with respect to the plurality of address translation schemes, and

select the second address translation scheme based on the resource utilization scores such that the memory resource utilization of the second address translation scheme is highest among the plurality of address translation schemes.

18. The application processor of any one of claims 11 to 17, wherein information indicating that the memory resource utilization of the second address translation scheme among the plurality of address translation schemes is highest is stored in a storage device, and

the memory controller is configured to change from the first address translation scheme to the second address translation scheme based on the information loaded from the storage device at reboot after the first time period.

19. A method of operating a memory controller to translate a system address to a memory address associated with a memory device, the method comprising:

translating the system address into the memory address based on a first address translation scheme selected from among a plurality of translation scheme candidates;

calculating resource utilization scores of each of the plurality of translation scheme candidates while translating the system address into the memory address based on the first address translation scheme;

selecting a next address translation scheme having highest resource utilization from the plurality of translation scheme candidates based on the resource utilization scores calculated while translating the system address into the memory address based on the first address translation scheme;

changing the address translation scheme to the next address translation scheme; and

translating the system address into the memory address based on the next address translation scheme.

20. The method of claim 19, wherein the calculating of the resource utilization score comprises:

generating a plurality of memory address candidates corresponding to a plurality of system addresses based on each of the plurality of translation scheme candidates;

generating a monitoring result by monitoring a change in memory resources associated with different ones of the plurality of memory address candidates; and

calculating the resource utilization score based on the monitoring result.