OPTICAL MULTI-DIE INTERCONNECT BRIDGE (OMIB)

Cross References

[0001] This application claims priority to U.S. provisional patent application serial no. 63/448,585, entitled "Optical, Multi-Die Interconnect Bridge (OMIB)", filed on February 27, 2023; U.S. provisional patent application serial no. 63/420,330, entitled "Thermally Stable Optical Modulation Elements Coupled to Electronic Elements", filed on October 28, 2022; and U.S. provisional patent application serial no. 63/321,453, entitled "Photonic Memory Fabric for System Memory Interconnection", filed on March 18, 2022. These priority applications are hereby incorporated by reference, as if set forth in full in this specification.

[0002] Each publication, patent, and/or patent application mentioned in this specification is herein incorporated by reference in its entirety to the same extent as if each individual publication and/or patent application was specifically and individually indicated to be incorporated by reference.

Background

Technical Field

[0003] The disclosed implementations relate generally to devices and methods used in interconnecting semiconductor dies, and in particular to those for optical interconnection using integrated circuits and/or external chiplets.

Context

[0004] The subject matter discussed in this section should not be assumed to be prior art merely as a result of its mention in this section. Similarly, a problem mentioned in this section or associated with the subject matter provided as background should not be assumed to have been previously recognized in the prior art. The subject matter in this section merely represents different approaches, which in and of themselves can also correspond to implementations of the claimed technology.

[0005] Integrated circuits (ICs) with processors, especially those for executing artificial intelligence and machine learning functions, move large amounts of data among one or more processor ICs and one or more memory ICs. Chiplets may aid in the interconnection of processor dies, memory dies, and other circuits to increase the bandwidth, and decrease the latency and power dissipated in the process.

Summary

[0006] Processing an AI workload often uses specialized hardware. Typical hardware bridges two chips with an electrical interconnect. The electrical interconnect consumes high power, has pin count limitations, and can only bring data to the edge of the chip. When the memory is in a central region of the chip it requires extra distance for signals to travel every time the memory is accessed by a processor sending a request to the edge of the chip from outside the chip. This is highly inefficient and makes it difficult for AI computing hardware to keep up with the demands required by an AI application.

[0007] In a first aspect, an implementation provides a package that includes a bridging element, a first unidirectional photonic path, and a second unidirectional photonic path. The bridging element includes a first interconnect region and a second interconnect region, both configured to electrically connect with one or more dies. The unidirectional photonic paths couple in opposite directions between the two interconnect regions. Third and fourth unidirectional photonic paths may couple two ways between the first interconnect region and an optical interface (OI). A first portion of a photonic transceiver may be coupled with the first interconnect region to send a first optical signal via the first unidirectional photonic path and receive a second optical signal via the second unidirectional photonic path. It may further be configured to send a third optical signal via the third unidirectional photonic path and receive a fourth optical signal via the fourth unidirectional photonic path. The first portion of the photonic transceiver may reside in a photonic integrated circuit (PIC) and a second portion of the photonic transceiver may reside in an electric integrated circuit (EIC). The first and the second portions may be coupled via an electrical interconnect less than 2 mm in length. The modulator may be an electro-absorption modulator fabricated with germanium, silicon, an alloy of germanium, an alloy of silicon, a III-V material based on indium phosphide (InP), or a III-V material based on gallium arsenide (GaAs). The EIC may include two or more compute elements around a central region. The second portion is proximate to one of the compute elements.

[0008] A further understanding of the nature and the advantages of particular implementations disclosed herein may be realized by reference of the remaining portions of the specification and the attached drawings.

Brief Description of the Drawings

[0009] The invention will be described with reference to the drawings, in which:

[0010] FIG. 1 is a top view of a wafer and a die that may include, or be included in, one or more microelectronic packages with an OMIB, in accordance with various implementations.

[0011] FIG. 2 shows an example OMIB with two dies it is bridging.

[0012] FIG. 3 shows an example package that die two dies can be coupled with via electrical interconnects.

[0013] FIG. 4 shows an example package that two dies can be coupled with via electrical interconnects.

[0014] FIGS. 5A-E show example packages that use a light engine to provide an optical signal for use by the photonic network.

[0015] FIG. 6 shows a perspective view of an example OMIB that bridges two dies and that is coupled with a light engine.

[0016] FIG. 7A shows a perspective view of an example OMIB that bridges two dies and that receives unmodulated light from a chiplet light engine (CLE).

[0017] FIG. 7B shows an example package that can use a CLE.

[0018] FIG. 8A is a diagram illustrating an example OMIB having photonic links capable of connecting two dies within a package, according to some implementations.

[0019] FIG. 8B shows one implementation having two OMIBs coupled between a first die and a second die.

[0020] FIG. 9 is a diagram illustrating an example system of a link that uses WDM for communication from a die to an external device, according to some implementations.

[0021] FIG. 10 illustrates an example reverse channel for the WDM system in FIG. 9, according to some implementations.

[0022] FIG. 11 illustrates an example unidirectional logical channel that comprises multiple photonic links.

[0023] FIG. 12 illustrates transfer of an example message of eight words in the unidirectional logical channel of FIG. 11.

[0024] FIG. 13 shows example AMS blocks in more detail.

[0025] FIG. 14A shows an arrangement of three OMIBs bridging a portion of two dies.

[0026] FIG. 14B shows an example arrangement of five dies being bridged by OMIBs.

[0027] FIG. 14C shows an example arrangement of dies being bridged by both OMIBs and electrical bridges.

[0028] FIG. 14D shows an example offset checkerboard of OMIBs bridging dies in two dimensions.

[0029] FIG. 15 is a flowchart showing example method of fabricating an OMIB according to various implementations.

[0030] FIG. 16 illustrates components of an example system in which one or OMIBs may be used.

[0031] FIGS. 17A-D illustrate examples of EIC/OMIB combinations that employ temperature compensation to widen the temperature range of the modulators in the OMIB.

[0032] FIG. 18 illustrates an example method 1800 of fabricating a system.

[0033] In the figures, like reference numbers may indicate functionally similar elements. The systems and methods illustrated in the figures, and described in the Detailed Description below, may be arranged and designed in a wide variety of different implementations. Neither the figures nor the Detailed Description are intended to limit the scope as claimed. Instead, they merely represent examples of different implementations of the invention.

Detailed Description

[0034] Processing an AI workload often uses specialized hardware. Typical hardware bridges two chips with an electrical interconnect. The electrical interconnect consumes high power, has pin count limitations, and can only bring data to the edge of the chip. When the memory is in a central region of the chip it requires extra distance for signals to travel every time the memory is accessed by a processor sending a request to the edge of the chip from outside the chip. This is highly inefficient and makes it difficult for AI computing hardware to keep up with the demands required by an AI application.

[0035] This document discloses an optical multi-die interconnect bridging element (OMIB). OMIBs can be used as bridges between semiconductor dies, e.g., electrical integrated circuits (EICs). A bridge can include the OMIB alone, or in combination with a substrate that is coupled to the OMIB or that has the OMIB embedded within it. The use of OMIBs for multi-die processing systems solves many of the problems associated with processing an AI workload, including latency, power, and bandwidth. A photonic receiver may comprise two portions, for example a first portion in the OMIB, including a modulator and/or a photodetector, and a second portion in the EIC, including an AMS block as described later herein.

[0036] In various arrangements, the OMIB can transmit or receive a photonic signal to transport data. A memory, such as a cache, can be positioned at a central region of the EIC die within two millimeters (2 mm) from an AMS block, such that the photonic transceiver in the OMIB is proximate to an edge of the memory directly above or below the portion of the die where the edge of the memory is positioned. The central region may intersect the center of the EIC die. Compute elements such as central processing units (CPUs), graphic processing units (GPUs),

tensor processing units (TPUs) can also be beneficially arranged at the central region of the die within two millimeters (2 mm) of where the photonic transceivers are positioned, or in a spatial association with the memory. Photonic ICs have avoided reaching the center of the die of connecting chips because of the heat produced by the connecting chips. Photonic chips may have a limited temperature range in which modulators perform within specifications. One reason an OMIB in the disclosed technology can reach the center of the die is that it uses temperature-stabilized modulators as described in U.S. provisional patent application serial no. 63/420,330, entitled "Thermally Stable Optical Modulation Elements Coupled to Electronic Elements."

[0037] As a result, the OMIB is faster and uses less power when compared to a traditional system. Latency is improved by carrying the data photonically to the point of compute rather than to the edge of the die. This allows the die to save electrical pipeline stages and also utilizes less electrical connections to carry the data from the edge of the chip to the interior where the memory is located. The electrical movement of the data from the edge of the die to the interior requires a path for the data that is slower and more power hungry. If an exemplary system is used to train an AI model, the benefit of moving the data photonically to the point of compute is repeated continuously, resulting in substantial savings and/or enabling the feasibility of these types of complex AI systems.

Terminology

[0038] The description may use perspective-based descriptions such as top/bottom, in/out, over/under, and the like. Such descriptions are merely used to facilitate the discussion and are not intended to restrict the application of implementations described herein to any particular orientation.

[0039] As used herein, the phrase "one of" should be interpreted to mean exactly one of the listed items. For example, the phrase "one of A, B, and C" should be interpreted to mean any of: only A, only B, or only C.

[0040] As used herein, the phrases "at least one of" and "one or more of" should be interpreted to mean one or more items. For example, the phrase "at least one of A, B, and C" or the phrase "at least one of A, B, or C" should be interpreted to mean any combination of A, B, and/or C.

[0041] Unless otherwise specified, the use of ordinal adjectives "first", "second", "third", etc., to describe an object, merely refers to different instances or classes of the object and does not imply any ranking or sequence.

[0042] The term "coupled" is used in an operational sense and is not limited to a direct or an indirect coupling. "Coupled to" is generally used in the sense of directly coupled, whereas

"coupled with" is generally used in the sense of directly or indirectly coupled. "Coupled" in an electronic system may refer to a configuration that allows a flow of information, signals, data, or physical quantities such as electrons between two elements coupled to or coupled with each other. In some cases, the flow may be unidirectional, in other cases the flow may be bidirectional or multidirectional. Coupling may be galvanic (in this context meaning that a direct electrical connection exists), capacitive, inductive, electromagnetic, optical, or through any other process allowed by physics.

[0043] The term "connected" is used to indicate a direct connection, such as electrical, optical, electromagnetic, or mechanical, between the things that are connected, without any intervening things or devices.

[0044] The term "configured to" perform a task or tasks is a broad recitation of structure generally meaning "having circuitry that" performs the task or tasks during operation. As such, the described item can be configured to perform the task even when the unit/circuit/component is not currently on or active. In general, the circuitry that forms the structure corresponding to "configured to" may include hardware circuits, and may further be controlled by switches, fuses, bond wires, metal masks, firmware, and/or software. Similarly, various items may be described as performing a task or tasks, for convenience in the description. Such descriptions should be interpreted as including the phrase "configured to."

[0045] As used herein, the term "based on" is used to describe one or more factors that affect a determination. This term does not foreclose the possibility that additional factors may affect the determination. That is, a determination may be solely based on specified factors or based on the specified factors as well as other, unspecified factors. Consider the phrase "determine A based on B." This phrase specifies that B is a factor that is used to determine A or that affects the determination of A. This phrase does not foreclose that the determination of A may also be based on some other factor, such as C. This phrase is also intended to cover an implementation in which A is determined based solely on B. The phrase "based on" is thus synonymous with the phrase "based at least in part on."

[0046] A "processor" includes any suitable hardware system, mechanism or component that processes data, signals or other information. A processor can include a system with a general-purpose central processing unit, multiple processing units, dedicated circuitry for achieving functionality, or other systems. Examples of processing systems can include servers, clients, end user devices, routers, switches, networked storage, etc. A "computer" may be any processor in communication with a memory. The memory may be any suitable processor-readable storage medium, such as random-access memory (RAM), read-only memory (ROM), magnetic or optical disk, or other tangible media suitable for storing instructions for execution by the processor.

[0047] The terms "substantially", "close", approximately", "near", and "about" refer to being within minus or plus 10% of an indicated value, unless explicitly specified otherwise.

[0048] The following terms or acronyms used herein are defined at least in part as follows:

[0049] **AI** - artificial intelligence

[0050] **AMS** - analog/mixed-signal

[0051] **BGA** - ball-grid array

[0052] A **channel** is one or more lanes that may be bonded together.

[0053] **Chiplet** - an integrated circuit with simple or specialized functionality to be used in combination with other ICs or chiplets in a multi-chip assembly.

[0054] **CLE** - chiplet light engine

[0055] **CPU** - central processing unit

[0056] **CW** - continuous wave

[0057] **DDR** memory - double-data rate memory

[0058] **DFB** - distributed fiber Bragg

[0059] **DIMM** - dual in-line memory module

[0060] **DRV** – driver. In some embodiments, the driver is a photonic-integrated circuit (PIC) or a electronic-integrated circuit (EIC)

[0061] **DSP** - digital signal processor

[0062] **EAM** - electro-absorption modulator

[0063] **EIC** - electronic integrated circuit

[0064] **EW** - evanescent wave

[0065] **FAU** - fiber array unit

[0066] **FBG** - fiber Bragg grating

[0067] **FPGA** - field-programmable gate array

[0068] **GC** - grating coupler - a coupling between an optical fiber and an on-chip photonic waveguide.

[0069] **GPU** - graphic processing unit

[0070] **GRIN** lens - graded index lens

[0071] **HBM** - high-bandwidth memory

[0072] **IC** - integrated circuit – a monolithically integrated circuit, i.e., a single semiconductor die which may be delivered as a bare die or as a packaged circuit. For the purposes of this document, the term integrated circuit also includes packaged circuits that include multiple semiconductor dies, stacked dies, or multiple-die substrates. Such constructions are now common in the industry, produced by the same supply chains, and for the average user often indistinguishable from monolithic circuits.

[0073] A **lane** includes a serializer, a link, and a deserializer.

[0074] **LED** - light emitting diode

[0075] **LDSU** - load/store unit

[0076] A **link** in the context of this patent document is the combination of a modulator, a photonic path (in an optical transmission medium), and a photodetector.

[0077] **LGA** - land grid array

[0078] **ML** - machine learning

[0079] **MLA** - micro-lens array

[0080] **MOD** – modulator

[0081] **MZI** - Mach-Zehnder interferometer

[0082] **OI** - optical interface—an interface that uses any means for optical interfacing between a fiber and a photonic IC.

[0083] **OMIB** - optical multi-die interconnect bridge

[0084] **PCB** - printed circuit board

[0085] **PCIe** - PCI express – a high-speed serial computer expansion bus.

[0086] **PCM** - phase-change memory

[0087] **PD** - photo detector, for example a photo diode.

[0088] **PGA** - pin-grid array

[0089] **PIC** - photonic integrated circuit

[0090] **QR** - quick response

[0091] A **processing device**, **processor**, **compute device**, or **compute element** may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0092] **RAM** - random access memory. Some types are static RAM (SRAM), dynamic RAM (DRAM), magnetic RAM (MRAM), resistive RAM (RRAM), conductive bridging RAM (CBRAM), etc.

[0093] **RDL** - redistribution layer - an extra metal layer on an IC to make bondpads available at other locations of the die.

[0094] **SCM** - storage-class memory

[0095] **SLD** - superluminiscent diode

[0096] **SSD** - solid-state drive

[0097] **SOA** - semiconductor optical amplifier

[0098] **TPU** - tensor processing unit

[0099] **UCIe** - Universal Chiplet Interconnect Express - an open specification for a die-to-die interconnect and serial bus between chiplets.

[0100] **VCSEL** - vertical-cavity surface-emitting lasers

[0101] A **waveguide** is an implementation of a unidirectional photonic path in an optical transmission medium.

[0102] **WDM** - wavelength division multiplexing.

Implementations

[0103] Implementations herein relate to resolving power, latency, or pin-count concerns by providing various OMIB configurations and various packages that include at least one OMIB. FIG. 1 is a top view of a wafer 100 and die 102 that may include, or be included in, one or more microelectronic packages with an OMIB, in accordance with various implementations. The wafer 100 may be composed of semiconductor material and may include one or more dies 102 having IC structures formed on a surface of the wafer 100. Each of the dies 102 may be a unit of a semiconductor product that includes a suitable IC. After the fabrication of the semiconductor product is complete, the wafer 100 may undergo a singulation process in which the dies are separated from one another to provide discrete "chips" of the semiconductor product. Die 102, and at least one other die, may be included in a microelectronic package with an OMIB.

[0104] The OMIB can be formed in a second process using a second wafer (not shown) in a manner analogous to the fabrication of the die 102. The OMIB is a photonic integrated circuit (PIC) and has optical components fabricated therein, as opposed to the die 102 which is an electronic integrated circuit (EIC) and typically has electronic elements fabricated therein. The OMIB can be embedded into a package substrate. The package substrate may be considered to

be a cored or coreless substrate. The package substrate may include one or more layers of a dielectric material which may be organic or inorganic. The package substrate may further include one or more conductive elements such as vias, pads, traces, microstrips, strip lines, and the like. The conductive elements may be internal to, or on the surface of, the package substrate. Generally, the conductive elements may allow for the routing of signals through the package substrate or between elements coupled to the package substrate. In some implementations the package substrate may be, for example, a printed circuit board (PCB), an interposer, a motherboard, or some other type of substrate.

[0105] FIG. 2 shows an example OMIB with two dies it is bridging. The OMIB 200 formed in the second stage of the fabrication process may share a dimension with each die 102 (horizontal or vertical) that was formed in the first stage of the fabrication process. The die may be as large as possible within the size limits of a reticle that is used to manufacture it. In FIG. 2, the dies 102 have a width that corresponds to the maximum reticle width MRW1 of an EIC reticle and a height that corresponds to the maximum reticle height MRH1 of an EIC reticle, and the OMIB 200 has a width that corresponds to the maximum reticle width MRW2 of a PIC reticle. This may be for convenience and cost-savings during the fabrication and is not limiting on various implementations.

[0106] In some implementations, the wafer 100 or the die 102 may include a memory device, a compute device, or both (examples include, but are not limited to, a random-access memory (RAM) device, (such as a static RAM (SRAM) device, a magnetic RAM (MRAM) device, a resistive RAM (RRAM) device, or a conductive-bridging RAM (CBRAM) device), a logic device (e.g., an AND, OR, NAND, NOR, or EXOR gate), a NAND flash memory, a solid-state drive (SSD) memory, a NOR flash memory, a CMOS memory, a thin film transistor-based memory, a phase-change memory (PCM), a storage class memory (SCM), a magneto-resistive memory (MRAM), a resistive RAM, a DRAM, a high bandwidth memory (HBM), a DDR-based DRAM, a DIMM memory, a CPU, a GPU, an MPU, a tensor engine, a load/store unit (LDSU), a neural compute engine, a dot-product and/or convolution engine, a field-programmable gate array (FPGA), an AI accelerator, or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 102. For example, die 102 may include a memory comprising multiple memory arrays, one or more processors, other logic, communication circuits, and power management functions, and execute instructions stored in the memory array, or otherwise interact with the memory array using the processors on die 102.

[0107] FIG. 3 shows an example package 300 that die 310 and die 320 can be coupled with via electrical interconnects. The package 300 includes OMIB 330 acting as a bridge between die 310 and die 320. An optional substrate 340 has been coupled to OMIB 330 such that OMIB 330 is embedded in the substrate 340. Although shown as flush in FIG. 3, OMIB 330 may not be flush

with the surface of the substrate 340, but rather may at least partially protrude from substrate 340 or be embedded in an inner layer of substrate 340. Various of the elements depicted may be at the surface of, or at least partially protruding from, OMIB 330 or dies 310 and/or 320. Additionally, the specific number of elements, the number of interconnects, dies, and other devices, may be different in other implementations. In some implementations, the package may include an adhesive, a sealant, an underfill, a mold, an overmold, or some other structural or dielectric material. In some implementations, certain elements may be positioned at a different location within a signal path relative to other elements. An optical interface (OI) 350 is included on a surface of the OMIB 330. Optical interface 350 may couple with a light engine 370 to receive unmodulated light through fiber(s) 360, and/or with an external device optical interface to exchange modulated and/or unmodulated light in either direction. Additional to optical interface 350, there may be one or more electrical interfaces on the surface of OMIB 330 to interface with external electrical devices.

[0108] Various implementations can use different types of light engines. The light engine can be external or integrated into the OMIB. Example implementations can use the following light engines to bring an optical signal to and from a package that includes OMIB 330: laser diodes—these are highly coherent light sources that produce a narrow beam of light, and that are widely used in photonic chips for data communication and sensing applications; light-emitting diodes (LEDs)—a type of diode that emits light when a current passes through it (they are low-cost, compact, and have a long lifetime, making them a popular choice for photonic chips); superluminescent diodes (SLDs)—SLDs are similar to LEDs, but they emit a wider, broadband light spectrum (SLDs are used for applications such as optical amplification, wavelength division multiplexing, and fiber optic sensing); vertical-cavity surface-emitting lasers (VCSELs)—these are lasers that emit light perpendicular to the chip surface, making them ideal for applications in photonics (VCSELs are widely used in data communication and sensing applications, such as 3D sensing, LiDAR, and data center interconnects); and silicon photonics—devices that use the light-carrying properties of silicon to produce light sources on silicon chips (silicon photonics has the potential to revolutionize photonics by reducing the size, cost, and power consumption of photonic components). These are some of the most commonly used light sources with a package that includes an OMIB 330. The choice of light engine depends on the specific requirements of the implementation, such as wavelength, power, and modulation speed.

[0109] The light engine may be located locally on OMIB 330 or connect to OMIB 330 via fiber 360. When integrated onto the PIC, distributed fiber Bragg (DFB) lasers or quantum dot lasers can be attached during processing or integrated in the native technology where possible. When remote, any packaged continuous wave (CW) laser suitable in power and spectrum for the

modulation technology may be used. In one implementation, the light source is a set of DFB lasers attached to a silicon interposer and connected to the PIC via optical fibers.

[0110] The optical interface 350 is used to terminate optical fibers at the edge or the top of OMIB 330 for optical input and/or output to occur from external processes or devices that are communicatively coupled to package 300 via the fibers. The choice of OI depends on the specific requirements of the implementation, such as the wavelength of light, the coupling efficiency, and the cost. Optical interface 350, and any other optical interfaces in and on OMIB 330, can include any means for optical interfacing between a fiber and a photonic IC, for example: an edge coupler; a grating coupler (CG); a graded index (GRIN) lens coupler, a fiber Bragg grating (FBG) coupler, a micro-lens array (MLA) coupler, an evanescent wave (EW) coupler, an adiabatic coupler, a wavelength division multiplexing (WDM) coupler, a prism coupler, a butt coupler, an end-fire coupler, and a V-groove coupler.

[0111] In one implementation, optical interface 350 includes a fiber array unit (FAU) to connect the OMIB optically to a light source and/or an optical I/O unit. The FAU is a device used in optical communication systems that combines or separates optical signals from multiple fibers into a single optical signal or multiple optical signals, respectively. The FAU can be used for a variety of applications, such as wavelength division multiplexing (WDM), parallel optical interconnects, and optical sensing. There are two main types of fiber array units that can be used: linear and circular. Linear FAUs combine or separate optical signals along a straight line, while circular fiber array units combine or separate optical signals in a circular configuration. Both types of fiber array units are typically made from a precision-molded optical plastic or ceramic material and can have anywhere from a few to hundreds of fibers arranged in a specific pattern. The choice of FAU depends on the specific requirements of an application, such as the number of fibers, the arrangement of the fibers, the wavelength of light being used, and the coupling efficiency desired. Each die can have an associated analog/mixed-signal (AMS) block associated with a portion of the OMIB it is coupled to and one or more transistors or supporting circuitry to route electrical signals to the transistors, or some other IC component.

[0112] OMIB 330 may further include one or more electrical interfaces (EIs). OIs and EIs may be affixed to a surface of the OMIB, either between the bridged dies 102 or offset in a region in the x or y direction where a die 102 does not extend. The EI has a function analogous to the OI, except it gives the OMIB the capability to transmit data to and from the dies via electrical connections instead of optical ones and can connect the external I/O block to the OMIB, for instance, via a wire from the EI to the external I/O block. Different types of electrical connections are possible including wires, RDLs and the like. The electrical connection typically transmits and receives data electrically across the electrical interconnection using known standards or bus protocols between the EI and any of the dies bridged by the OMIB or the EI and the external I/O

block. The electrical pathways between the EI and the dies can be routed through the OMIB, through the substrate, or both (or in the case of an RDL through one of the layers of the OMIB and/or substrate).

[0113] FIG. 4 shows an example package 400 that die 410 and die 420 can be coupled with via electrical interconnects. Package 400 is similar to package 300 of FIG. 3, with like element numbering, in addition to which it shows a first photonic transceiver 432 and second photonic transceiver 434. A portion of the first transceiver 432 is in die 410 and a portion of the second photonic transceiver 434 is in die 420. Another portion of first transceiver 432 is in OMIB 430, and another portion of second transceiver 434 is in OMIB 430. FIG. 4 shows bidirectional photonic paths 481, 482, and 483. Bidirectional photonic path 483 connects first photonic transceiver 432 and second photonic transceiver 434. Bidirectional photonic path 483 can include two or more unidirectional photonic paths in opposite directions to create a bidirectional path between the two transceivers to enable optical communication and/or data movement across the photonic channel in both directions between the two dies 410 and 420. Bidirectional photonic path 481 links photonic transceiver 432 to optical interface 450, and bidirectional photonic path 482 links photonic transceiver 434 to optical interface 450. Optical interface 450 is coupled with light engine 470 via fiber(s) 460. Bidirectional photonic paths 481-483 may form a photonic network inside OMIB 430. Optical interface 450 may include any means for interfacing between a fiber and a photonic IC. Substrate 440 is optional.

[0114] A photonic path may be implemented in an optical transmission medium. The optical transmission medium may include a waveguide on a PIC, an optical fiber or other optical transmission medium (such as free space optics or glass-etched waveguide), or some combination of the foregoing. Examples of optical modulators include, but are not limited to, electro-absorption modulators (EAMs), micro-ring resonators, or any suitable optical component with sufficient thermal stability.

[0115] FIGS. 5A-E show example packages that use a light engine to provide an optical signal for use by the photonic network. The light engine can include a laser diode, optics, and/or control electronics. The laser diode is the source of the laser light, and the optics are used to shape and control the output of the laser. Control electronics (not drawn) provide the necessary power and modulation to the laser diode to generate the desired output. In the implementations of FIGS. 5A-E, the light engine provides an optical signal through an optical interface such as an FAU and a GC, to a splitter, a modulator (MOD) abutting an AMS block in a first die, and finally to a photo detector (PD) abutting the AMS block of a second die. Where the laser is in a chiplet light engine (as will be described with reference to FIG. 7A), an FAU is not needed, and light can be guided directly into the GC. The photonic networks in the OMIBs of FIGS. 5A-E enable multiple

optical paths. Although FIGS. 5A-E show a GC and FAU jointly forming an optical interface, implementations may use any means for interfacing between a fiber and a photonic IC.

[0116] FIG. 5A shows an example 500 of intra-OMIB connections, illustrating the optical paths starting at the light engine 570. FIG. 5A includes first die 510, divided in a general part 510B that may include various processing, storage, and communication functions, and an AMS part 510A that includes analog/mixed-signal circuits for interfacing with OMIB 530. It further includes an optional substrate 540 and light engine 570. AMS part 510A of first die 510 may include a driver (DRV1) and a transimpedance amplifier (TIA1). AMS part 520A of second die 520 may include a driver (DRV2) and a transimpedance amplifier (TIA2).

[0117] Light engine 570 transmits light via the fiber array unit FAU and grating coupler GC (or any other OI configured to receive light on an OI input and to pass the received light on an OI output) into splitter SP inside OMIB 530. Splitter SP distributes the light over two different photonic paths 531 and 532 towards modulator MOD1 and modulator MOD2. In some implementations, the splitter, or a splitter tree, distributes the light over more than two different photonic paths to feed additional modulators. A photonic path may be implemented with any suitable optical transmission medium, and may include a mixture of waveguides and fibers.

[0118] Modulator MOD1 modulates the light it receives from the splitter SP with information from driver DRV1, and transmit the modulated light to photodetector PD2 via photonic path 533. Photodetector PD2 converts the received light to an electrical signal for second die 520. Modulator MOD2 modulates light it receives from the splitter SP with information from driver DRV2, and transmit the modulated light to photodetector PD1 via photonic path 534. Photodetector PD1 converts the received light to an electrical signal for first die 510. Jointly with a serializer (not shown) in first die 510, driver DRV1, transimpedance amplifier TIA2, and a deserializer (not shown) in second die 520, modulator MOD1, photonic path 533, and photodetector PD1 form a data channel from first die 510 to second die 520.

[0119] OMIB 530, a photonic IC, includes a first interconnect region, a second interconnect region, and an offset region. The first interconnect region includes a bondpad pattern located over MOD1 and PD1 that matches a bondpad pattern on first die 510 located under DRV1 and TIA1, or is otherwise configured to form an electrical interconnection between the respective components. The second interconnect region includes a bondpad pattern located over PD2 and MOD2 that matches a bondpad pattern on second die 520 located under TIA2 and DRV2, or is otherwise configured to form an electrical interconnection between the respective components. The offset region, which is further illustrated in FIG. 6, includes optical interfaces such as GC/FAU. Two or more bondpads of the bondpad pattern on first die 510 are physically and electrically coupled with two or more bondpads of the bondpad pattern in the first interconnect region, and

two or more bondpads on the bondpad pattern on the second integrated circuit are physically and electrically coupled with two or more bondpads of the bondpad pattern in the second interconnect region. One or more of the two or more bondpads on first die 510 may be located more than 100 microns (100 µm) from the edge of first die 510. One or more of the two or more bondpads on second die 520 may be located more than 100 microns (100 µm) from the edge of second die 520. The distance between the (lower) surface of first die 510 and the (top) surface of OMIB 530 is less than 2 mm and in many cases less than 50 microns. The distance between the (lower) surface of second die 520 and the (top) surface of OMIB 530 is less than 2 mm and in many cases less than 50 microns.

[0120] FIG. 5B shows the same example, illustrating only the signal path. Paths for unmodulated light have been omitted. FIG. 5B shows one signal path in bold lines as follows. Interface I/F1 in first die 510 delivers a digital signal carrying information to be transmitted from general part 510B of first die 510 to driver DRV1. Driver DRV1 converts the digital signal to an analog electrical signal suitable for driving a photonic modulator and delivers the analog electrical signal to modulator MOD1 in OMIB 530. Modulator MOD1 sends light modulated with the information to be transmitted to photodetector PD2 via photonic path 533. Photodetector PD2 converts the modulated light to a current signal, and delivers the current signal to transimpedance amplifier TIA2, which amplifies the signal and converts it to a voltage signal for suitable for digital interface I/F2. Interface I/F2 converts the voltage to a digital signal suitable for processing in general part 520B of second die 520. Similarly, information to be transmitted from general part 520B of second die 520 to general part 510B of first die 510 travels via I/F2, DRV2, MOD2, photonic path 534, photodetector PD1, transimpedance amplifier TIA1, and interface I/F1.

[0121] Photonic paths 533 and 534 include waveguides or other suitable optical transmission media to carry the optical signals from a modulator to a photodetector. The modulators in OMIB 530 are coupled with drivers in the AMS parts of the first or second die via a copper pillar or other suitable electrical interconnect. The photodetectors in OMIB 530 are coupled with transimpedance amplifiers in the AMS parts of the first or second die via a copper pillar or other suitable electrical interconnect. Photonic paths in OMIB 530 may be unidirectional, so that a pair of photonic paths in opposite directions can be comprised in a single bidirectional information channel.

[0122] An electrical interconnect is shown as making a coupling (or abutted coupling) between elements in the AMS parts and the corresponding elements in OMIB 530. In one implementation, the interconnect is a copper pillar no longer than 2 millimeters. In other implementations, the electrical interconnects can be solder bumps that are formed of a material such as tin, silver, or copper. If solder bumps are used for the interconnects, then the solder bumps may be flip-chip bumps. In yet other implementations, the interconnects may be elements

of a ball-grid array (BGA), pins of a pin grid array (PGA), elements of a land grid array (LGA), or some other type of interconnect. Generally, the interconnects may physically and electrically couple the AMS blocks to OMIB 530. For example, one or more of the interconnects may physically couple with, and allow electrical signals to pass between, pads of the dies and pads of substrate 540 and/or OMIB 530. The interconnects 525 may not have a uniform size, shape, or pitch. A finer pitch of interconnects may be desirable to allow a denser communication pathway between elements coupled to the OMIB. In implementations, the size, shape, pitch, or type of one or more of the interconnects may be different than depicted in the figures, or different than others of the interconnects. The specific type, size, shape, or pitch of the interconnects may be based on one or more factors such as use case, materials used, design considerations, and manufacturing considerations.

[0123] FIG. 5C shows an example of inter-OMIB connections. Paths for unmodulated light have been omitted. First die 510 and second die 520 can photonically communicate with external device optical interface 571 with OMIB 580 and fibers 561. For example, first die 510 may transmit to external device optical interface 571 via I/F1, DRV1, MOD1, photonic path 581, optional multiplexer MUX (in case wavelength division multiplexing is desired), GC, FAU, and fibers 561. Conversely, first die 510 may receive from external device optical interface 571 via fibers 561, FAU, GC, photonic path 583, optional demultiplexer DEMUX (in case wavelength division multiplexing is desired), PD1, TIA1, and I/F1.

[0124] FIG. 5D shows an example of a stacked-dies arrangement. The AMS circuits (DRV1 and TIA1) are included in a first AMS die 511A, and general/digital circuits are included in a first general die 511B. First AMS die 511A is stacked on top of OMIB 580 via electrical interconnects 526A, and first general die 511B is stacked on top of first AMS die 511A via electrical interconnects 526B. OMIB 580 interfaces with light engine 570 and/or external device optical interface 571 via fibers 560, and may further interface with a second die 520.

[0125] FIG. 5E shows an arrangement where the first general die 512B and the first AMS die 512A are separately stacked on OMIB 590 and positioned side by side. An electrical inter-connection such as a bus enables signals to and from first general die 512B and the first AMS die 512A (e.g., using UCIe, PCIe, or any suitable protocol). The electrical interconnection may include an electrical path 527A from TIA1 to I/F1, and an electrical path 527B from I/F1 to DRV1.

[0126] FIG. 6 shows a perspective view 600 of an example OMIB 630 that bridges two dies (first die 610 and second die 620) and that is coupled with a light engine 670. Substrate 640 is optional. First die 610 and second die 620 each have an AMS block (first AMS part 610A and second AMS part 620A) in a region that overlaps OMIB 630 such that the AMS blocks abut OMIB 630 and/or are stacked on OMIB 630 in a configuration that couples first die 610 with OMIB 630

via an electrical interconnect, and that also couples second die 620 with OMID 630. The interconnect could be made with a copper pillar or any other suitable electrical interconnect. An offset portion of the OMIB creates an offset region where the OI and/or the external light engine 670 can be positioned. External light engine 670 provides a light source for the photonic network via the OI. An external device optical interface 671 provides bidirectional communication with the dies via fibers between the OI and external device optical interface 671. In FIG. 6, the top surface of OMIB 630 and substrate 640 are shown as being substantially co-planar, although as previously stated, OMIB 630 is not required to be flush with the surface of substrate 640. The bottom surface of first die 610 or second die 620 may be physically and electrically coupled with the top surface of OMIB 630. If the first portion of the transceiver (modulator and/or PD in OMIB 630) line up with the second portion of the transceiver (the AMS part 610A or AMS part 620A), then OMIB 630 and first die 610 or second die 620 form an abutted coupling.

[0127] FIG. 7A shows a perspective view of an example OMIB 730 that bridges two dies and that receives unmodulated light from a chiplet light engine (CLE). Substrate 740 is optional. First die 710 and second die 720 each include an AMS block (710A, 720A) in a region that overlaps OMIB 730 such that the AMS blocks are above OMIB 730 and/or stacked on OMIB 730 in a configuration that couples the two dies to OMIB 730 via suitable electrical interconnects (e.g., where a modulator is positioned directly over a driver and a TIA is positioned directly over a PD). The CLE is positioned in the offset region of OMIB 730. The CLE includes a laser that may be positioned in parallel with the surface of OMIB 730, a first optical component (for example, a mirror 701 to reflect the laser beam downwards or to a side), and a second optical component (for example, a lens 702 to focus the laser beam onto a smaller area), wherein the first optical component, and a second optical component may be configured to turn the light substantially ninety (90) degrees to enable the light from the laser to be directed into the OMIB. Inside the OMIB, the light may enter a GC that also includes a ninety-degree mirror, so that the light may enter a waveguide that runs parallel to the surface of the OMIB. An external device optical interface 771 communicates bidirectionally with the dies via fibers between the OI and external device optical interface 771.

[0128] FIG. 7B shows an example package 700 that can use a CLE 775. Substrate 741 is optional. An optical signal is provided through the OMIB 731 from CLE 775 to a grating coupler CG1 (or any other means of interfacing between a fiber and a photonic IC) and splitter SP, from where it is guided first die 711 and second die 721. OMIB 731 also provides optical paths in both directions between the dies. A second grating coupler CG2 and an FAU, or other relevant fiber connector using any other means of interfacing between a fiber and a photonic IC, can provide access from and to external device optical interface 771. In some implementations, CLE 775 may

be included in a CLE array. In further implementations, CLE 775 may include a semiconductor optical amplifier (SOA) or an SOA array to amplify the power of the unmodulated light.

[0129] FIG. 8A is a diagram illustrating an example OMIB 830 having photonic links capable of connecting two dies within a package, according to some implementations. OMIB 830 provides optical communication from each modulator (MOD1-4) in first die 810 to each photodetector (PD1-4) in second die 820. A waveguide system in the OMIB can bridge and/or enable a connection between a transmit unit (not shown) in a first die 810 and a receive unit (not shown) in a second die 820. A light engine 870, which can be internal or external to OMIB 830, outputs carrier light at a single wavelength λa1. A splitter tree SPT may divide the light, having wavelength λa1, over multiple optical paths (four have been drawn) leading to the modulators MOD1-4. The modulators modulate the light having the single wavelength λa1 and transmit the modulated light via respective waveguides to photodetectors PD1-4. FIG. 8A shows four links, each including a modulator, a photonic path, and a photodetector. Each link may be part of a lane, which further includes a serializer and a deserializer. Multiple lanes may be bonded together in a single channel, which may be unidirectional or bidirectional.

[0130] FIG. 8B shows one implementation having two OMIBs 831 and 832 coupled between first die 811 and second die 821. A light engine 870 outputs carrier light to a splitter tree SPT, which may divide the light between multiple optical paths leading to the modulators MOD1-4 associated with one or more photonic channels. For example, a first bidirectional photonic channel may include the links MOD1/PD1 and MOD2/PD2, and a second bidirectional photonic channel may include the links MOD3/PD3 and MOD4/PD4.

[0131] FIG. 9 is a diagram illustrating an example system of a link that uses WDM for communication from a die to an external device, according to some implementations. In this example, first die 910 and external device are coupled through a grating coupler GC and an FAU (or any other means for optical interfacing between a fiber and a photonic IC) in the OMIB 930, an optical fiber 991, and external device optical interface 971.

[0132] A light engine 970, which can be internal or external, provides light of multiple wavelengths (e.g., between 2 and 16 wavelengths), such as four wavelengths λb1, λb2, λb3, λb4, as shown, to OMIB 930. A splitter tree SPT (e.g., similar to that of FIG. 8A) may divide the light at the multiple wavelengths between multiple different channels or different links (e.g., two links, where only one is fully shown), which may be in different OMIBs or different PICs. The carrier light at the wavelengths λb1, λb2, λb3, λb4 is provided to the optical modulators MOD1-4 which may modulate the four light beams with different parts of the information to be transmitted, and a WDM multiplexer (MUX) combines the four light beams into a single beam that includes the four

different wavelengths. The single beam of light is then transmitted to external device optical interface 971 via the GC, FAU and optical fiber 991.

[0133] FIG. 10 illustrates an example reverse channel for the WDM system in FIG. 9, according to some implementations. External device optical interface 971 provides an optical signal via the fiber 991, FAU, and GC to a WDM demultiplexer (DEMUX) in OMIB 930. The WDM demultiplexer separates the optical signal into four separate modulated signals having wavelength λb1, λb2, λb3, λb4. These four signals are provided, via respective optical waveguides, to photodetectors PD1-4, which interface electrically with first die 910 to provide the information from the external device to first die 910.

[0134] Although the implementation discussed above is directed to a photonic channel showing four optical links in one direction and a WDM multiplexer receiving four different wavelengths, in other implementations, two or more optical links and a WDM multiplexer receiving two or more different wavelengths may be used. The WDM demultiplexer would, accordingly, output two or more different wavelengths corresponding to these alternative implementations.

[0135] Using intra-OMIB and inter-OMIB photonic channels, e.g., as described above, generally including one or more links per direction, the processors in the EIC(s) in a single package can be connected into electro-photonic networks. The resulting network topology generally depends on the selection of pairs of dies that are coupled via an associated photonic channel; various example topologies are known in the art. Note that, while this document generally refers to bidirectional photonic channels, which, as compared with unidirectional photonic channels, result in network structures providing greater flexibility for implementing ML and other computational models, electro-photonic networks can in principle also be formed with unidirectional photonic channels, and such networks may retain any of the benefits discussed herein (e.g., power savings due to photonic data transfer over longer distances).

[0136] As previously stated, a photonic channel includes at least two unidirectional sets of one or more links, capable of making a bidirectional channel. Examples of such a channel include, but are not limited to, the photonic channel between two dies, when bridged by an OMIB and the photonic channel between an OI on an OMIB and an external device optical interface. The nature of the external device optical interface can vary so long as it has the optical capability to receive messages sent from the OMIB and/or send messages that can be received and used by the OMIB or any dies using the OMIB as a bridge.

[0137] The messages can be in the form of variably sized packets. FIG. 11 illustrates an example unidirectional logical channel 1100 that comprises multiple photonic links. Logical channel 1100 has an input link 1101, a transmit bonding engine 1102, photonic paths 1103A-D, a receive bonding engine 1104, and an output link 1105. The transmit bonding engine 1102 may

split incoming data packets across active photonic links and add sequence information. Receive bonding engine 1104 reassembles the data packets using the sequence information. In the depicted example, data arrives at the receive bonding engine on four links.

[0138] FIG. 12 illustrates transfer of an example message of eight words in the unidirectional logical channel 1100 of FIG. 11. The message comprises words W0-W7. Transmit bonding engine 1102 splits the words across four active photonic links. For example, a first link conveys words W0 and W4. A second link conveys words W1 and W5, and so on. Transmit bonding engine 1102 adds the sequence information to each of the partial messages and receive bonding engine 1104 reassembles the full message at its output. Bonding can allow construction of high-bandwidth, low-latency channels from multiple lower-bandwidth links, and may provide the ability to avoid non-working links.

[0139] FIG. 13 shows example AMS blocks in more detail. FIG. 13 shows an AMS transmit block 1310A for a first die and an AMS receive block 1320A for a second die. The AMS receive block 1315 for the first die and the AMS transmit block 1328 for the second die are not detailed to simplify the diagram. Each of the AMS blocks 1310A and 1320A can be connected to OMIB 1330 via one or more electrical interconnects (here only interconnects 1314 for AMS transmit block 1310A and 1321 for AMS receive block 1320A are shown). As shown in FIG. 13, each link in a photonic channel comprises an optical transmit unit Tx, an optical receive unit Rx, and an optical transmission medium (e.g., an optical waveguide or fiber) connecting the transmit unit to the receive unit, in this case AMS transmit block 1310A is coupled with AMS receive block 1320A and AMS transmit block 1335 is coupled with AMS receive block 1336. The transmit unit (e.g., transmit unit 1331) includes an optical modulator (e.g., modulator 1333) that imparts a message onto an optical signal by modulating carrier light output by a light engine 1370, and an electrical serializer (e.g., serializer 1313) that converts an electronic message received in the form of parallel data words into a signal suitable for driving the optical modulator. The receive unit (e.g., receive unit 1332) includes a photodetector (e.g., photodetector 1334) to convert the optical signal received via the transmission medium back to an electrical signal, and associated electronics including a transimpedance amplifier (e.g., TIA 1322) and gain control (e.g., gain control 1323) to normalize the signal level, a slicer (e.g., slicer 1324) to extract the bit-stream, and a de-serializer (e.g., de-serializer 1325) to convert the received message back into parallel data. AMS transmit block 1310A further includes a transmit bonding engine 1312 that can split messages from first interface 1311 as detailed with reference to FIG. 11, and AMS receive block 1320A includes a receive bonding engine 1326 to reassemble messages for second interface 1327 as detailed with reference to FIG. 12. OMIB 1330 may further include a receive block 1336 interfacing with AMS receive block 1315; a transmit block 1335 interfacing with AMS transmit block 1328; a light engine 1370; an optical interface OI1; and an optical interface OI2.

[0140] In one implementation, information is modulated at 56 Gb/s in a non-return-to-zero (NRZ) code, but more spectrally efficient modulation schemes such as PAM-4 or PAM-8 or higher-order pulse amplitude modulation may be used to allow higher-bandwidth and lower-latency links.

[0141] FIG. 14A shows an arrangement of three OMIBs bridging a portion of two dies. OMIB 1430A bridges two compute elements 1411 in first die 1410, a first part of central region 1412 in first die 1410, two compute elements 1421 in second die 1420, and a first part of memory region 1422 in second die 1420. OMIB 1430B bridges two compute elements 1421 in second die 1420 and a second part of memory region 1422 in second die 1420. OMIB 1430C bridges two compute elements 1411 in first die 1410, a second part of central region 1412 in first die 1410, two compute elements 1421 in second die 1420, and a third part of memory region 1422 in second die 1420. Central region 1412 is located centrally in first die 1410 to even out latencies between the compute elements 1411 and central region 1412. Central region 1412 may include memory, cache memory, other shared memories, a network on-chip crossbar, a switch, a routing mechanism, and memory controllers. Memory region 1422 is located centrally in second die 1420 to even out latencies between the compute elements 1421 and memory region 1422. Memory region 1422 may include cache memory, other shared memories, and memory controllers. The portions of the dies that the OMIBs bridge have 10 compute elements and two memory regions. Additional OMIBs (not shown) could be positioned on an opposite side of first die 1410 and second die 1420 to bridge to additional dies, compute elements, and parts of the memory regions. The arrangement enables a packet to be routed photonically from an external device optical interface 1471 to an AMS block proximate to the memory that is being utilized or accessed and proximate to the location where the compute element 1411 or 1421 can perform one or more computations on the data in the memory region. The capability of an OMIB to carry instructions from an arbitrary compute element or external device, for example to load or store data in the memory region 1422 and/or process the data with a compute element 1411 or 1421 that is proximate to the central region 1412 or the memory region 1422, using a packet that is carried as a photonic signal via the OMIB to the interior of one of the dies 1410 or 1420 addresses many of the problems of stranded memory and/or the latency introduced when an optical signal cannot extend beyond the edge of a die.

[0142] The AMS transmit and receive blocks can take an optical signal to the central region of either die (e.g., to a memory controller to access a memory in the central region) from any external device optical interface that is connected by an inter-OMIB link to the OMIB or from and AMS transmit and receive block that has an inter-OMIB connection within the bridge. The OI of each OMIB can also be connected by a fiber although this is not required. A first side of an AMS transmit block 1413 or an AMS receive block 1414 (e.g., the right side) is aligned with a first side (e.g., the right side) of the central region (e.g., central region 1412). The first side of the central

region being proximate and/or touching a compute element 1411 such as a CPU, GPU, TPU and the like. A second side of the AMS transmit block 1413 or an AMS receive block 1414 (e.g., the left side) is aligned with the left side of the OMIB. The alignment of the sides is approximate and need not be exact but typically the alignment is in at least two dimensions to allow for abutment between optical and electrical elements in the OMIB and AMS blocks respectively.

[0143] FIG. 14B shows an example arrangement of five dies 1430-1434 being bridged by OMIBs. Using this arrangement of package 1440, bridges can be added indefinitely in two dimensions as needed. In this configuration, each OMIB has two interconnect regions for attaching dies. An L2 cache or other memory region can be positioned and/or fabricated at a central portion of the die such that the memory region can be reached photonically at the interior of the die (rather than the edge), which results in less latency. It is also possible to provide optical channels among OMIBs, for example by linking two OMIBs via an optical fiber. An OI can be positioned in the offset region of an OMIB. The arrangement of FIG. 14B can be extended indefinitely in the x and y directions. Moreover, the arrangement of FIG. 14B allows routing through multiple hops in a diagonal direction thereby significantly further reducing the routing latency.

[0144] FIG. 14C shows an example arrangement of dies 1413-1417 being bridged by both OMIBs and electrical bridges 1419. In some implementations, an OMIB and an electrical bridge are combined in a single die.

[0145] As shown in the following, one OMIB can bridge four dies. For example, the OMIB is used to bridge dies both vertically and horizontally, which results in 4 interconnect regions on each OMIB to correspond to four AMS blocks on the respective dies. An OMIB in this arrangement may provide channels in six directions, including two horizontally, two vertically, and two diagonally.

[0146] FIG. 14D shows an example offset checkerboard of OMIBs bridging dies (1410, 1418) in two dimensions. Each OMIB has four interconnection regions and is capable of bridging four dies using six links (2 vertical, 2 horizontal, and 2 diagonal links), representing 6 intra-die connections on each OMIB. Some dies, e.g., die 1418, may include memory regions. AMS blocks can interface with the memory regions as well as with any processing elements and other logic. Note that FIG. 14D may not be to scale. OMIBs whose dimensions are similar to those of the dies being bridged can reach AMS blocks close to the center of the dies. Also, AMS blocks may be relatively much smaller than those shown in the example, and each die and each OMIB may have more than four interconnect regions.

[0147] FIG. 15 is a flowchart showing example method 1500 of fabricating an OMIB according to various implementations. Method 1500 comprises the following operations.

[0148] Operation 1510 – fabricating a bridge including a photonic link from a first interconnect region to a second interconnect region, wherein the photonic link includes a first electrical interconnect, a modulator coupled with the first electrical interconnect, an optical transmission medium coupled with the modulator, a photodetector coupled with the optical transmission medium, and a second electrical interconnect. In some implementations, the modulator is configured to be temperature stabilized by applying a stabilization voltage to the modulator, wherein the stabilization voltage is related to a die temperature, and wherein the stabilization voltage induces a change in an electrical absorption in the modulator.

[0149] Operation 1520 – positioning the interconnect regions to enable an electrical interconnect and/or abutted coupling to AMS blocks in the dies.

[0150] Operation 1530 – fabricating an intra-OMIB connection between the interconnect regions.

[0151] Operation 1540 – fabricating an inter-OMIB connection between the two interconnect regions and an optical interface.

[0152] FIG. 16 illustrates components of an example system 1600 in which one or OMIBs may be used. Each of the components, or group of components, may include AMS blocks and interfaces to couple with one or more OMIBs. For example, the system 1600 may include display device interface circuitry like connectors and drivers to which a display device 1606 may be coupled. In this case it is not necessary for a display device 1606 to be integrated into or be a component of the system 1600. Similarly, the system 1600 may not have an audio input device 1624 or an audio output device 1608 but may have audio input or output device interface circuitry, such as connectors and supporting circuitry, for coupling to an external audio input device or external audio output device.

[0153] System 1600 may include one or more processing devices 1602. Processing device 1602 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), tensor processing units (TPUs), AI accelerators, fixed-gate programmable arrays (FPGAs), load/ store units (LDSUs), neural compute engines (NCEs), dot-product and/or convolution engines, server processors, or any other suitable processing devices. System 1600 may include a memory 1604, which may itself include one or more memory devices such as volatile memory, nonvolatile memory, flash memory, solid state memory, and/or a hard drive, including but not limited to: a random-access memory (RAM) device, (such as static RAM (SRAM) device, a magnetic RAM (MRAM) device, a resistive RAM (RRAM) device, or a conductive-bridging RAM (CBRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), A NAND Flash memory, a solid-state drive (SSD) memory, a NOR Flash memory, a CMOS memory, a thin film transistor-based

memory, a phase change memory (PCM), a storage class memory (SCM), a magneto-resistive memory (MRAM), a resistive RAM, a DRAM, a high bandwidth memory (HBM), a DDR-based DRAM, a DIMM memory. In some implementations, the memory 1604 may include memory that shares a die with the processing device 1602. This memory may be used as cache memory and may include embedded dynamic RAM or spin transfer torque magnetic RAM.

[0154] In some implementations, system 1600 may include a communication chip 1612. For example, communication chip 1612 may be configured for managing wireless communications for the transfer of data to and from the device.

[0155] Communication chip 1612 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and / or revisions (e.g., advanced LTE project, ultra-mobile broadband (UMB) project (also referred to as "3GPP2"), and others). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. Communication chip 1612 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. Communication chip 1612 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). Communication chip 1612 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. Communication chip 1612 may operate in accordance with other wireless protocols in other implementations. System 1600 may include an antenna 1622 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0156] In some implementations, communication chip 1612 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet or USB). As noted above, the communication chip 1612 may include multiple communication chips. For instance, a first communication chip 1612 may be dedicated to shorter range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1612 may be dedicated to longer-range wireless communications such as EDGE, GPRS, CDMA,

WiMAX, LTE, EV-DO, or others. In some implementations, a first communication chip 1612 may be dedicated to wireless communications, and a second communication chip 1612 may be dedicated to wired communications.

[0157] System 1600 may include battery/power circuitry 1614. The battery power circuitry 1614 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of system 1600 to an external energy source (e.g., AC line power). System 1600 may include a display device 1606 (or corresponding interface circuitry, as discussed above). The display device 1606 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, a flat panel display, a virtual reality headset, an augmented reality headset, etc. System 1600 may include an audio output device 1608 (or corresponding interface circuitry, as discussed above). The audio output device 1608 may include any device that generates an audible indicator, such as speakers, headsets, earbuds, vibration elements, piezo crystals, etc. System 1600 may include an audio input device 1624 (or corresponding interface circuitry, as discussed above). The audio input device 1624 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a pickup or a musical instrument digital interface (MIDI) output).

[0158] System 1600 may include a positioning device 1618 (or corresponding interface circuitry), such as according to the global positioning system (GPS), Galileo, GLONASS, BeiDou, IRNSS, NavIC, and/or QZSS. The positioning device 1618 may be in communication with a satellite-based system and may receive a location of system 1600, as known in the art. System 1600 may include another output device 1610 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1610 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device. System 1600 may include another input device 1620 (or corresponding interface circuitry, as discussed above). Examples of another input device 1620 include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0159] System 1600 may have any desired form factor, such as a handheld or mobile device (e.g., a cell phone, a smartphone, a tablet computer, a laptop computer, an Internet-of-Things (IoT) device, a netbook computer, an ultrabook computer, a mobile internet device, a music player, a personal digital assistant (PDA), an ultra-mobile personal computer, and others), a desktop electrical device, a server device or other networked computing component, a printer, a scanner, a monitor, a settop box, an entertainment control unit, a vehicle control unit, a digital

camera, a digital video recorder, or a wearable electrical device. In some implementations, system 1600 may be any other electronic device that processes data.

Thermal Behavior

[0160] The close spacing and abutment of an EIC and a PIC chiplet (less than 2 millimeters and often within 50 microns) creates a thermal challenge for an OMIB. Depending on the type of modulators used, the temperature range for operation within specifications may be less than thirty degrees Celsius. However, the die temperature of an EIC can vary significantly more, dependent on the ambient temperature, load conditions, supply voltage, and other factors. Modulator types include Mach-Zehnder interferometer (MZI), ring modulator, and electro-absorption modulator (EAM). Ring modulators have a very narrow temperature range (less than one degree Celsius), whereas MZI and EAM may have an operating range of more than thirty degrees Celsius. Both the modulator temperature and bias voltage may affect the frequency (wavelength) at which the modulator's efficiency peaks. The laser's wavelength may be unaffected, or differently affected, by these parameters. Thus, a change in temperature will result in a difference between the laser wavelength and the modulator's efficiency peak wavelength, thus affecting the modulation depth.

[0161] Implementations may include modulators that are inherently optimal over a desired temperature range. Alternatively, an implementation may provide temperature compensation including a temperature sensing or predicting capability. The temperature compensation may be fully incorporated in the OMIB, or partially in the OMIB and partially in a connecting die.

[0162] FIGS. 17A-D illustrate examples of EIC/OMIB combinations that employ temperature compensation to widen the temperature range of the modulators in the OMIB. FIG. 17A shows an EIC 1710, physically and electrically coupled with a PIC 1720 (e.g., an OMIB) via metal interconnects such as bumps or copper pillars. EIC 1710 includes a driver DRV 1711, and a temperature element TE 1712. TE 1712 may include a temperature sensor, a temperature predictor, or both (a temperature predictor predicts die or PIC temperature based on a processor's load conditions known in its software or firmware). In some implementations, the temperature sensor is located less than two millimeters (2 mm) from DRV 1711. In further implementations, the temperature sensor is located less than fifty micron (50 μm) from DRV 1711. Driver DRV 1711 delivers a high-data rate modulation signal to modulator 1721 in PIC 1720. TE 1712 delivers a low-frequency (compared to the data rate) temperature-dependent bias voltage to MOD 1721. If the temperature dependency of the bias voltage inversely matches that of the modulator over an extended temperature range, it will cancel the effects of the temperature on the modulator performance in the extended temperature range. In further implementations, TE 1712 includes a lookup table to translate the measured or predicted temperature to a temperature-compensating modulator bias voltage.

[0163] In FIG. 17B, EIC 1730 is physically and electrically coupled with PIC 1740 (e.g., an OMIB). EIC 1730 includes driver DRV 1731, temperature element TE 1732, and adder 1733. PIC 1740 includes modulator MOD 1741. Adder 1733 adds the low-frequency temperature-dependent bias voltage from TE 1732 to the high-data rate modulation signal from DRV 1731, and forwards it to MOD 1741. In some implementations, TE 1732 includes a lookup table to translate the measured or predicted temperature to a temperature-compensating modulator bias voltage.

[0164] In FIG. 17C, EIC 1750 is physically and electrically coupled with PIC 1760 (e.g., an OMIB). EIC 1750 includes driver 1751, whereas PIC 1760 (e.g., an OMIB) includes modulator MOD 1761 and temperature sensor TS 1762. TS 1762 is located close to MOD 1761, and delivers a temperature-dependent bias voltage to MOD 1761. The temperature dependency of the bias voltage inversely matches that of the MOD 1761 over an extended temperature range, extending its operating temperature range.

[0165] In FIG. 17D, EIC 1770 is physically and electrically coupled with PIC 1780 (e.g., an OMIB). PIC 1780 includes modulator MOD 1781 and temperature sensor TS 1782. TS has a temperature sensor output configured to be coupled with a circuit external to PIC 1780 (e.g., EIC 1770). EIC 1770 includes driver DRV 1771, temperature controller TC 1772, and adder 1773. TC 1772 is configured to receive a first temperature-dependent signal from a circuit external to EIC 1770 (e.g., from TS 1782 in PIC 1780). TC 1772 converts the first temperature-dependent signal to a temperature-dependent bias voltage, whose temperature dependency inversely matches that of the MOD 1781 over an extended temperature range. TC 1772 may perform the conversion using temperature-linear and temperature-nonlinear analog circuits. Alternatively, or additionally, TC 1772 may perform the conversion using digital circuits to access a memory 1774 that stores a temperature profile. TC 1772 may be included in in temperature element TE, such as TE 1732 in FIG. 17B. In some implementations, TC 1772 includes a lookup table to translate the measured or predicted temperature to a temperature-compensating modulator bias voltage.

[0166] Some modulators can provide stable operation over a wide temperature range of modulation for optical components, for example when incorporated into an OMIB, even without the addition of temperature compensation. Modulators may utilize the Franz-Keldysh effect for electrically-induced changes in optical absorption. A variety of materials may be used in the modulators, including germanium and its alloys, silicon and its alloys, III-V materials, such as those based on indium phosphide (InP) or gallium arsenide (GaAs) material systems. For example, one or more implementations described herein involve chip hardware including features and functionality that provide a thermally stable optical modulation element(s) coupled to electronic element(s) (e.g., a driver in an AMS transmit block). In one or more implementations, the hardware is an apparatus that includes an electronic-integrated circuit (EIC) and a photonic-integrated circuit (PIC). The PIC may be electrically interconnected in a coupling or an abutted

coupling with the EIC. Each of the transmit units may include a thermally-stable optical modulator in a portion that resides in the PIC. The data may be moved optically in the PIC via an optical carrier between one of the thermally stable optical modulators in a first portion of the OMIB and one of the receive units in or interconnected with a second portion of the OMIB. In one or more implementations, a thermally stable optical modulator operates in a temperature range larger than thirty degrees Celsius. In this example, the thermally stable optical modulator may further include materials selected from a group including of germanium, silicon, an alloy of germanium, an alloy of silicon, a III-V material based on indium phosphide (InP), and a III-V material based on gallium arsenide (GaAs). In one or more implementations, the optical modulator is an electro-absorption modulator (EAM) which uses the Franz-Keldysh effect for an electrically induced charge in an optical absorption.

[0167] In one or more implementations, the thermally stable optical modulator is an EAM that operates in a temperature range smaller than thirty degrees Celsius. In this example, the thermally stable optical modulator may include (e.g., include of) materials selected from a group including germanium, silicon, an alloy of germanium, an alloy of silicon, a III-V material based on indium phosphide (InP), and a III-V material based on gallium arsenide (GaAs). In one or more implementations, the thermally stable optical modulator uses a quantum-confined stark effect (QCSE) for an electrically induced change in an optical absorption. In one or more implementations, the thermally stable optical modulator has an output that has a high optical modulation amplitude. In this example, the thermally stable optical modulator may include materials selected from a group including germanium, silicon, an alloy of germanium, an alloy of silicon, a III-V material based on indium phosphide (InP), and a III-V material based on gallium arsenide (GaAs). In one or more implementations, the thermally stable optical modulator uses a quantum confined stark effect (QCSE) for an electrically induced change in an optical absorption. In one or more implementations, the thermally stable optical modulator is configured for stable operation over a wide temperature range. In this example, the thermally stable optical modulator may include materials selected from the group including of germanium, silicon, an alloy of germanium, an alloy of silicon, a III-V material based on Indium Phosphide (InP), and a III-V material based on gallium arsenide (GaAs). In one or more implementations, the modulator uses a Franz-Keldysh effect for an electrically induced change in an optical absorption.

Fabrication

[0168] FIG. 18 illustrates an example method 1800 of fabricating a system. Method 1800 comprises Step 1810 which includes fabricating a system that includes a first die (integrated circuit), a second die (integrated circuit), a photonic IC that provides a bridge function, a light source, and a data channel. The photonic IC includes a first interconnect region, a second

interconnect region, and an offset region. A bondpad pattern on the first integrated circuit matches a bondpad pattern in the first interconnect region, and a bondpad pattern on the second integrated circuit matches a bondpad pattern in the second interconnect region. Two or more bondpads on the first integrated circuit are physically and electrically coupled with two or more bondpads in the first interconnect region, and two or more bondpads on the second integrated circuit are physically and electrically coupled with two or more bondpads in the second interconnect region. The light source is optically coupled with a first optical interface (a first OI) in the offset region. The data channel comprises a serializer and a driver in the first integrated circuit, a modulator, photonic path, and photodetector in the photonic IC, a transimpedance amplifier and a deserializer in the second integrated circuit. The distance between the surface of the first integrated circuit and the surface of the photonic IC is less than 2 mm, and the distance between the surface of the second integrated circuit and the surface of the photonic IC is less than 2 mm. In many cases, the distances are less than 50 microns (50 μm). At least one of the two or more bondpads on the first integrated circuit may be located more than 100 microns (100 μm) from the edge of the first integrated circuit. At least one of the two or more bondpads on the second integrated circuit may be located more than 100 microns (100 μm) from the edge of the second integrated circuit. The modulator can be an electro-absorption modulator (EAM). The modulator can be a Mach-Zehnder Interferometer (MZI). The first die or the photonic IC may include a temperature sensor or a temperature predictor that can deliver a temperature-dependent bias signal.

Considerations

[0169] Although the description has been described with respect to particular implementations thereof, these particular implementations are merely illustrative, and not restrictive. The description may reference specific structural implementations and methods, and does not intend to limit the technology to the specifically disclosed implementations and methods. The technology may be practiced using other features, elements, methods and implementations. Implementations are described to illustrate the present technology, not to limit its scope, which is defined by the claims. Those of ordinary skill in the art recognize a variety of equivalent variations on the description above.

[0170] For example, many examples in this document couple a fiber to a photonics IC using a grating coupler. However, many of the implementations work well using other means for optical interfacing between a fiber and a photonic IC, such as described with reference to FIG. 3. Although many examples show only an OMIB bridging a first die and a second die, an OMIB may bridge any number of dies. Although most examples show the AMS functions included in the first die and/or second die, the AMS functions may be partially or fully included in separately stacked

ICs, such as shown in FIGS. 5D-E. All such implementations are within the scope and ambit of the disclosed technology.

[0171] All features disclosed in the specification, including the claims, abstract, and drawings, and all the steps in any method or process disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive. Each feature disclosed in the specification, including the claims, abstract, and drawings, can be replaced by alternative features serving the same, equivalent, or similar purpose, unless expressly stated otherwise.

[0172] Although the description has been described with respect to particular implementations thereof, these particular implementations are merely illustrative, and not restrictive. For instance, many of the operations can be implemented on a printed circuit board (PCB) using off-the-shelf devices, in a System-on-Chip (SoC), application-specific integrated circuit (ASIC), programmable processor, a coarse-grained reconfigurable architecture (CGRA), or in a programmable logic device such as a field-programmable gate array (FPGA), obviating the need for at least part of any dedicated hardware. Implementations may be as a single chip, or as a multi-chip module (MCM) packaging multiple semiconductor dies in a single package. All such variations and modifications are to be considered within the ambit of the disclosed technology the nature of which is to be determined from the foregoing description.

[0173] Any suitable technology for manufacturing electronic devices can be used to implement the circuits of particular implementations, including CMOS, FinFET, BiCMOS, bipolar, JFET, MOS, NMOS, PMOS, HBT, MESFET, etc. Different semiconductor materials can be employed, such as silicon, germanium, SiGe, GaAs, InP, GaN, SiC, graphene, etc. Circuits may have single-ended or differential inputs, and single-ended or differential outputs. Terminals to circuits may function as inputs, outputs, both, or be in a high-impedance state, or they may function to receive supply power, a ground reference, a reference voltage, a reference current, or other. Although the physical processing of signals may be presented in a specific order, this order may be changed in different particular implementations. In some particular implementations, multiple elements, devices, or circuits shown as sequential in this specification can be operating in parallel.

[0174] Particular implementations may be implemented by using a programmed general-purpose digital computer, application-specific integrated circuits, programmable logic devices, field-programmable gate arrays, optical, chemical, biological, quantum or nanoengineered systems, etc. Other components and mechanisms may be used. In general, the functions of particular implementations can be achieved by any means as is known in the art. Distributed,

networked systems, components, and/or circuits can be used. Communication, or transfer, of data may be wired, wireless, or by any other means.

[0175] It will also be appreciated that one or more of the elements depicted in the drawings/figures can also be implemented in a more separated or integrated manner, or even removed or rendered as inoperable in certain cases, as is useful in accordance with a particular application.

[0176] Thus, while particular implementations have been described herein, latitudes of modification, various changes, and substitutions are intended in the foregoing disclosures, and it will be appreciated that in some instances some features of particular implementations will be employed without a corresponding use of other features without departing from the scope and spirit as set forth. Therefore, many modifications may be made to adapt a particular situation or material to the essential scope and spirit.

Claims

1. A bridging apparatus for optically joining a first die and a second die, comprising:

a bridge having first and second interconnect regions for electrical interconnection to the first and second dies respectively;

a first photonic path in the bridge from the first interconnect region to the second interconnect region;

a second photonic path in the bridge from the second interconnect region to the first interconnect region; and

a first portion of a photonic transceiver coupled with the first interconnect region to send a first optical signal via the first photonic path and receive a second optical signal via the second photonic path;

wherein:

the first portion of the photonic transceiver resides in a photonic integrated circuit (PIC) and a second portion of the photonic transceiver resides in an electric integrated circuit (EIC), the first and the second portions being coupled via an electrical interconnect less than 2 mm in length, and wherein:

the first portion of the photonic transceiver comprises a modulator or photodetector, and the second portion of the photonic transceiver comprises a serializer or deserializer.

2. The bridging apparatus of claim 1, wherein the first interconnect region includes bondpads arranged in a first bondpad pattern matching with bondpads arranged in a first corresponding bondpad pattern on the first die, and second interconnect region includes bondpads arranged in a second bondpad pattern matching with bondpads arranged in a second corresponding bondpad pattern on the second die.

3. The bridging apparatus of claim 1, further comprising one or more analog/mixed signal (AMS) blocks disposed on the bridge, the one or more AMS blocks each including a respective serializer and a deserializer for implementing data serialization and deserialization interfaces between the bridge and the first and second dies to be joined by the bridge, wherein the bridge

further comprises an electrical inter-connection providing a signal path between a corresponding AMS block and the first or second die, when joined by the bridge.

4. The bridging apparatus of claim 3, further comprising the first and second dies, the first and second dies being bonded and electrically coupled to the bridge.

5. The bridging apparatus of claim 3, wherein the first and second dies are each electrically connected to respective AMS blocks through electrical paths in the bridge.

6. The bridging apparatus of claim 3, further comprising the first and second dies and a first and a second AMS block, wherein the first and second AMS blocks are bonded and electrically coupled to the first die and the second die respectively.

7. The bridging apparatus of claim 6, wherein the first and second AMS blocks abut the first die and the second die respectively.

8. The bridging apparatus of claim 6, wherein the first and second die each have a respective central region, and the first and the second AMS blocks are bonded to the respective central regions of the first die and second die.

9. The bridging apparatus of claim 8, wherein a compute element is disposed around the central region of the first die.

10. The bridging apparatus of claim 8, wherein a memory region is disposed around the central region of the first die.

11. The bridging apparatus of claim 1, further comprising a photonic network, comprising the first and second photonics paths, and an edge coupler coupled to the photonic network, the edge coupler configured to provide an optical interface to one or more optical fibers.

12. The bridging apparatus of claim 11, wherein the photonic transceiver comprises a modulator, and further comprising a light engine, the light engine being external to the bridge and optically coupled to the one or more optical fibers, the light engine providing optical signals for transmission on the photonic network to the modulator.

13. The bridging apparatus of claim 1, wherein the photonic transceiver comprises a modulator, and further comprising a light engine integrated with the bridge and optically coupled to the modulator.

14. The bridging apparatus of claim 13, wherein the modulator is configured to modulate the optical signals provided by the light engine.

15. The bridging apparatus of claim 3, wherein the photonic transceiver comprises a modulator, and further comprising a modulator driver that is a part of the bridge and coupled to the modulator, wherein a corresponding AMS block is operable to provide a control signal to the modulator driver.

16. The bridging apparatus of claim 3, wherein the one or more AMS blocks are abutted to the bridge at a distance less than 50 microns.

17. The bridging apparatus of claim 3, wherein corresponding AMS blocks are respectively connectable to each of the first and second dies to be joined by the bridge using electrical interfaces supporting a communication protocol, wherein the communication protocol is UCIe (Universal Chiplet Interconnect Express) or PCIe (Peripheral Component Interconnect Express).

18. The bridging apparatus of claim 1, wherein the photonic transceiver comprises a modulator, the modulator comprising one or more of Mach-Zehnder interferometer, ring modulator, or micro-ring resonator.

19. The bridging apparatus of claim 5, wherein the photonic transceiver comprises a photodetector, and wherein the bridge further comprises photonic network, comprising the first and second photonics paths, and a multiplexer and a demultiplexer, the multiplexer being optical

coupled through the photonic network to the modulator, and further optically coupled through the photonic network to provide signals to an optical interface, wherein the multiplexer is configured to perform wavelength division multiplexing (WDM), and the demultiplexer being optically coupled through the photonic network to the photodetector, and further optically coupled through the photonic network to receive signals from the optical interface, wherein the demultiplexer is configured to demultiplex WDM-multiplexed signals.

20. The bridging apparatus of claim 19, further comprising a second modulator in the bridge, the second modulator optically coupled to the photonic network and electrically coupled to a corresponding AMS block, and wherein the multiplexer receives modulated signals from both the modulator and the second modulator.

21. The bridging apparatus of claim 1, wherein the modulator comprises a Mach-Zehnder interferometer in combination with a micro-ring resonator.