

Abstract of the Disclosure

A television receiver including a MPU (15) with OSD
circuitry (20) on a single chip. The OSD circuitry
5 includes multisystem detection circuitry (22) which
counts the number of horizontal lines between vertical
flyback pulses to determine the vertical frequency of the
received standard signal and measures the time of a
horizontal line using a fixed frequency signal to
10 determine the horizontal frequency of the received
standard signal and uses this information to control the
outputs of a PLL (21) to synchronize the receiver to the
received standard. The PLL includes a VCO (35) having a
constant offset current applied to the control terminal
15 to prevent alternating phases of the output control
signal from the loop phase detector (39), which
alternating phases cause jitter in the display.

(FIG. 3 accompanies this abstract)

This Sheet Has Been Replaced

