

MEMORY ARRAYS AND ASSOCIATED METHODS OF MANUFACTURING

TECHNICAL FIELD

[0001] The present technology is directed generally to memory arrays and associated methods of manufacturing.

BACKGROUND

[0002] Memory cells (e.g., floating-gate transistors or PCRAM cells) are typically arranged in an array connected to a grid formed by a plurality of Word lines and Bit lines. The Word lines are generally parallel to one another and perpendicular to the Bit lines. Each of the memory cells forms a node of the array, and each node is connected to a particular pair of Word lines and Bit lines. In operation, each memory cell may be individually accessed by energizing a particular pair of Word lines and Bit lines while floating or oppositely biasing the rest of the Word lines and Bit lines.

[0003] The conventional arrangement of the memory array, however, cannot accommodate more than one memory cell per node. If the memory array includes two memory cells per node that are connected to a pair of Word lines and Bit lines, energizing the pair of Word lines and Bit lines would simultaneously energize the two parallel memory cells. Thus, the two memory cells may not be individually addressed or accessed. Accordingly, certain improvements to the memory arrays may be needed to accommodate more than one memory cell per node.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1A is a schematic circuit diagram of a non-orthogonal memory array in accordance with embodiments of the technology.

[0005] Figure 1B is a schematic circuit diagram of a memory node in the non-orthogonal memory array of Figure 1A.

[0006] Figure 2 is a perspective view of one implementation of the non-orthogonal memory array in Figure 1 in accordance with embodiments of the technology.

[0007] Figure 3 is a top view of the non-orthogonal memory array in Figure 2 in accordance with embodiments of the technology.

[0008] Figure 4A is a perspective view of a two-cell memory sub-assembly useful for the non-orthogonal memory array in Figure 2 in accordance with embodiments of the technology.

[0009] Figure 4B is a cross-sectional view of another two-cell memory sub-assembly useful for the non-orthogonal memory array in Figure 2 in accordance with embodiments of the technology.

[0010] Figures 5A-5K are top and cross-sectional views of a portion of a substrate material undergoing a process useful for forming several embodiments of the non-orthogonal memory array of Figure 2 in accordance with embodiments of the technology.

[0011] Figure 6 is a schematic circuit diagram of an orthogonal memory array configured to accommodate multiple memory cells per node in accordance with other embodiments of the technology.

[0012] Figure 7 is a top view of one implementation of the orthogonal memory array in Figure 6 in accordance with embodiments of the technology.

[0013] Figures 8A-8F are top and cross-sectional views of a portion of a semiconductor substrate undergoing a process useful for forming several embodiments of the orthogonal memory array of Figure 7 in accordance with embodiments of the technology.

DETAILED DESCRIPTION

[0014] Several embodiments of the present technology are described below with reference to memory arrays and associated methods of manufacturing. Many details of certain embodiments are described below with reference to semiconductor substrates. The term "semiconductor substrate" is used throughout to include a variety of articles of manufacture, including, for example, individual integrated circuit dies, sensor dies, and/or dies having other semiconductor features. Several of the processes described below may be used to form memory arrays on a wafer or a portion of a wafer. The wafer or wafer portion (e.g., wafer form) can include an unsingulated wafer or wafer portion, or a repopulated carrier wafer. The repopulated

carrier wafer can include singulated elements (e.g., dies) surrounded by an adhesive material (e.g., a flexible adhesive) and a generally rigid frame. Many specific details of certain embodiments are set forth in Figures 1-8F and in the following text to provide a thorough understanding of these embodiments. Several other embodiments can have configurations, components, and/or processes different than those described in this disclosure. A person skilled in the relevant art, therefore, will appreciate that additional embodiments may be practiced without several of the details of the embodiments shown in Figures 1-8F.

[0015] Figure 1A is a schematic circuit diagram of a portion of a non-orthogonal memory array 100 in accordance with several embodiments of the technology, and Figure 1B is a schematic circuit diagram of a memory node 106 in the non-orthogonal memory array of Figure 1A. As used herein, the term "orthogonal" generally describes a positional relationship that is perpendicular. The term "non-orthogonal" generally describes a positional relationship that is oblique or canted. As shown in Figure 1, the memory array 100 can include a grid 101 and a plurality of memory nodes 106 carried by the grid 101. Even though only certain components of the memory array 100 are shown in Figure 1A, in certain embodiments the memory array 100 may also include peripheral circuits, registers, and/or other suitable components.

[0016] The grid 101 can include a plurality of contact lines 102 and a plurality of access lines 104. The contact lines 102 are generally parallel to one another, and the access lines 104 are generally parallel to one another. In the illustrated embodiment, the contact lines 102 include first to seventh contact lines 102a-102g, and the access lines 104 include first to fourth access lines 104a-104d. In other embodiments, the contact and access lines 102 and 104 may include a greater or smaller number of lines.

[0017] The contact and access lines 102 and 104 can be non-orthogonal relative to one another. In the illustrated embodiment, the individual contact and access lines 102 and 104 are at an angle α of about 63° . In other embodiments, the individual contact and access lines 102 and 104 can be at other suitable angles based on the dimensions and/or relative arrangements of the contact and access lines 102 and 104, as discussed in more detail below with reference to Figure 3. In further embodiments, the contact and access lines 102 and 104 can also be generally orthogonal while configured to accommodate the memory nodes 106 with two memory cells, as discussed in more detail below with reference to Figures 6-8F.

[0018] The memory nodes 106 are individually connected to the contact and access lines 102 and 104. As shown in Figure 1B, the individual memory nodes 106 can include a first rectifier 108a, a first memory cell 110a, a second memory cell 110b, and a second rectifier 108b connected to one another in series. The input terminals of the first and second rectifiers 108a and 108b form an input point 114 electrically coupled to a corresponding second access line 104. The output terminals of the first and second rectifiers 108a and 108b are electrically connected to the corresponding first and second memory cells 110a and 110b, respectively. In the illustrated embodiment, the first and second rectifiers 108a and 108b each include a diode. In other embodiments, the first and second rectifiers 108a and 108b can also include a bipolar transistor, a junction field effect transistor ("JFET"), a metal oxide field effect transistor ("MOSFET"), and/or other suitable types of rectifying device.

[0019] The first and second memory cells 110a and 110b (collectively referred to as "memory cells 110") can include any suitable memory cell configurations. For example, in a particular embodiment, the memory cells 110 can include a phase change random access memory ("PCRAM") component constructed from chalcogenide glass, as described in more detail below with reference to Figures 4A and 4B. In one embodiment, the PCRAM structure is switchable between two states. In other embodiments, the PCRAM structure may be switchable between four, eight, or another number of states. In further embodiments, the memory cells 110 can include a floating gate transistor and/or other suitable types of memory structures.

[0020] The memory nodes 106 can include a first output point 107a and a second output point 107b electrically connected to corresponding contact lines 102 (e.g., fourth and fifth contact lines 102d and 102e, respectively, as shown in Figure 1B) via optional third rectifiers 112. In the illustrated embodiment, the third rectifier 112 includes a diode. In other embodiments, the third rectifier 112 can also include a bipolar transistor, a JFET, a MOSFET, and/or other suitable types of rectifying device. In further embodiments, the third rectifier 112 may be omitted, and a direct electrical link (e.g., a metal trace, a metal wire, and/or other conductive coupler) may directly connect the output points 107a and 107b to the corresponding contact lines.

[0021] One feature of several embodiments of the memory array 100 is that the memory cells 110 in the memory nodes 106 are individually connected to different pairs of the contact and access lines 102 and 104 to form different circuits. For example, as shown in Figure 1B, the first memory cell 110a is connected between fourth access line 104d and the fifth contact line

102e forming a first circuit. The second memory cell 110b is connected to the fourth access line 104d and the fourth contact line 102d forming a second circuit. The first and second circuits are electrically isolated from each other.

[0022] The foregoing feature allows each of the memory cells 110 in the individual memory nodes 106 to be individually addressed or accessed. For example, the first and second memory cells 110a and 110b of the memory node 106 may be individually accessed by energizing (1) the fourth access line 104d and the fourth contact line 102d or (2) the fourth access line 104d and the fifth contact line 102e. As shown in Figure 1B, to access the first memory cell 110a, the fourth access line 104d and the fifth contact line 102e may be energized (e.g., by reversing the polarity relative to other access lines). As a result, electrical current may flow between the fourth access line 104d and the fifth contact line 102e via a path formed by the input point 114, the first rectifier 108a, the first memory cell 110a, the first output point 107a, and the optional third rectifier 112. Thus, the state and/or other information stored in the first memory cell 110a may be altered or accessed. While accessing the first memory cell 110a, the second memory cell 110b can retain its current state because the fourth contact line 102d is reversely biased or kept floating. After the first memory cell 110a is accessed, the second memory cell 110b may be accessed by energizing the fourth access line 104d and the fourth contact line 102d while reversely biasing or floating the fifth contact line 102e.

[0023] Figure 2 is a perspective view of one implementation of the non-orthogonal memory array 100 in Figure 1, and Figure 3 is a top view of the non-orthogonal memory array 100 in Figure 2 in accordance with embodiments of the technology. In Figures 2 and 3, inter-component insulation of the memory array 100 is removed for clarity.

[0024] Referring to both Figures 2 and 3 together, the memory array 100 can include a plurality of contact lines 102, a plurality of memory nodes 106 in direct contact with and stacked on the contact lines 102 via a plurality of conductive contacts 116, and a plurality of access lines 104 in direct contact with the memory nodes 106. The contact and access lines 102 and 104 can be at an angle α based on a first distance a between two adjacent contact lines 102 and a second distance b between two access lines 104. For example, the angle α may be determined according to the following formula:

$$\alpha = \arctan\left(\frac{b}{a}\right)$$

In other embodiments, the value of α may be determined based on other suitable dimensions and/or conditions.

[0025] The individual contact and access lines 102 and 104 can include a trace, a channel, and/or other suitable structure constructed from doped polysilicon, a metal, a metal alloy, and/or other suitable materials. The conductive contacts 116 can include a volume of a metal (e.g., copper, aluminum, or gold), a metal alloy (e.g., solder), and/or other suitable conductive materials. The memory nodes 106 can include two memory cells 110a and 110b, as described in more detail below with reference to Figures 4A and 4B. Even though the contact and access lines 102 and 104 are shown as having generally rectangular shapes, in other embodiments the contact and access lines 102 and 104 may include curves, apertures, steps, and/or other structural features.

[0026] Figure 4A is a perspective view of a two-cell memory node 106 useful for the non-orthogonal memory array 100 in Figure 2 in accordance with embodiments of the technology. As shown in Figure 4A, the memory node 106 includes a generally rectangular memory dielectric 130 having a first sidewall 132a, a second sidewall 132b, and a top wall 134 between the first and second sidewalls 132a and 132b. The memory dielectric 130 can include silicon dioxide, silicon nitride, and/or other suitable insulation materials.

[0027] The memory node 106 can also include a doped material 131 on the top wall 134 of the memory dielectric 130. In the illustrated embodiment, the doped material 131 includes a first N-type region 136a, a second N-type region 136b, and a P-type region 138 therebetween. The P-type region 138 is between the first and second N-type regions 136a and 136b to form two back-to-back P/N junctions as the first and second rectifiers 108a and 108b (Figure 1). Even though two N-type regions are illustrated in Figure 4A, in certain embodiments, the memory node 106 may include two P-type regions separated by one N-type region. In further embodiments, the memory node 106 may include other components and/or structures for forming a JFET, a MOSFET, and/or other suitable rectifiers.

[0028] The memory node 106 also includes a first memory structure 140a in direct contact with the first sidewall 132a, and a second memory structure 140b in direct contact with the second sidewall 132b. In one embodiment, the first and second memory structures 140a and 140b (collectively referred to as “memory structures 140”) can include a layer of chalcogenide

glass. In other embodiments, the memory structures 140 may include a floating gate transistor and/or other suitable materials and/or structures.

[0029] Even though the memory structures 140 are shown as being generally rectangular, in other embodiments, the memory structures 140 may have other configurations. For example, as shown in Figure 4B, the first and second memory structures 140a and 140b have an L shape and are in direct contact with an insulating material 142 (e.g., silicon oxide). In further embodiments, the memory structures 140 may have other suitable configurations.

[0030] Figures 5A-5K are top and cross-sectional views of a portion of a semiconductor substrate material 150 undergoing a process useful for forming several embodiments of the non-orthogonal memory array 100 of Figure 2 in accordance with embodiments of the technology. In the illustrated embodiment, the substrate material 150 includes a P-type dopant for illustration purposes. One of ordinary skill in the art would understand that the substrate material 150 may also include an N-type dopant or that it may be intrinsic (i.e., not doped).

[0031] Figures 5A and 5B are top and cross-sectional views of the substrate material 150 during an initial stage of the process in which the contact lines 102 are formed. As shown in Figures 5A and 5B, an N-type silicon material 151 can be blanket-deposited onto the substrate material 150 using chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), and/or another suitable technique, or may be formed by counterdoping the P-type silicon substrate.

[0032] Subsequently, a photoresist (not shown) may be deposited on the N-type silicon material 151 via spin coating or another suitable deposition technique. The photoresist may then be patterned to form a plurality of trenches. The term "patterning" as used hereinafter generally refers to the process of printing a desired pattern on a photoresist and subsequently removing certain portions of the photoresist to form the desired pattern in the photoresist using photolithography and/or another suitable technique.

[0033] With the patterned photoresist, portions of the N-type silicon material 151 may be removed to form first trenches 153. Suitable removal techniques can include wet etching, dry etching, reactive ion etching, and/or other suitable techniques. In the illustrated embodiment, the first trenches 153 extend through the N-type silicon material 151 into the substrate material 150. In other embodiments, the first trenches 153 extend through the N-type silicon material 151 to interface with the substrate material 150. In further embodiments, the first trenches 153

extend partially through the N-type silicon material 151 without reaching the substrate material 150.

[0034] After partially removing the N-type silicon material 151, the first trenches 153 may be filled with an insulation material to isolate the contact lines 102. For example, in one embodiment, a blanket insulation material 152 (e.g., silicon oxide) may be deposited onto the substrate material 150 and then removed to expose the top surface 151a of the N-type silicon material 151. Suitable removal techniques include chemical mechanical polishing, electro-chemical mechanical polishing, and/or other suitable techniques.

[0035] Figures 5C and 5D are top and cross-sectional views of the substrate material 150 during an optional stage of the process in which the optional third rectifiers 112 are formed. Referring to both Figures 5C and 5D, the third rectifiers 112 can be formed by first patterning the substrate material 150 with a photoresist (not shown) to identify the desired implantation areas. Then, a P-type dopant can be implanted using diffusion, ion implantation, and/or another suitable technique. In one embodiment, the P-type dopant can have a concentration higher than that of the substrate material 150. In other embodiments, the P-type dopant may have other desired concentrations.

[0036] Figures 5E and 5F are top and cross-sectional views of the substrate material 150 during another stage of the process in which the conductive contacts 116 are formed. Referring to both Figures 5E and 5F, a contact dielectric 156 can be deposited onto the substrate material 150. The contact dielectric 156 can then be patterned with a photoresist and partially removed to form a plurality of second trenches 157. In the illustrated embodiment, the second trenches 157 have a T shape with a first end 158a in direct contact with the optional third rectifier 112 and a second end 158b generally planar with the contact dielectric 156. In other embodiments, the second trenches 157 can have a rectangular, oval, partially spherical, and/or another suitable type of shape. After forming the second trenches 157, a conductive material 158 can be deposited onto the contact dielectric 156 and subsequently polished to fill the second trenches 157. The conductive material 158 can include tungsten, copper, aluminum, gold, and/or another suitable material.

[0037] Figures 5G and 5H are top and cross-sectional views of the substrate material 150 during another stage of the process in which a plurality of memory nodes 106 are formed. During this stage, the memory dielectric 130 and an N-type material 136 can be deposited in a

series onto a top surface 156a of the contact dielectric 156. Subsequently, the N-type material 136 may be patterned with a photoresist (not shown) and doped with a P-type dopant to form the P-type regions 138 between the first and second N-type regions 136a and 136b.

[0038] After forming the P-type regions 138, the process can then include patterning the N-type material 136 and removing portions of the N-type material 136 and the memory dielectric 130 to form columns 160 as shown in Figure 5G. Each of the columns 160 can have a first sidewall 160a, a second sidewall 160b, and a top wall 160c therebetween. The first and second sidewalls 160a and 160b individually correspond to a pair of adjacent conductive contacts 116.

[0039] Subsequently, a conformal memory structure 140 may be deposited on the columns 160 and the top surface 156a of the contact dielectric 156. Then, the memory structure 140 may be spacer etched and/or otherwise selectively removed to form the first and second memory structures 140a and 140b on the first and second sidewalls 160a and 160b of the columns 160, respectively. Then, the columns 160 may be patterned and etched to form individual memory nodes 106, as shown in Figure 5J.

[0040] Even though the foregoing description discusses forming the memory structures 140 as shown in Figure 4A, in certain embodiments, the process can include stages for forming the memory structures 140 as shown in Figure 4B. As shown in Figure 5I, the process can include depositing a conformal layer of the memory structure 140 onto the columns 160 and the top surface 156a of the contact dielectric 156. Then, the insulating material 142 may be deposited onto the memory structure 140 and polished to expose the columns 160. The insulating material 142 and the memory structure 140 can then be spacer-etched together to form L-shaped memory structures 140.

[0041] Figures 5J and 5K are top and cross-sectional views of the substrate material 150 during another stage of the process in which the access lines 104 are formed. As shown in Figure 5K, an access dielectric 162 may be deposited onto the contact dielectric 156 and the memory nodes 106 and polished to form a generally flat surface 162a. As shown in Figure 5J, the access dielectric 162 may be patterned and etched to form third trenches 164 exposing the P-type regions 138 of the individual memory nodes 106. Subsequently, a conductive material 166 (e.g., copper) can be deposited in the third trenches 164 and on the top surface 162a of the

access dielectric 162. The deposited conductive material 166 can then be polished such that only those portions in the third trenches 164 remain, thus forming the access lines 104.

[0042] Figure 6 is a schematic circuit diagram of a portion of an orthogonal memory array 200, and Figure 7 is a top view of one implementation of the memory array 200 in Figure 6 in accordance with embodiments of the technology. The memory array 200 can include components that are generally similar in structure and function to those of the memory array 100 in Figure 1. As such, similar identification numbers generally refer to similar structure and/or components.

[0043] Referring to both Figures 6 and 7, the memory array 200 can include a grid 201 and a plurality of memory nodes 206 (identified individually as first to sixteenth memory nodes 206a-206p, respectively) carried by the grid 201. The grid 201 can include a plurality of first access lines 202 (identified individually as first to fourth contact lines 202a-202d, respectively) and a plurality of second access lines 204 (identified individually as first to eighth access lines 204a-204h, respectively). The first and second access lines 202 and 204 can be generally orthogonal relative to one another. The first and second access lines 202 and 204 can include a generally conductive trace constructed from a metal, a metal alloy, doped semiconductor material, and/or other suitable materials.

[0044] The memory nodes 206 are individually connected to the first and second access lines 202 and 204. As shown in Figure 6, an individual memory node 106 can include a first memory cell 110a, a first rectifier 108a, a second rectifier 108b, and a second memory cell 110b connected to one another in a series. The input terminals of the first and second rectifiers 108a and 108b share an input point 114 that is electrically connected to corresponding first access lines 202. The output terminals of the first and second rectifiers 108a and 108b are electrically connected to the first and second memory cells 110a and 110b, which are in turn connected to corresponding second access lines 204, respectively.

[0045] Any of the memory nodes 206 that share a common first access line 202 do not share a common second access line 204. For example, the first memory node 206a and the second memory node 206b are both connected to the first access line 202a. However, these two memory nodes 206a and 206b do not share a common second access line 204. Instead, the first memory node 206a is connected to the first and second access lines 204a and 204b while the second memory node 206b is connected to the third and fourth access lines 204c and 204d.

[0046] In operation, each of the memory cells 110 in the individual memory nodes 206 may be addressed or accessed by energizing a pair of corresponding first and second access lines 202 and 204. For example, the memory cells 110 of the tenth memory node 206j may be accessed by energizing the first access line 202c and one of the second access lines 204c and 204d. As shown in Figure 6, the first access line 202c and the second access line 204c are energized (as indicated by the thickened lines) by having reversed polarity relative to other first and second access lines 202 and 204. As a result, electrical current flows from the first access line 202c via the connection node 114, the first rectifier 108a, and the first memory cell 110a to the second access line 204c. As a result, the state and/or other information stored in the first memory cell 110a may be changed or read. While accessing the first memory cell 110a, the second memory cell 110b is not altered because the second access line 204d connected to the second memory cell 110b is biased with the same polarity as the first access line 202c. After the first memory cell 110a is accessed, the second memory cell 110b may be accessed by energizing the first access line 202c and the second access line 204d. As a result, electrical current flows from the first access line 202c via the connection node 114, the second rectifier 108b, and the second memory cell 110b to the second access line 204d.

[0047] Figures 8A-8F are top and cross-sectional views of a portion of a semiconductor substrate material 250 undergoing a process useful for forming several embodiments of the orthogonal memory array 200 of Figure 6 in accordance with embodiments of the technology. In the illustrated embodiment, the substrate material 250 includes a P-type dopant for illustration purposes. One of ordinary skill in the art would understand that the substrate material 250 may also include an N-type dopant or that the substrate material 250 may also be not doped.

[0048] Figures 8A and 8B are top and cross-sectional views of the substrate material 150 during an initial stage of the process in which the second access lines 204 are formed. As shown in Figures 8A and 8B, an N-type silicon material 251 can be blanket-deposited onto the substrate material 250 using chemical vapor deposition (CVD), plasma-enhanced vapor deposition (PEVD), and/or another suitable technique, or by counterdoping the P-type substrate with N-type dopants. Subsequently, the N-type silicon material 251 can be patterned using photolithography and partially removed to form a plurality of first trenches 253.

[0049] In the illustrated embodiment, the first trenches 253 extend through the N-type silicon material 251 into the substrate material 250. In other embodiments, the first trenches 253 extend through the N-type silicon material 251 to interface with the substrate material 250. In

further embodiments, the first trenches 253 extend partially through the N-type silicon material 251 without reaching the substrate material 250. After partially removing the N-type silicon material 251, the first trenches 253 may be filled with an insulation material to isolate the contact lines 102 (not shown). For example, in one embodiment, a blanket insulation material 252 may be deposited onto the substrate material 250 and then removed to expose the top surface 251a of the N-type material 251.

[0050] Figures 8C and 8D are top and cross-sectional views of the substrate material 150 during another stage of the process in which the conductive contacts 216 are formed following a process generally similar to that discussed above with reference to Figures 5E and 5F. Figures 8E and 8F are top and cross-sectional views of the substrate material 250 during another stage of the process in which the memory nodes 206 are formed following a process generally similar to that discussed above with reference to Figures 5G and 5H. However, unlike the embodiment illustrated in Figures 5G and 5H, the individual columns 160 do not share a common conductive contact 116. Instead, each conductive contact 116 is associated with only one column 160. Subsequently, the process may include forming individual memory nodes by patterning and etching the columns 160. The process may then include forming the first access lines 202 over the formed memory nodes 106 following a process generally similar to that discussed with reference to Figures 5J and 5K.

[0051] From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the disclosure. Many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the disclosure is not limited except as by the appended claims.

CLAIMS

I/We claim:

1. A memory structure, comprising:
 - an access line extending along a first direction;
 - a first contact line and a second contact line extending along a second direction different than the first direction, the first and second contact lines being generally parallel to each other;
 - a memory node including:
 - a first memory cell electrically connected between the access line and the first contact line to form a first circuit; and
 - a second memory cell electrically connected between the access line and the second contact line to form a second circuit electrically independent from the first circuit.
2. The memory structure of claim 1 wherein the first and second contact lines form an oblique angle with the access line.
3. The memory structure of claim 1 wherein
 - the first and second directions form an oblique angle of about 63° ; and
 - the memory node further includes:
 - a first rectifier having a first input terminal and a first output terminal;
 - a second rectifier having a second input terminal and a second output terminal;
 - the first input terminal of the first rectifier and the second input terminal of the second rectifier being electrically connected to the access line;
 - the first and second memory cells including chalcogenide glass;
 - the first memory cell being electrically connected to the first output terminal of the first rectifier and the first contact line; and
 - the second memory cell is electrically connected to the second output terminal of the second rectifier and the second contact line.

4. The memory structure of claim 1 wherein:
the first and second directions form an oblique angle of about 63° ; and
the first and second circuits are electrically isolated from each other.
5. The memory structure of claim 1 wherein
the first and second directions form an oblique angle; and
the memory node further includes:
 - a first rectifier having a first input terminal and a first output terminal;
 - a second rectifier having a second input terminal and a second output terminal;
 - the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line; and
 - the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.
6. The memory structure of claim 1, further comprising:
a first contact rectifier between the first memory cell and the first contact line; and
a second contact rectifier between the second memory cell and the second contact line.
7. The memory structure of claim 1 wherein
the first and second directions form an oblique angle;
the memory node further includes:
 - a first rectifier having a first input terminal and a first output terminal;
 - a second rectifier having a second input terminal and a second output terminal;
 - the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line; and
 - the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively; andthe memory structure, further comprising a first contact rectifier between the first memory cell and the first contact line; and
a second contact rectifier between the second memory cell and the second contact line.

8. The memory structure of claim 1 wherein the first and second contact lines are generally orthogonal relative to the access line.

9. The memory structure of claim 1 wherein:

the first and second contact lines are generally orthogonal relative to the access line;

the memory node further includes:

a first rectifier having a first input terminal and a first output terminal;

a second rectifier having a second input terminal and a second output terminal;

and

the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line.

10. A memory structure, comprising:

a plurality of access lines extending along a first direction;

a plurality of contact lines extending along a second direction different from the first direction, the individual contact lines and the individual access lines forming a plurality of pairs of access and contact lines;

a plurality of memory nodes electrically connected to the access and contact lines, the individual memory nodes including:

a first memory cell electrically connected between a first pair of access and contact lines; and

a second memory cell electrically connected between a second pair of access and contact lines, the first and second pairs of access and contact lines are electrically isolated from each other.

11. The memory structure of claim 10 wherein the contact lines form an oblique angle with the access lines.

12. The memory structure of claim 10 wherein

the individual memory nodes further include:

a first rectifier having a first input terminal and a first output terminal;

a second rectifier having a second input terminal and a second output terminal;

the first input terminal of the first rectifier and the second input terminal of the second rectifier are electrically connected to the access line; and
the first output terminal of the first rectifier and the second output terminal of the second rectifier are electrically connected to the first and second memory cells, respectively.

13. The memory structure of claim 10, further comprising:

a first contact rectifier between the first memory cell and the individual contact lines;
and
a second contact rectifier between the second memory cell and the individual contact lines.

14. The memory structure of claim 10 wherein the contact lines are generally orthogonal relative to the access lines.

15. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;
the contact lines include a first contact line and a second contact line;
the access lines include a first access line and a second access line;
the memory nodes include a first memory node and a second memory node;
the first memory node includes:

a first memory cell electrically connected to the first contact line;
a first rectifier having a first input terminal electrically connected to the first access line and a first output terminal electrically connected to the first memory cell, the first contact line, the first memory cell, the first rectifier, and the first access line forming a first circuit;
a second memory cell electrically connected to the second contact line; and
a second rectifier having a second input terminal electrically connected to the first access line and a second output terminal electrically connected to the second memory cell, the second contact line, the second memory cell, the second rectifier, and the first access line forming a second circuit; and

the second memory node includes:

a first memory cell electrically connected to the first contact line;
a first rectifier having a first input terminal electrically connected to the second access line and a first output terminal electrically connected to the first memory cell, the first contact line, the first memory cell, the first rectifier, and the second access line forming a third circuit;
a second memory cell electrically connected to the second contact line;
a second rectifier having a second input terminal electrically connected to the second access line and a second output terminal electrically connected to the second memory cell, the second contact line, the second memory cell, the second rectifier, and the second access line forming a fourth circuit;
the first, second, third, and fourth circuits are electrically isolated from one another.

16. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines form a first pair of contact lines and a second pair of contact lines adjacent to the first pair of contact lines; and
the first and second pairs of contact lines are electrically isolated from each other.

17. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines form a first pair of contact lines and a second pair of contact lines adjacent to the first pair of contact lines;
the memory nodes include a first memory node electrically connected to one of the access lines and the first pair of contact lines, and a second memory node electrically connected to the one of the access lines and the second pair of contact lines; and
the first and second memory nodes are electrically isolated from each other.

18. The memory structure of claim 10 wherein:
the contact lines are generally orthogonal relative to the access lines;
the contact lines include first and second contact lines;
the access lines include first and second access lines;

the memory nodes include a first memory node electrically connected to the first access line and the first and second contact lines, and a second memory node electrically connected to the second access line and the first and second contact lines; and the first and second memory nodes are electrically isolated from each other.

19. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;

the contact lines include first and second contact lines;

the access lines include first and second access lines;

the memory nodes include a first memory node and a second memory node;

the first memory node includes:

a first memory cell electrically connected between the first access line and the first contact line forming a first circuit; and

a second memory cell electrically connected between the first access line and the second contact line forming a second circuit;

the second memory node includes:

a first memory cell electrically connected between the second access line and the first contact line forming a third circuit; and

a second memory cell electrically connected between the second access line and the second contact line forming a fourth circuit; and

the first, second, third, and fourth circuits are electrically isolated from one another.

20. The memory structure of claim 10 wherein:

the contact lines are generally orthogonal relative to the access lines;

the contact lines include first and second contact lines;

the access lines include first and second access lines;

the memory nodes include a first memory node and a second memory node;

the first memory node includes:

a first memory cell and a first rectifier electrically connected between the first access line and the first contact line forming a first circuit; and

a second memory cell and a second rectifier electrically connected between the first access line and the second contact line forming a second circuit;

the second memory node includes:

- a first memory cell and a first rectifier electrically connected between the second access line and the first contact line forming a third circuit; and
- a second memory cell and a second rectifier electrically connected between the second access line and the second contact line forming a fourth circuit; and

the first, second, third, and fourth circuits are electrically isolated from one another.

21. A memory structure, comprising:

- a dielectric having a first sidewall, a second sidewall, and a third wall between the first and second sidewalls;
- a first memory cell on the first sidewall;
- a second memory cell on the second sidewall; and
- a doped material on the third wall of the dielectric, the doped material having a first portion, a second portion, and a third portion between the first and second portions, the first and second portions including a first dopant, the third portion including a second dopant different than the first dopant.

22. The memory structure of claim 21 wherein:

- the dielectric has a generally rectangular shape;
- the first and second memory cells include chalcogenide glass;
- the first and second portions of the doped material include an N-type material; and
- the third portion of the doped material includes a P-type material.

23. The memory structure of claim 21 wherein the first and second memory cells include a layer of chalcogenide glass.

24. The memory structure of claim 21 wherein:

- the dielectric is a first dielectric;
- the first and second memory cells have an L shape; and
- the memory structure further includes a second dielectric partially enclosed by the first and second memory cells.

25. A method for manufacturing a memory structure, comprising:
forming a first contact line and a second contact line in a substrate material, the first and second contact lines extending along a first direction;
electrically connecting a memory node to the first and second contact lines, the memory node including a first memory cell electrically connected to the first contact line and a second memory cell electrically connected to a second contact line;
forming an access line in and/or on the substrate material, the access line extending along a second direction different from the first direction; and
electrically connecting the access line to the first and second memory cells, the access line, the first memory cell, and the first contact line forming a first circuit, the access line, the second cell, and the second contact line forming a second circuit electrically isolated from the first circuit.

26. The method of claim 25 wherein:
forming a first contact line and a second contact line includes:
depositing a conductive material onto the substrate material;
removing a portion of the deposited conductive material;
forming the first and second contact lines with the remaining conductive material; and
insulating the first and second contact lines with an insulation material;
electrically connecting a memory node to the first and second contact lines includes:
depositing a first dielectric onto the first and second contact lines;
forming a plurality of openings in the first dielectric, the openings exposing the first and second contact lines; and
depositing a first conductive material in the openings, and thereby forming a plurality of conductive contacts between the memory node and the first and second contact lines; and
forming an access line in and/or on the substrate material includes:
depositing a second dielectric onto the conductive contacts and the memory node;
forming a trench in the second dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is at an oblique angle with the first direction; and

depositing a second conductive material in the trench, and thereby forming the access line.

27. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material; and

insulating the first and second contact lines with an insulation material; and

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a trench in the dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is at an angle of about 63° with the first direction; and

depositing a conductive material in the trench, and thereby forming the access line.

28. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material, the first and second contact lines having a first width a therebetween; and

insulating the first and second contact lines with an insulation material;

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a first trench and a second trench in the dielectric, the first and second trenches having a second width b therebetween and extending along a second direction forming an angle α according to the following formula:

$$\alpha = \arctan\left(\frac{b}{a}\right); \text{ and}$$

depositing a conductive material in the first and second trenches, and thereby forming a first access line and a second access line.

29. The method of claim 25 wherein:

forming a first contact line and a second contact line includes:

depositing a conductive material onto the substrate material;

removing a portion of the deposited conductive material;

forming the first and second contact lines with the remaining conductive material; and

insulating the first and second contact lines with an insulation material; and

forming an access line in the substrate material includes:

depositing a dielectric onto the memory node;

forming a trench in the dielectric, the trench exposing at least a portion of the memory node and extending along a second direction that is generally orthogonal to the first direction; and

depositing a conductive material in the trench, and thereby forming the access line.

30. A method for manufacturing a memory structure, comprising:

forming a column on a substrate material, the column having of a dielectric in direct contact with the substrate material and a doped material on the dielectric, the column having a first sidewall and a second sidewall;

depositing a memory material on the column and the substrate material; and

selectively removing a portion of the memory material from the column and the substrate material such that a first portion of the memory material remains on the first sidewall and a second portion of the memory material remains on the second sidewall.

31. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric; and

selectively removing a portion of the dielectric and the doped material to form the column.

32. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric, the doped material including a first dopant;

selectively removing a portion of the dielectric and the doped material to form the column; and

the method further includes selectively introducing a second dopant into the doped material, the second dopant being different from the first dopant.

33. The method of claim 30 wherein forming a column on a substrate material includes:

depositing the dielectric on the substrate;

depositing the doped material on the dielectric, the doped material including an N-type dopant;

selectively removing a portion of the dielectric and the doped material to form the column; and

the method further includes selectively introducing a P-type dopant into the doped material and forming a first P/N junction and a second P/N junction in the doped material.

34. The method of claim 30 wherein depositing a memory material includes depositing a memory material containing chalcogenide glass.

35. The method of claim 30 wherein:

the column includes a third wall between the first and second sidewalls;

depositing a memory material includes depositing a memory material containing chalcogenide glass onto the first and second sidewalls and the third wall; and

selectively removing a portion of the memory material includes selectively removing a portion of the memory material from the third wall of the column and the substrate material such that the first portion of the memory material remains on the first sidewall and the second portion of the memory material remains on the second sidewall.

36. The method of claim 30 wherein:

the column includes a third wall between the first and second sidewalls;

depositing a memory material includes depositing a memory material containing chalcogenide glass onto the first and second sidewalls and the third wall; and

selectively removing a portion of the memory material includes spacer etching the memory material such that the first portion of the memory material remains on the first sidewall and the second portion of the memory material remains on the second sidewall.

37. The method of claim 30 wherein:

the dielectric is a first dielectric; and

the method further includes:

depositing a second dielectric on the memory material; and

selectively removing a portion of the memory material by spacer etching the memory material and the second dielectric such that a first portion of the memory material and the second dielectric remains on the first sidewall and a second portion of the memory material and the second dielectric remains on the second sidewall.

38. The method of claim 30 wherein:

the dielectric is a first dielectric; and

the method further includes:

depositing a second dielectric on the memory material;

selectively removing a portion of the memory material by spacer etching the memory material and the second dielectric such that a first portion of the memory material and the second dielectric remains on the first sidewall

and a second portion of the memory material and the second dielectric remains on the second sidewall; and
removing a portion of the column after removing a portion of the memory material, and thereby forming a plurality of discrete nodes.