MANUFACTURING PROCESS FOR A MULTILAYER STRUCTURE

The present invention relates to a manufacturing process for a multilayer structure made of semiconductor materials, said structure comprising a substrate made of a first semiconductor material and a superficial thin layer made of a second semiconductor material, the two semiconductor materials having substantially different lattice parameters.

Processes of this type are already known.

It is therefore known to produce structures comprising a substrate made of a material such as silicon, and a superficial thin layer made of a material such as silicon-germanium (SiGe), or even germanium (Ge).

Patent application FR 0208600 in the name of the applicant relates to a process for producing a structure comprising a thin layer of semiconductor material from a wafer comprising a lattice parameter adaptation layer comprising an upper layer made of semiconductor material having a first lattice parameter, characterised in that it comprises the following stages:

(a) growth on the upper layer of the adaptation layer of a film of semiconductor material having a second nominal lattice parameter substantially different to the first lattice parameter, with a sufficiently minimal thickness to keep the first lattice parameter of the upper layer of the underlying adaptation layer and therefore be strained,

(b) growth on the film of a relaxed layer of semiconductor material having a nominal lattice parameter substantially identical to the first lattice parameter,

(c) removal of at least a part of the wafer on the side of the adaptation layer relative to the relaxed layer comprising the following operations:

- formation of an embrittlement zone to the side of the adaptation layer relative to the relaxed layer,
- power supply at the embrittlement zone to detach from the wafer a structure comprising the relaxed layer.

The process of this patent application therefore employs a layer transfer technique (in particular of the SMARTCUT® type or the ELTRAN® type) to constitute the desired wafer.

And a starting element of this process is a wafer comprising a lattice parameter adaptation layer corresponding to a region of the wafer presenting on its surface a layer of substantially relaxed material, without a large number of structural defects, such as dislocations.

It is specified that relaxed layer is understood to mean any layer of a semiconductor material which has a non-strained crystallographic structure, that is, one which has a lattice parameter substantially identical to

the nominal lattice parameter of the material making up the layer.

Inversely, a strained layer is referred to as any layer of a semiconductor material whereof the crystallographic structure is strained in traction or in compression during crystalline growth, such as epitaxy, obliging at least a lattice parameter to be substantially different to the nominal lattice parameter of this material.

The process of patent application FR 0208600 constitutes an advantageous solution to constitute structures such as mentioned at the start of this text.

The object of the present invention is to provide a certain complement to the teaching of this patent application.

To attain this aim the invention proposes a production process for a multilayer structure made of semiconductor materials, said structure comprising a substrate made of a first semiconductor material and a superficial thin layer made of a second semiconductor material, the two semiconductor materials having substantially different lattice parameters, characterised in that the process comprises the following steps:

- producing a layer comprising said superficial thin layer on a support substrate,
- creating an embrittlement zone in the ensemble formed by said support substrate and said deposited layer,
- bonding said ensemble with a target substrate,
- detaching at the level of this embrittlement zone,

- treating the surface of the resulting structure.

Other aspects, aims and advantages of the invention will emerge more clearly from the following description of the invention, given with reference to the attached diagrams, in which Figures 1a to 1f illustrate the principal steps for implementing an embodiment of the invention.

With reference firstly to Figure 1a, this shows a support substrate 100, on which a layer 105 (shown in hatching) has been deposited.

The support substrate 100 is made of a semiconductor material having a first lattice parameter. It can be made of silicon, for instance.

The layer 105 is a layer made of a material having a second lattice parameter different to the first lattice parameter mentioned hereinabove.

The layer 105 can therefore be made of SiGe, or even of Ge.

It is said that the layer 105 is deposited by a technique allowing:

- depositing of a desired thickness of a material whereof the lattice parameter is substantially different to the lattice parameter of the support substrate on which the deposit is made,
- while constituting a superficial layer of such a deposit which is virtually exempt from defects of dislocation type.

The document WO 00/15885 teaches for example a process allowing SiGe or Ge to be deposited on silicon.

Such a deposit process can therefore for example be done according to a first mode in which monocrystalline

Ge is deposited on a support substrate of monocrystalline silicon, by putting into effect the following steps:

- temperature stabilisation of the substrate of monocrystalline silicon at a first preset stabilised temperature of 400°C to 500°C, preferably 430°C to 460°C,
- chemical deposition in the steam phase (CVD) of Ge at said first preset temperature until a base layer of Ge is obtained on the support substrate of a preset thickness of less than a final desired thickness,
- increase of the temperature of the chemical deposition in the steam phase of the Ge from the first preset temperature to a second preset temperature ranging from 750°C to 850°C, preferably from 800°C to 850°C, and
- continuing chemical deposition in the steam phase of Ge at said second preset temperature until a final desired thickness is obtained for the layer of monocrystalline Ge.

Such a deposit process can also be carried out according to variants - for example those disclosed by the document WO 00/15885.

Other methods for obtaining a thin layer of relaxed SiGe or relaxed Ge, directly on a support substrate which can be made of silicon, are also feasible.

Reference could also be made to the publication 'Strain relaxation of pseudomorphic Si1-xGex/Si (100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication', B. Holländer et al, Nuclear Instrument and Methods in

Physics Research B175-177 (2001) 357-367 which is incorporated by reference herein.

In such a process, the layer 110 is produced by making a strained layer, and by relaxation of this layer.

Thin layers of relaxed SiGe can also be obtained by techniques disclosed in the following documents, which are incorporated by reference as they disclose methods for obtaining such layers which can be carried out for the invention :

- "Development of a new type of SiGe thin strained relaxed buffer based on the incorporation of carbon containing layer", presented in the first SiGe Technology and Device Meeting (ISTDM, Nagoya, Japan, January 15-17, 2003,

- "Thin SiGe Buffers with High Ge content for n-Mosfets" (Lyutovich et al. Material Science & Engineering, B89 (2002), 341-345),

- "Relaxed SiGe buffers with thickness below 0.1 μm" (Bauer et al.- Thin Solid Films 369 (2000), 152-156).

Coming back to the process of the invention, in all cases a layer 110 which comprises the superficial thin layer of the structure to be produced has been created on the support substrate 100.

An intermediate wafer 10, comprising a layer 110 of SiGe (with the desired Si/Ge ratio) or of Ge on the support substrate 100, has thus been made.

The free surface of this layer 100 can be polished in order to allow the bonding of the intermediate wafer 10 which is to follow in the process.

The surface roughness of the intermediate wafer 10 should indeed be no more than a few angstroms rms for such bonding.

An interface 105 is therefore defined between the layer 110 and the support 100.

It is specified that by using this type of deposit process, the defects of dislocation type have been confined to the region of the layer 110 which is adjacent to the interface 105.

Confinement is understood to mean the majority of the defects of dislocation type located in said region. The rest of the layer 110 is not fully exempt from defects, but their concentration is compatible with microelectronic applications.

Accordingly, this region of the layer 110 in which the defects of dislocation type are confined make up a lattice parameter adaptation layer, between the support substrate 100 made of silicon and the superficial region of the layer 110, which makes up in itself a layer of the wafer 10 made of Ge or relaxed SiGe.

And this layer of Ge or relaxed SiGe has a desired thickness following the deposit made at the beginning of the process. This desired thickness can be in particular of the order of 0.5 to 1 micron.

With reference now to Figure 1b, an embrittlement zone 120 is created in the thickness of the wafer 10.

This embrittlement zone can in particular be made by implantation of species through the layer 110.

The species implanted are one or several atomic or molecular species, e.g. hydrogen or helium ions or molecules.

The implantation can also be a co-implantation of different species, e.g. hydrogen and helium. It is specified that in this text "implantation" covers as well such a co-implantation of at least two species.

When the embrittlement zone is made by implantation, the implantation parameters can be defined so that the embrittlement zone is located in the support substrate 100, as illustrated in Figure 1b.

It is also possible to define these parameters so that the embrittlement zone is located in the layer 110 itself (preferably in the region of this layer adjacent to the interface 105).

It is specified that the embrittlement zone can also have been made by creating a porous region in the support substrate 100, before depositing the layer 110.

Next comes the wafer comprising its embrittlement zone, and this wafer is bonded to a target substrate 20.

The target substrate 20 can be made of silicon.

The face of the wafer 10 which is stuck onto the target substrate is that which corresponds to the relaxed surface of the layer 110.

To carry out this bonding, the surfaces have been cleaned prior to being placed in contact and an bonding layer has been optionally inserted in between these surfaces.

Also, an electrical insulating layer, for example an oxide, can have been inserted in between the wafer and the target substrate.

Such an oxide can originate from oxidation of the surface of the target substrate 20.

It can likewise originate from oxidation of the surface of the layer 110, if it is made of SiGe.

If the layer 110 is made of Ge or SiGe, then it is also possible to associate an oxide layer to it prior to bonding, by oxide deposition.

The wafer and/or the target substrate can therefore be associated to an insulating layer, prior to bonding.

If required, the surface of one or both of the substrates to be bonded can be treated, in order to bring the surface roughness of these substrates down to values which favour bonding (i.e. not more than a few angströms rms).

Such surface treatment can be a polishing step.

After bonding, it is possible to proceed with classic thermal treatment for consolidation of the bonding interface.

Next comes detachment at the level of the embrittlement interface, by thermal and/or mechanical power supply.

The result is a structure 30 comprising, as illustrated in Figure 1d:

- the target substrate 20,
- the layer 110,
- optionally residue of the support substrate 100.

In this structure, the layer 110 itself comprises:

- a lattice parameter adaptation layer (part of the layer 110 which is adjacent to the residue of the support substrate 100), and
- a relaxed layer of desired thickness.

In the event where the embrittlement zone has been constituted by implantation in the thickness of the "lattice parameter adaptation layer" of layer 110, the resulting structure 30 does not comprise residue of the

support substrate, and a part of the lattice parameter adaptation layer has been separated from this structure 30 during detachment.

In this case, the surface of the resulting structure is treated (Figure 1e) to improve the surface state of the layer 110.

This surface treatment can comprise polishing, as well as other types of treatment.

It is also possible to perform the implantation so as to obtain the embrittlement zone in the part of layer 110 which is relaxed.

In such case, the transferred layer does not comprise defaults such as dislocations (or only very few), and the resulting structure after detachment can present a surface layer (which comes from the relaxed part of layer 110) which does not need any additional treatment.

In the case where the embrittlement zone has been made up in the thickness of the support substrate 100 (by implantation or by a priori creation of a porous region), the next step is selective attack of the residue of this support substrate.

This selective attack can be selective chemical etching, which attacks only the material of the support substrate.

Such etching can be done by a humid method (choice of an adapted etching solution), or by a dry method (selective etching via energy plasma, or pulverisation).

Such etching can be preceded by polishing.

At the beginning of this selective attack, the free surface of the layer 110 is treated to remove the lattice parameter adaptation layer, corresponding to the

part of this layer 110 in which the defects of dislocation type are confined.

Described hereinabove are two main variants for implementing the invention (creation of an embrittlement zone in the support substrate, and in the layer 110 respectively).

In these two cases, the active layer of the final structure corresponds to the relaxed part of the layer 110.

In accordance with a third main variant, the layer 110 is in reality constituted by different levels (or strata), and this layer 110 has been created as follows:

- deposit of a first level, for example by a technique such as that disclosed by the document WO 00/15885 or by the reference B. Holländer et al mentioned above, or generally by any other known technique for producing a relaxed thin layer,
- deposit of a second level, constituting a stop layer for chemical attack,
- deposit of a third level corresponding to a relaxed layer to constitute the active layer of the final structure. Such deposition is done with a desired thickness for the active layer.

The first level corresponds to the lattice parameter adaptation layer. It can be made of SiGe, or Ge.

The second level at the same time must:

- have good selectivity relative to the third level, vis-à-vis chemical attack (in this respect, different materials must be employed for levels 2 and 3), and

- not induce too significant a difference in terms of lattice parameter with the two levels surrounding it (in this respect, the materials of levels 1, 2 and 3 must not be too different).

For example, the following combinations could be created:

Material level 1	Material level 2	Material level 3
Ge	SiGe (50/50)	SiGe or Ge
SiGe	strained Si	SiGe or Ge

It is preferable for the layers of level 1 and 3 to be made from materials of the same nature, so that the layer of level 2, intercalated between these two layers, receives homogeneous constraints on its two faces.

In this case, the following materials will preferably be used:

Material level 1	Material level 2	Material level 3
Ge	SiGe (50/50)	Ge
SiGe	strained Si	SiGe

In this third variant, the same steps are followed for creating an embrittlement zone, bonding and detachment of the structure 30.

The embrittlement zone can therefore here again be located in the layer 110. In this case, it is preferably located in the thickness of the first level (in which it has been created by implantation).

To obtain the final structure two selective attacks are carried out:

- a first selective attack for eliminating the residue of the first level. This attack can in particular be a chemical attack, thus justifying insertion of a level corresponding to a stop layer,
- a second selective attack for eliminating the stop layer itself.

It is also possible to constitute the layer 110 with only two levels, whereof a first level such as described hereinabove and a second level resembling the levels 2 and 3 mentioned above.

In this case, the second level can for example be made of strained silicon, whereas the first level is made of SiGe or Ge.

And the second level thus makes up the active layer of the final structure, while the first level still constitutes a lattice parameter adaptation layer.

Still in this case, the following materials will be able to be used (this table, as with the preceding ones, is given by way of non-limiting example):

Material level 1	Material level 2
Ge	SiGe (50/50)
SiGe	strained Si

In all cases, conventional surface treatment measures can be followed after the structure of Figure 1e has been produced.

The invention therefore enables multilayer structures to be produced which comprise for example a layer of Ge or SiGe on a silicon substrate.

It shall be noted that in the case of the invention, the adaptation layer of layer 110 does not

present a concentration gradient in its thickness (e.g. a gradient of the concentration in Germanium if the adaptation layer is between a Si support substrate and a relaxed layer in Ge or SiGe with a given concentration of Ge).

Conventional adaptation layers often present such a concentration gradient, which corresponds to a gradient of the lattice parameter in the adaptation layer.

But such adaptation layers with a concentration gradient are necessarily relatively thick (the more important the difference in lattice parameter on both sides of the adaptation layer, the thicker the adaptation layer).

WO 02/15244 discloses an example of such traditional adaptation layer with a concentration gradient.

In the case of the invention, on the contrary, the adaptation layer can be very thin.

It is indeed reminded that the defects (e.g. dislocations) are confined to the region of the layer 110 which is adjacent to its interface 105 with the support substrate 100.

This specific aspect of the invention is advantageous (in comparison with known techniques, such as disclosed e.g. in WO 02/15244).

An illustration of the advantages associated to this aspect is the fact that such thin adaptation layer makes it possible to create the embrittlement zone by implantation within the support substrate 100, by traversing the adaptation layer with the implanted species.

This allows, after detachment and suppression of the remaining material (Si or other) of the support substrate 100, to obtain for the final structure a very good quality surface, without needing burdensome treatments for treating a splitted surface such as the one that would be obtained by detachment at an embrittlement zone located within the adaptation layer itself (which would be the case with the adaptation layers with gradient, which are too thick to be traversed by the implantation).

It shall also be noted that the structures obtained by the present invention are examples of defects of dislocation type, even in an embedded region.

And the resulting structures can then be used to have supplementary layers, for example strained silicon, grow by epitaxy on the layer of SiGe or Ge.

In the case where the layer of level 2 is made of strained Si, it can be advantageous to make only a single selective attack in order to conserve a final structure consisting of a bi-layer of strained silicon - SiGe on a silicon substrate.

In this case, the final structure preserves the stop layer.

Finally , it is also possible to deposit a layer of strained silicon on the layer of level 3 prior to the stage of bonding this structure onto the target substrate, so as to finally produce a structure comprising a layer of strained silicon on a silicon substrate.

CLAIMS

1. A production process for a multilayer structure made of semiconductor materials, said structure comprising a substrate (20) made of a first semiconductor material and a superficial thin layer made of a second semiconductor material, the two semiconductor materials having substantially different lattice parameters, characterised in that the process comprises the following steps:

- producing a layer (110) comprising said superficial thin layer on a support substrate (100),
- creating an embrittlement zone in the ensemble (10) formed by said support substrate and said deposited layer,
- bonding said ensemble with a target substrate (20),
- detaching at the level of this embrittlement zone,
- treating the surface of the resulting structure.

2. The process as claimed in the preceding claim, characterised in that said step of producing a layer is made by epitaxy.

3. The process as claimed in the preceding claim, characterised in that said epitaxy is undertaken using the following steps:

- temperature stabilisation of the support substrate at a first preset stabilised temperature,

- chemical deposition in the steam phase at said first preset temperature until a base layer is obtained on the support substrate of a preset thickness of less than a final desired thickness for said layer (110) comprising the superficial thin layer,
- increase of the temperature of the chemical deposition in the steam phase from the first preset temperature to a second preset temperature, and
- continuing chemical deposition in the steam phase at said second preset temperature until a final desired thickness is obtained for the layer.

4. The process as claimed in the preceding claim, characterised in that the first preset temperature is of the order of 400°C to 500°C, and the second preset temperature is of the order of 750°C to 850°C.

5. The process as claimed in the preceding claim, characterised in that the first preset temperature is of the order of 430°C to 460°C, and the second preset temperature is of the order of 800°C to 850°C.

6. The process as claimed in Claim 1, characterised in that said layer is produced by creating a strained layer and by relaxation of this layer.

7. The process as claimed in any one of the preceding claims, characterised in that said production of the embrittlement zone is carried out by implantation.

8. The process as claimed in the preceding claim, characterised in that the implantation is a co-implantation of at least two species.

9. The process as claimed in one of the two preceding claims, characterised in that said implantation is carried out between the production stage and the bonding stage.

10. The process as claimed in the preceding claim, characterised in that implantation is carried out so as to define the embrittlement zone in the thickness of the support substrate.

11. The process as claimed in Claim 9, characterised in that implantation is carried out so as to define the embrittlement zone in a region of the layer (110) created corresponding to a lattice parameter adaptation layer.

12. The process as claimed in Claim 9, characterised in that implantation is carried out so as to define the embrittlement zone in a region of the layer (110) created corresponding to a relaxed layer.

13. The process as claimed in any one of the preceding claims, characterised in that prior to bonding an electrically insulating layer was inserted between said ensemble (10) formed by the support substrate and the deposited layer, and the target substrate (20).

14. The process as claimed in the preceding claim, characterised in that prior to bonding an electrically insulating layer was formed on the surface of said ensemble (10) formed by the support substrate and the deposited layer.

15. The process as claimed in any one of the two preceding claims, characterised in that prior to bonding an electrically insulating layer was formed on the target substrate.

16. The process as claimed in any one of the three preceding claims, characterised in that said electrically insulating layer is a layer of oxide.

17. The process as claimed in any one of the preceding claims, characterised in that the substrate (20) of the multilayer structure is made of silicon.

18. The process as claimed in any one of the preceding claims, characterised in that the support substrate (100) is made of silicon.

19. The process as claimed in any one of the preceding claims, characterised in that the layer (110) created is made of SiGe or Ge.

20. The process as claimed in any one of the preceding claims, characterised in that when the layer is being formed a level is created corresponding to a stop layer for chemical attack during the surface treatment stage.

21. The process as claimed in the preceding claim, characterised in that when the layer is being formed three levels are formed corresponding to the following:

- Level 1: lattice parameter adaptation layer,
- Level 2: stop layer,
- Level 3: active layer of the structure to be obtained.

22. The process as claimed in the preceding claim, characterised in that the materials of the layers corresponding to said three levels constitute one of the following combinations:

Material level 1	Material level 2	Material level 3
Ge	SiGe (50/50)	SiGe or Ge
SiGe	strained Si	SiGe or Ge

23. The process as claimed in the preceding claim, characterised in that the materials of the layers corresponding to said three levels constitute one of the following combinations:

Material level 1	Material level 2	Material level 3
Ge	SiGe (50/50)	Ge
SiGe	strained Si	SiGe

24. The process as claimed in any one of the four preceding claims, characterised in that the stop layer is preserved in the final structure.

25. The process as claimed in Claim 19, characterised in that when the layer is being formed two levels are formed corresponding respectively to:

- Level 1: lattice parameter adaptation layer,
- Level 2: active layer of the structure to be obtained.

26. The process as claimed in the preceding claim, characterised in that the materials of the layers corresponding to said three levels constitute one of the following combinations:

Material level 1	Material level 2
Ge	SiGe (50/50)
SiGe	strained Si