

APPLICATION FOR PATENT IN SINGAPORE

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INVENTION: DELTA-SIGMA MODULATOR

S P E C I F I C A T I O N

SPECIFICATION

DELTA-SIGMA MODULATOR

5 FIELD OF THE INVENTION

This invention relates to a delta-sigma modulator and more particularly to one composing oversampled plural-order modulator portion used in a
10 high precision A/D converter. The modulator performs noise shaping with minimal signal-to-noise ratio (S/N) degradation over a wide range of input levels.

15 BACKGROUND OF THE INVENTION

An oversampled A/D converter, often denoted as "delta-sigma A/D converter" is well known in the prior art. The delta-sigma A/D converter has come
20 into wide use primarily due to its high resolution output and adaptability to mixed-signal VLSI processes. The delta-sigma A/D converter is inherently an oversampling converter, although oversampling is just one of the techniques
25 contributing to its overall performance. The delta-sigma A/D converter essentially digitizes an analog

signal at a very high sampling rate (oversampling) to perform a noise-shaping function. Digital filtering after noise-shaping allows the delta-sigma A/D converter to achieve higher effective resolution than the quantized output from the delta-sigma modulator. Decimation is thereafter applied to reduce an effective sampling rate back to the "Nyquist rate". To gain an understanding of the delta-sigma A/D converter it is important to understand the operation of oversampling, noise-shaping, digital filtering and decimation.

Fig. 1 illustrates a conventional second-order delta-sigma modulator 10. The modulator 10 is denoted a second-order delta-sigma modulator in that an error signal at output Y is integrated twice with respect to time. Accordingly, the modulator 10 comprises two integrator circuits 12 shown in a dashed line. The integrators 12 are connected in series between a first summing node 14 and a quantizer 16. The quantizer 16 (shown as a analog-to-digital conversion block for digitizing, or "a/d" block) quantizes an analog output signal from the second integrator 12 to produce a digital code at the output Y. The quantized output is fed back to amplifiers having respective gain scale factors g_0 and g_1 denoted in Fig. 1, through a digital-to-analog

(denoted as "d/a") converter 18. The respective outputs of the amplifiers are connected to the first summing node 14 or a second summing node 20.

The output signal Y is fed to a digital
5 decimation filter 22 as a digital code. The filter 22 has the functions of filtering out the high frequency component of the quantization noise produced by quantizer 16, and of decimating the sampling frequency back to the original Nyquist
10 rate. Digital filtering is fairly well known and includes low pass technique utilizing a finite impulse response (FIR) filter, an infinite impulse response (IIR) filter, or a combination of both. Decimation can be included in or separate from the
15 filters.

The feedback from the digital-to-analog conversion circuit 18 to the first and second summing nodes 14 and 20, respectively, provides stability to the overall architecture. The circuit
20 18, the output of which is coupled either directly or through the amplifiers to nodes 14 and 20 via the feedback, basically functions as a reference voltage selector. Either a positive or a negative reference voltage (either +Vref or -Vref) is respectively
25 selected by the circuit 18 in accordance with its input level, a high logic level or a low logic

level. The selector 18 thereby can forward an appropriate reference voltage to the summing nodes 14 and 20 in accordance with the corresponding logic value of the digital output signal Y.

5 Conventional delta-sigma modulators often have difficulty in converting a full-range of analog input voltages. As shown in Fig. 2, as an analog input signal X approaches a full scale (i.e., 0.0 dB), noise is injected into the feedback loop due to
10 the non-linear behavior of the quantizer 16. Specifically, as the input signal X approaches a peak value, the quantizer 16, which is essentially a comparator with gain, begins to enter a non-linear state. Non-linearity is caused primarily from an
15 increase at quantizer 16 input while the reference feedback level from the circuit 18 remains fixed. That is, the gain of the quantizer 16 undergoes non-linear operation. The non-linear response at high input values causes the feedback loop to operate in
20 what is often called an "overload" condition. Overload is defined herein as a property of a delta-sigma modulator resulting from the failure of the quantized output data to follow increases in analog input values through negative feedback. Since the
25 output levels ($\pm V_{ref}$) of the quantizer 16 are limited, the quantizer gain will appear smaller as

its input increases. At some input level exceeding the threshold of overload amount, linear operation of the delta-sigma modulator cannot be maintained, causing the drop of signal-to-noise (S/N) ratio.

5 Fig. 2 illustrates a relatively linear slope 24 which changes to a non-linear curvature 26 as the input level is increased toward the full scale or peak value. The overload of the feedback loop is illustrated at the point (approximately -6.0 dB)
10 where the linear slope 24 changes to the substantially non-linear curvature 26.

Reduction in the comparator gain from a linear model to a non-linear model not only injects unacceptable noise into the feedback loop during
15 peak voltages of the input signal, but it may also cause the overall instability of the delta-sigma modulator even after the input signal which caused the instability is removed. Many skilled artisans have utilized reset trigger at the integrator
20 circuits, which resets modulator operation if a loop instability occurs. In addition to, or in lieu of reset trigger, gain scaling the first-order integrator has also been used. Gain scaling the feedback reference voltages to a level above the
25 peak analog input values is equal to reducing the signal levels within the integrator and quantizer,

and so the overload can be avoided. A description of gain scaling applicable to a first-order or second-order, single stage delta-sigma modulator is provided in reference to U.S. Patent No. 4,851,841
5 (herein incorporated by reference).

Gain scaling an effective feedback reference voltage to a level exceeding the analog input voltage allows the S/N boosting of the converted analog input signal near to the extremes of the
10 input signal peak values. Gain scaling the effective feedback reference voltage is illustrated in reference to the following transfer function of the output signal Y, indicative of the single stage second-order delta-sigma modulator of Fig. 1:

15

$$Y = XZ^{-2}/g_0 + Q(1-Z^{-1})^2 \quad (\text{Eq. 1})$$

, where Z^{-2} represents two delay times associated with blocks d of both integrators 12, $1-Z^{-1}$
20 represents the reciprocal of the transfer function of each integrator 12, and g_0 represents the scale factor of the first-order amplifier. After decimation, D_{out} is represented as the following transfer function:

25

$$D_{out} = Yg_0 = XZ^{-2} + Q(1-Z^{-1})^2g_0 \quad (\text{Eq. 2})$$

If noise is present with the analog input signal, then an analog noise factor is added to equation 2. The application of the scale factor g_0 to the analog input will cause an increase in the analog noise as well as an increase in the quantization noise $Q(1-Z^{-1})^2$. The application of the gain scale factor g_0 is therefore beneficial in the avoiding the overload, but at the cost of increasing the quantization noise and/or analog noise associated with the digital output signal D_{out} .

Modern day delta-sigma modulators attempt to minimize overload by utilizing what is often called a cascaded arrangement. A cascaded delta-sigma modulator is defined as one having more than one stage of first-order or multiple-order integrators coupled together. Fig. 3 illustrates a second-order stage coupled in cascade with a second first-order stage to form a cascaded 2:1 delta-sigma modulator. Between the second-order stage and the first-order stage, an interstage summing node 34 is coupled. The summing node 34 is configured to receive a scaled down analog signal from an amplifier 36 and a selectively amplified analog output from an amplifier 38. The scaling function of the amplifier 36 can be designed to have a scaling coefficient which is the inverse of the

product of scaling coefficients within amplifiers 40a and 40b. Additionally, the amplifier 38 can be designed to receive programmable instructions which define an amplification factor which allows the
5 interstage summing node 34 to produce (i) only analog data (i.e., data at the input of the quantizer 16) from the first stage 30 absent quantization noise, (ii) only the quantization noise absent the analog data from the first stage 30, or
10 (iii) a combination of the data and the noise.

The amplifier 42 at the output of the interstage summing node is preferably configured with a scale factor less than one. As a result, the level of the data, noise, or both, applied to the input of the
15 second stage 32 is maintained at a level necessary to minimize the overload of the stage 32. Reducing the input level to the second stage makes the input level to the quantizer 44 small, which causes the second stage to operate in a more linear range.
20 Even if the first stage utilizes its overall dynamic range, the level of signal forwarded from the amplifier 42 is maintained at a relatively low level so as not to exceed the feedback voltage levels sent from a reference voltage selector (i.e., digital-to-
25 analog converter) 46.

Fig. 4 illustrates a noise cancellation circuit 50 designed to receive the digital outputs Y_1 and Y_2 at respective outputs of the stages 30 and 32. A delay circuit 52 is coupled to receive the output Y_1 .
5 The delay circuit 52 functions to delay Y_1 data relative to Y_2 data, as Y_1 is presented to a summing node 54. The digital difference signal between the outputs Y_1 and Y_2 is produced at the output of a summing mode 62. A differentiator unit 60 comprises
10 two series-connected digital differentiators, which differentiates the digital difference signal from the summing node 62 in a manner known in the art. The output from the digital differentiator unit 60 is added to the output of the delay circuit 52 via
15 summing node 54, which yields a digital code at an output Y . A digital signal Y represents a digital code of high-speed digital bit pattern forwarded at the same frequency as the clock frequency of the quantizer circuits 16 and 44. The relative number
20 of logic 1's to logic 0's provided by the signal Y is indicative of the polarity and voltage magnitude of an analog input signal X .

The configuration and function of the cascaded 2:1 delta-sigma modulator 33 and the associated
25 noise cancellation circuit 50 of Figs. 3 and 4 are described in reference to U.S. Patent Nos. 5,148,166

and 4,920,544 (herein incorporated by reference).
As described in each of the above U.S. Patents, at
least two reasons for implementing a cascaded
arrangement, with appropriate noise cancellation,
5 are to remove the quantization noise generated by
the first stage 30 and to increase noise shaping
orders for the quantization noise of the second
stage. Scaling the output of the interstage summing
node 34 alleviates overload problems generally
10 associated with many non-cascaded arrangements. The
cascaded arrangement thereby achieves the advantages
associated with gain scaling the first-order input
of the first stage. Unfortunately, however, the
aforesaid cascaded arrangement by itself cannot
15 completely eliminate overload during times when the
input analog signal X is at or near the full scale
values.

Figs. 5 and 6 illustrate a cascaded 2:2 delta-
sigma modulator 70 with associated noise
20 cancellation circuit 72. The modulator 70 is
similar to the cascaded 2:1 delta-sigma modulator 33
of Fig. 3. However, the modulator 70 includes not
one, but two integrators within a second stage 74.
The second-order second stage 74 is therefore
25 similar to a second-order first stage 76. An i
interstage summing node 34, shown by the same

reference numeral as that in Fig. 3, includes the amplifiers 36 and 38 which input a scaled signal to the summing node 34. An output amplification is carried out by the amplifier 42 through a scale
5 factor preferably less than 1, and in many instances less than 1/2. Quantized signals Y_1 and Y_2 are fed into a noise cancellation circuit 72 shown in Fig. 6, with the delay circuit 52, the summing node 54 and the differentiator 60 shown by the same
10 reference numerals as that in Fig. 4.

The combination of the modulator 70 and noise cancellation circuit 72 produces the following transfer characteristic at output signal Y:

15
$$Y = XZ^{-4} + (1-Z^{-1})^4 Q_2 / hc1 \quad (\text{Eq. 3})$$

, where Z^{-4} represents four delay times associated with the delay circuits 78 and 80 of Fig. 5 and the dual delay circuit 52 of Fig. 6. $(1-Z^{-1})^4$ represents
20 a fourth-order noise shaping function within the modulator 70; Q_2 represents the quantization noise produced by the quantizer 44; and $hc1$ represents the gain scale factor of the amplifier 42 (at the interstage summing node 34 output). The
25 quantization noise produced by the quantizer 16 is canceled by use of the noise cancellation circuit

72. The gain scaling coefficient (or scale factor) of the amplifier 42 is denoted as hc_1 . The transfer functions of delay circuits associated with integrators and the integrators themselves are of common knowledge to skilled artisans and set forth in the U.S. Patent No. 5,061,928 (herein incorporated by reference).

The overload performance of a cascaded delta-sigma modulator such as a 2:1 or a 2:2 cascaded arrangement is generally better than a single stage delta-sigma modulator. Accordingly, the arrangements shown in Figs. 3 and 5 provide a significant improvement upon the arrangement shown in Fig. 1. Cascaded modulators perform over a wider dynamic range whether the first stage is overloaded or not, provided the subsequent (second) stage is not overloaded. Any overloaded quantization noise of the first stage will be canceled by the noise cancellation circuit 50 or 72. In order to minimize the possibility of overloading the second stage, the gain scale factor (hc_1) of the amplifier 42 is made very small, preferably less than 1, and in many instances less than 1/2. By making the gain scale factor small, overload is minimized at the cost of S/N ratio. The transfer function for the digital output signal Y of equation 3 bears this result.

Fig. 7 illustrates S/N ratio for a cascaded 2:1 arrangement such as that shown in Fig. 3, plotted as a function of input level. The figure shows that reduction in interstage gain scaling causes an improvement in overload performance at the cost of a higher S/N ratio. For example, an interstage gain scaling of $hc1=1/8$ results in a linear range closer to the full scale (0.0 dB) than the other larger gain scale factors. However, a gain scale factor of $1/8$ produces a lower S/N than the other gain scale factors. By gain scaling the analog input voltage for a cascaded 2:1 arrangement with a gain scale factor g_0 similar to that described in U.S. Patent No. 4,851,841, the transfer function of the output signal Y is as follows:

$$Y = XZ^{-3}/g_0 + (1-Z^{-1})^3 Q_2/hc1 \quad (\text{Eq. 4})$$

After decimation and gain compensation of g_0 , the decimator output D_{out} will be as follows:

$$D_{out} = g_0 Y = XZ^{-3} + g_0 (1-Z^{-1})^3 Q_2/hc1 \quad (\text{Eq. 5})$$

Increase in the input gain scale factor g_0 increases the quantization noise factor. As such,

equation 5 illustrates the negative effect of g_0 upon S/N ratio.

In an attempt to offset S/N degradation associated with the interstage gain scaling, the cascaded 2:2 modulator 70 can be employed, having the response shown in Fig. 8. Similar to Fig. 7, Fig. 8 represents the simulated output response of the signal Y for various input levels of the signal X. Fig. 8 indicates the improvement of overload performance in accordance with a decrease in the interstage gain scale factor h_{c1} , yet at the cost of S/N ratio. A comparison of Fig. 8 to Fig. 7 illustrates the advantage in using a cascaded 2:2 arrangement. Specifically, a cascaded 2:2 modulator achieves significantly higher S/N ratios via a given interstage gain scale factor. Given a smaller interstage gain scale factor, the cascaded 2:2 arrangement can achieve better overload performance. For example, in Fig. 8, the cascaded 2:2 arrangement indicates a linear roll-off (i.e., overload) at -2.0 dB input level with a $1/8$ interstage scale factor. While S/N and overload performance are significantly improved in the cascaded 2:2 arrangement, overload nonetheless remains near input peak values.

Regardless of the delta-sigma configuration, whether it is a single stage type with input gain

scaling, a cascaded 2:1 modulator with interstage gain scaling and noise cancellation, or a cascaded 2:2 modulator with interstage gain scaling and noise cancellation, the results remain the same. That is, the modulators get overloaded as analog input voltages approaches the peak or full scale value. Figs. 2, 7 and 8 all shows that overload occurs before the input signal X reaching full scale. For example, if the analog input value reaches a voltage near the reference voltage, a conventional modulator will change from a linear operation to a non-linear operation. To further clarify, using an exemplary of +3.0 v. Vref and -3.0 v. Vref feedback levels, an analog input level approaching the peak voltages (e.g., exceeding in absolute value $\pm 2.9\text{v.}$) of Vref will cause the modulator to experience an overload condition regardless of the modulator configuration. Attempts to alleviate the overload by gain scaling the feedback Vref voltage or by scaling the interstage gain merely reduces the S/N ratio as a trade off for improved overload performance. It would be desirable to further enhance overload performance without detriment of S/N ratio. Thus, improvements for conventional modulators entail a configuration which does not enter overload before the analog input signal

reaching the peak value. Of further importance, is the desire for a configuration which can maintain a high S/N ratio throughout the dynamic range of the modulator and having an input signal which can
5 extend up to and exceed the peak value level of the feedback reference voltages.

DISCLOSURE OF THE INVENTION

10 The problems outlined above are in most cases solved by an improved modulator configuration of the present invention. That is, the delta-sigma modulator of the invention utilizes a local feedback arrangement which selectively controls a local
15 integrator circuit placed subsequent to a first integrator circuit. The local feedback arrangement is thereby not necessarily used for the first integrator, but for an integrator subsequent to the first integrator, i.e., for a second-order
20 integrator in a cascaded 2:x configuration, for a second and/or a third order integrator in a cascaded 3:x configuration, etc. Thus, the local feedback is preferably not placed on the first-order integrator in the first stage. The local feedback is used to
25 control the output of each local integrator by use

of a negative local feedback that includes an individual quantizer.

Broadly speaking, the present invention contemplates a delta-sigma modulator. The delta-sigma modulator includes first and second integrators coupled in series between an analog input node and an analog output node. A first summing node is coupled between the analog input node and the first integrator. A second summing node is coupled between the first integrator and the second integrator. A local feedback loop is coupled preferably only between the analog output node and the second summing node. The local feedback loop comprises a first quantizer coupled in series with a first reference voltage selector. A plural-order feedback loop (or a global feedback loop) may be coupled between the analog output node and the input of the delta-sigma modulator, preferably the first summing node. If desired, the global feedback loop may also be coupled between the analog output node and both of the first and second summing nodes. The global feedback loop comprises a second quantizer coupled in series with a second reference voltage selector. The global feedback loop is dissimilar from the local feedback loop, wherein the global feedback loop feeds back to the summing nodes

preceding the first and second integrators.

Conversely, the local feedback loop merely feeds back the output of one integrator to the summing node preceding that integrator, but not to the
5 summing nodes preceding other integrators.

The present invention further contemplates a plural-order, cascaded analog-to-digital converter. The analog-to-digital converter includes a first stage of at least two primary integrators
10 electrically coupled in series between an analog input node and a first analog output node. At least one local feedback loop is coupled across respective primary integrators except for a first-order integrator with which the analog input node is
15 coupled. In other words, the local feedback loops are coupled across each of the primary integrators except for the first-order integrator. The primary integrators which receive the feedback via the local feedback loop are the second-order, third-order,
20 etc. integrators in the first stage. If desired, other local feedback loops can be arranged across various integrators in a second stage as well. A second stage of at least one secondary integrator is electrically coupled between the first analog output
25 node and a second analog output node. A noise cancellation circuit is coupled to receive quantized

signals of the first analog output node in the local
feedback loop (or loops), and of the second analog
output node. The noise cancellation circuit
produces a digital output out of the quantized
5 signals.

Other objects and advantages of the invention
will become apparent upon reading the following
detailed description and upon reference to the
accompanying drawings.

10

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a single stage,
second-order delta-sigma modulator of conventional
15 design;

Fig. 2 is a graph of S/N plotted as a function
of the analog input level for the modulator shown in
the Fig. 1;

Fig. 3 is a block diagram of a cascaded 2:1
20 delta-sigma modulator having a second-order first
stage and a first-order second stage of conventional
design;

Fig. 4 is a block diagram of a noise
cancellation circuit used in conjunction with the
25 modulator shown in the Fig. 3;

Fig. 5 is a block diagram of a cascaded 2:2 delta-sigma modulator having a second-order first stage and a second-order second stage of conventional design;

5 Fig. 6 is a block diagram of a noise cancellation circuit used in conjunction with the modulator shown in the Fig. 5;

Fig. 7 is a graph of S/N plotted as a function of analog input level and interstage gain scale factor for the modulator and noise cancellation circuit shown in the Figs. 3 and 4;

10

Fig. 8 is a graph of S/N plotted as a function of analog input level and interstage gain scale factor for the modulator and noise cancellation circuit shown in the Figs. 5 and 6;

15

Fig. 9 is a block diagram of a single stage, second-order delta-sigma modulator having a local feedback loop provided for each order;

Fig. 10 is a block diagram of a noise cancellation circuit used in conjunction with the modulator shown in the Fig. 9;

20

Fig. 11 is a block diagram of a cascaded 2:2 delta-sigma modulator having a local feedback loop provided only for a second-order in a first stage;

Fig. 12 is a block diagram of a noise cancellation circuit used in conjunction with the modulator shown in the Fig. 11;

Fig. 13 is a graph of S/N plotted as a function of analog input level for mismatch errors between the local feedback gain coefficient and noise cancellation gain coefficient of the modulator and noise cancellation circuit shown in the Figs. 9 and 10;

Fig. 14 is a graph of S/N plotted as a function of analog input level, and is dependent upon the presence or absence of local feedback, for the modulator and noise cancellation circuit shown in the Figs. 11 and 12; and

Fig. 15 is a circuit diagram of a the second integrator within the first stage of a cascaded delta-sigma modulator having a tri-level reference voltage selector controlled by the local feedback loop provided in the cascaded delta-sigma modulator in the Fig. 11.

PREFERRED EMBODIMENT OF THE INVENTION

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in

the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form

5 disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

10 To ensure stable operation and minimize instances of overload, it is necessary that feedback loops are used besides conventional feedback loops. Namely, the present invention is directed to supplementary feedback loops (or local feedback
15 loops). The local feedback loops are used in addition to the conventional plural-order (or global) feedback loops associated with all delta-sigma modulators. The local feedback loop is defined as a feedback loop which extends from the
20 output of an integrator back to the input of that same integrator. Thus, the local feedback loop does not extend back from the output of one integrator to a prior-connected other integrator, as is the normal case in the global feedback loop.

25 The local feedback loop is derived in consideration of the shortcomings associated with a

global feedback loop that includes plural-order integrators. Delta-sigma modulators which rely solely upon the global feedback loop is more susceptible to overload at inputs close to full
5 scale. This is because of the plural-order integration of a analog signal that makes the input of a quantizer grow more rapidly in correspondence to the increase of an input level.

Referring now to Fig. 9, a single stage delta-
10 sigma modulator having both global feedback and local feedback loops is shown. The global feedback loop is of the conventional design and is denoted as reference numeral 101. A global feedback loop 101 includes a quantizer 102 and a digital-to-analog
15 conversion circuit (or bi-level reference voltage selector) 104. The quantizer 102 and reference voltage selector 104 are coupled between the output of a integrator 106 and the inputs of two amplifiers 110 and 112. At the input of a first integrator 108
20 is a first summing node 111, and at the input of the second integrator 106 is a second summing node 114. A first local feedback loop 116 is coupled from the output of the first integrator 108 to the first summing node 111. Additionally, a second local
25 feedback loop 118 is coupled between the output of the second integrator 106 and the second summing

node 114. The first local feedback loop 116 and second local feedback loop 118 each include an analog-to-digital conversion circuit (quantizer) 120 and 122, respectively, and further include a
5 digital-to-analog conversion circuit (reference voltage selector) 124 and 126 respectively.

The purpose of using the local feedback loop on each integrator is to maintain the corresponding integrator's output voltage within a certain range
10 so that the global feedback loop will not overload. Each local feedback loop 116 and 118 prevents associated individual integrators from saturating so that the output voltages of respective integrators are within proper ranges. The outputs of individual
15 integrators 106 and 108 are continuously examined by the quantizer 120 and 122. If the integrator outputs exceed the proper ranges, negatively feeding back the outputs of the reference voltage selectors 124 and 126 controlled by the outputs of those
20 integrators returns corresponding integrators to their normal operating ranges. Respective quantizer outputs of both local feedback loops are sent to a noise cancellation circuit shown in Fig. 10. The noise cancellation circuit in Fig. 10 indicates two
25 amplifiers 130 and 132 coupled to receive respective quantized signals Y_{1a} and Y_{1b} within each local

feedback loop. The noise cancellation circuit 128 further includes a differentiator 134 coupled to the output of the amplifier 132, and a series of delay circuits, "d"s, coupled to the outputs of the
5 amplifier 130 and differentiator 134. The delay circuits are necessary to maintain synchronized signals at the inputs of a noise cancellation summing node 138.

The operation of a delta-sigma modulator 100 and
10 noise cancellation circuit 128 is best described in reference to an overall transfer function. Specifically, the transfer function representing a digital output signal Y_1 is as follows:

$$15 \quad Y_1 = XZ^{-2} + (1-Z^{-1})^2 Q_1 - g_0 Z^{-2} Y_{1a} - g_2 (1-Z^{-1}) Z^{-1} Y_{1b}$$

(Eq. 6),

where $(1-Z^{-1})^2$ represents the second-order noise shaping function of series-connected integrators 106
20 and 108. Each local feedback loop 116 and 118 includes respective scale factors g_0 and g_2 used to scale the front end of the corresponding integrator. The amplifiers 110 and 112 also have scale factors, denoted as g_3 and g_1 , respectively.

25 The above equation 6 is derived by designating the scale factor g_3 to one and the scale factor g_1 to

two. When these scale factors g_1 and g_3 are given to the global feedback loop 101, the equation 6 indicates that the quantization noise within a signal Y_1 is directly fed to an output signal Y_1 ,
5 whereas the quantization noise within a signal Y_{1b} is fed through a noise shaping transfer function denoted as $1-Z^{-1}$. The noise cancellation circuit 128 receives the signals presented at Y_{1a} , Y_{1b} and Y_1 and produces a noise canceled digital output signal Y .
10 The transfer function representative of the noise cancellation circuit 128 is shown in a simplified form as follows:

$$Y = Y_1 + g_0'Z^{-2}Y_{1a} + g_2'Z^{-1}(1-Z^{-1})Y_{1b} \quad (\text{Eq. 7}),$$

15

where $1-Z^{-1}$ represents a first-order noise shaping function, Z^{-2} represents the two delay blocks (or delay times) at the output of the amplifier 130, and Z^{-1} represents the delay block at the output of the
20 integrator 134. Substituting the transfer function Y_1 of equation 6 into equation 7 presents the following transfer function.

$$Y = XZ^{-2} + (1-Z^{-1})^2Q_1 - g_0Z^{-2}Y_{1a} - g_2(1-Z^{-1})Z^{-1}Y_{1b} \\
25 \quad +g_0'Z^{-2}Y_{1a} + g_2'Z^{-1}(1-Z^{-1})Y_{1b} \quad (\text{Eq. 8})$$

As illustrated in equation 8, any mismatch between g_0 and g_0' will cause direct leakage of the quantized noise within the signal Y_{1a} to signal Y . Whereas, if any mismatch between scale factors g_2 and g_2' occurs, the signal Y_{1b} is substantially suppressed by the first-order noise shaping process (i.e., $1-Z^{-1}$ first-order noise shaping), so that the quantized noise component of the signal will leak out.

The basic operation of the local feedback loops 116 and 118 used in each integrator within a single stage plural-order delta-sigma modulator is described, in reference to an article by Moussavi, et al., "High-Order Single-Stage Single-Bit Oversampling A/D Converters Stabilized with Local Feedback Loops", IEEE Trans. on Circuits and Systems, Vol. 41, No. 1, January 1994, pp. 19-25 (herein incorporated by reference). Using a local feedback loop in each integrator, as described in Moussavi et al., is beneficial in preventing overload of a global feedback loop. Provided the non-idealities of each integrator 106 and 108 can be controlled, provided amplifiers scale factors g_0 and g_2 properly match with respective scale factors g_0' and g_2' of the noise cancellation circuit, and further provided the scale factors g_3 and g_1 of the

global feedback loop properly match with a desired value, the single stage, dual local feedback configuration of Moussavi et al. will ideally function and bear the following transfer function:

5

$$Y = XZ^{-2} + (1-Z^{-1})^2 Q_1 \quad (\text{Eq. 9}),$$

where Q_1 represents the quantization error of the quantizer 102. The quantization error Q_1 , however,
10 is minimized by receiving noise shaping of a second-order transfer function $(1-Z^{-1})^2$. Accordingly, in an ideal situation, the digital output signal Y can include very little quantization noise associated with that signal, as indicated in equation 9.
15 However, in most instances, the ideal situation cannot be obtained.

The ideal transfer function of equation 9 cannot be always obtained in case of semiconductor fabrication process inferior, or erroneous design,
20 layout or manufacture of modulator 100 components. As shown above, for example, non-idealities of the amplifier g_0 will appear as direct noise leakage upon the digital output Y . To prevent overload in a second-order single stage configuration, the second
25 and first local feedback loops (feedback loops 118 and 116) must be activated at input levels of

approximately -10 dB to the full scale (0.0 dB) and
-8.0 dB to the full scale, respectively. Local
feedbacks can suppress only the output swing of the
corresponding integrator. As far as the first local
5 feedback, a first-order integration function will
still remain within the signal path between the
analog input and the quantizer. With first-order
integration of the analog input as the quantizer
input, the global loop will still overload.

10 Therefore, overload can not be prevented in a
second-order, single stage configuration without
activating the first feedback loop (feedback loop
116). Since the quantization noise leakage of the
first feedback loop 116 is severe and direct upon
15 the digital output Y, only the input levels before
the activation of the first local feedback loop are
considered as the normal operating range. In
addition, the first local feedback circuit will
become another analog noise source, the noise from
20 which will become a new noise source converted to
the analog input when implemented by actual
circuits. Further details regarding operation
ranges of the first and second local feedbacks are
provided hereinbelow.

25 Turning now to Fig. 11, a block diagram of a
cascaded 2:2 delta-sigma modulator 200 according to



the present invention is shown. The modulator 200 includes first and second stages 202 and 204, respectively. It is understood that the stage 202 includes a minimum of two-orders of integration, and
5 that the stage 204 contains a minimum of one-order of integration. Accordingly, the stage 202 includes a first integrator 206 and a second integrator 208, whereas the stage 204 includes a first integrator 210 and a second integrator 212. The first
10 integrator 206 of the stage 202 produces an analog output signal fed to the input of the second integrator 208. The analog input signal to the second integrator 208 is denoted as A_{in} . The second integrator 208 produces an analog output signal
15 denoted as A_{out} . The output signal is quantized by a quantizer 102 equally configured as shown in Fig. 9, and fed back to a first summing node 221 and a second summing node 222 via a digital-to-analog conversion circuit 104. The amplifier 112 is
20 designed to have a scale factor g_1 , wherein g_1 is preferably defined as two. The quantizer 102, digital-to-analog conversion circuit 104 and amplifier 112 constitute a global feedback loop 101, similar to that of Fig. 9.

25 The cascaded arrangement of Fig. 11 purposefully avoids using a local feedback loop between the

output of the first integrator 206 and the input of the first integrator 206 (or first summing node 221 of the first integrator 206). Instead, the modulator 200 of Fig. 11 uses a feedback loop 220
5 coupled between the output and the input of the integrator 208, via a second summing node 222. The local feedback loop 220 includes a quantizer 224 and a digital-to-analog conversion circuit (reference voltage selector) 226. The local feedback loop 220
10 functions to detect an overload condition at the output of the second integrator 208 (or any subsequent order integrators), and to produce a local feedback signal at the output of the selector 226 which feeds back a compensating signal to the
15 input of the integrator 208. The quantizer 224 of the local feedback loop 220 generates the digital code representative of the compensating signal, which maintains the second-order integrator output within a desired, specified range. By monitoring
20 the output of the second integrator 208 and feeding back the quantized signal of the second-order integrator, the local feedback loop prevents the integrator output voltage from increasing in order to avoid overload of the second stage 204.

25 The local feedback loop 220 and associated circuitry can be duplicated, and can be used in

plural-order integrators within a cascaded analog-to-digital converter. For example, a $x:y$ cascaded converter may have $X-1$ local feedback loop arranged across each integrator in the first stage. The only
5 integrator in the first stage which purposefully does not use local feedback is the first-order integrator (i.e., the integrator which receives the analog input signal X). All orders of the second stage are designed for having no local feedback. A
10 local feedback loop is not needed for the first-order in the first stage since it is not necessary to eliminate overload from the first stage. Any quantization noise from the first stage will be canceled by the noise cancellation circuit.

15 Given a proper selection of interstage gain scaling by providing a local feedback loop for subsequent orders in the first stage, the second stage is prevented from entering overload. In case of a $x:y:z$ cascaded converter, $X-1$ local feedback loops
20 are used in the first stage, y (or $y-1$) local feedback loops are used in the second stage, and z (or $z-1$) local feedback loops are used on the third stage, etc.

The first stage 202 in Fig. 11 is coupled to the
25 second stage via an interstage summing node 232. Amplified outputs from the selector 104 as well as



integrator 208 are fed to the summing node 232. Accordingly, amplifier 234 operates preferably at a scale factor which is the product of the inverse of scale factors for amplifiers 228 and 230. An
5 amplifier 236 operates at a scale factor of 0, 1 or 2 depending upon what is fed to the stage 204 from the stage 202 via the summing node 232, namely data, noise or a combination of the data and the noise, respectively. The output of the interstage summing
10 node 232 is scaled by scale factor h_{c1} of an amplifier 238. The scale factor h_{c1} of the amplifier 238 is set at less than one, preferably less than one half in order to prevent the second stage from overloading without use of a local
15 feedback in the first-order integrator in the first stage. Scaled output from the summing node 232 is fed to a first summing node 240 in the stage 204, along with a global feedback signal within a global feedback loop 101'. The second stage 204 is
20 identical in configuration with the first stage 202, except for having no local feedback loop such as feedback loop 220 in the stage 202. Both in the first and second stages 202 and 204, the global feedbacks of unity scale factor are utilized to the
25 first summing nodes 221 and 240. Moreover, scaling to the second feedback nodes 222 and 242 is

performed preferably at a scale factor of two. The cascaded arrangement shown in Fig. 11 is illustrative of a 2:2 cascaded converter, however, it is understood that additional orders can be added to the first stage, second stage, or further stages within an overall configuration. for example, a 3:1 cascaded modulator having a third-order integrator in a first stage and a first-order integrator in a second stage is also intended to. Regardless of the configuration, it is important that the first-order within the first stage does not contain a local feedback loop, and each subsequent order contains a local feedback loop. The spirit and scope of the present invention device thereby contemplates any cascaded arrangement having at least two orders in the first stage, and at least one order in the subsequent stages.

Turning now to Fig. 12, a block diagram of a noise cancellation circuit 260 is shown. The circuit 260 is designed to cancel quantized noise generated from all the stages but the last stage of the modulator 200. Thus, the circuit 260 is used to cancel noise generated by all quantizers within the first stage 202. The only remaining noise with the digital output signal Y is that of the quantized noise produced by a quantizer 244 in second stage

204. The circuit 260 receives the quantized output signals Y_{1b} , Y_1 and Y_2 from the modulator 200. The quantized signal Y_{1b} of the local feedback loop 220 is singly differentiated by a differentiator 262 in the circuit 260. Various delay circuits designated with a "d" reference are coupled to the output of the differentiator 262 to synchronize input signals at the noise cancellation summing node 264 in the time domain. The outputs Y_1 and Y_2 of the quantizers 102 and 244 in the global feedback loops are double differentiated by a differentiator 266. The summing node 264 adds the double differentiated global feedback loop outputs to the singly differentiated local feedback loop output.

Referring now to Fig. 13, a graph of S/N plotted as the function of the analog signal X input level is shown. Fig. 13 represents the S/N ratio simulation when the single stage second-order modulator 100 in Fig. 9 is coupled to the noise cancellation circuit 128 in Fig. 10. The S/N ratio is dependent not only upon the input level, but also upon the mismatch errors of the scale factors g_0 and g_2 within the first and second local feedback loops. Fig. 13 shows that a 1.0% mismatch error between g_0 of the first local feedback 116 in Fig. 9 and g_0' of the noise cancellation circuit amplifier 130 in Fig.

10 causes serious quantization noise leakage
problems at an input level of approximately -8.0 dB.
Fig. 13 also shows that a 1.0% mismatch error
between g_2 and g_2' in Figs. 9 and 10 causes somewhat
5 less serious quantization noise leakage problems at
an input level of approximately -4.0 dB.

As shown in Fig. 13, the significant increase in
noise leakage upon the output signal Y occurs if
there is any mismatch between amplifier gain scale
10 factors g_0 and g_2 relative to g_0' and g_2' . Fig. 13
shows that the first-order local feedback loop 116
in Fig. 9 is activated at approximately -8.0 dB to
the full scale. The second-order local feedback 118
is active before the first local feedback is
15 activated, given a rising input voltage to a peak
value. The second local feedback, however,
maintains a greater degree of linearity relative to
the activated first local feedback. The linearity
difference primarily depends upon whether the
20 leakages of respective first and second local
feedbacks influence directly to or through first-
order noise shaping. The result shown in Fig. 13 is
explanatory of the transfer function shown by
equation 8. Direct leakage is represented in
25 equation 8 as a transfer function Z^{-2} , whereas the
first-order quantization noise leakage is

represented as a transfer function $1-Z^{-1}$. A combination of the transfer functions shown in equation 8 and the graph of Fig. 13 indicates the importance of the present invention. That is, the influence of mismatch errors can be substantially eliminated using the configuration of Figs. 11 and 12. A cascaded converter having only one local feedback at the second-order in the first stage substantially eliminates any direct leakage associated with a first local feedback. The elimination of direct leakage is due to eliminating the first local feedback and utilizing only a second (or possibly third, etc.) local feedback. Thus, the present invention prevents overload without the use of a first local feedback loop. A single loop (single stage) arrangement cannot achieve this condition. In a cascaded arrangement, the quantization noise within the first stage will be canceled provided the latter stage (second stage) is not in an overload condition. Appropriately scaling the amplifier 238 in Fig. 11, and further limiting the output signal level of the first stage by the function of the local feedback loop 220 avoids overload of the second or subsequent stages.

Fig. 14 illustrates simulation result of what is achieved by having a single local feedback loop in

the cascaded 2:2 converter with appropriate noise cancellation, shown in Figs. 11 and 12. A scale factor of less than 1/2 is chosen as the interstage gain scale factor. Fig. 14 illustrates, for
5 comparison purposes, S/N ratio as the function of the input level X both with and without a local feedback loop. It is important to note that not only the S/N ratio in Fig. 14 is higher than one in Fig. 13, but it is further important to note that
10 the S/N ratios depend upon whether the local feedback loop is used or not. If the local feedback is employed, the S/N ratio maintains a substantially linear slope all the way to the full scale (0.0 dB). In fact, Fig. 14 shows, by way of simulation, that
15 the overload is not only minimized when the local feedback is used but the overload is effectively eliminated. Still further, the arrangement of Fig. 11 achieves the illustrated result in Fig. 14 since g_0 and g_0' no longer exist and therefore any mismatch
20 and direct noise leakage will no longer occur.

Utilizing a local feedback in the second-order (second integrator) in the first stage 202 controls the output swing from the second integrator 208 in order to ensure that the resulting output signal
25 does not cause the overload of the second stage 204. Thus, controlling carefully the output from the

first stage through use of a local feedback, in many instances, eliminates the constraints of using an extremely small scale factor for the amplifier 238. If the scale factor (hc1) of the amplifier 238 is
5 made too small, there is a possibility that the S/N ratio correspondingly can be made too small as well.

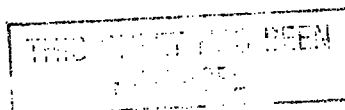
The quantizer 224 of the local feedback loop 220 in Fig. 11 can be designed as a bi-level or tri-level quantizer. It is preferable that the
10 quantizer 224 be made a tri-level quantizer which functions to detect overload and to produce one of three corresponding digital levels. The quantizer 224 can thereby be represented as a window comparator, for example, which produces -1 or +1
15 depending upon the polarity of the input voltage. When the integrator 208 operates within the operating range, quantizer 224 outputs 0 levels such that the local feedback loop 220 is not activated. Thus, if the integrator output exceeds the specified
20 boundaries, the quantizer produces a proper local feedback signal which forces the integrator to return to the normal operating range by the corresponding tri-level digital-to-analog circuit 226. The fully-differential architecture, well
25 known in the art, of the tri-level digital-to-analog circuit 226 can be implemented with a high degree of

linearity. A tri-level digital-to-analog circuit is used to minimize noise leakage at small signal inputs by providing primarily zero levels at those input values.

5 Turning now to Fig. 15, a circuit diagram of block 209 shown in Fig. 11 is illustrated. Fig. 15 illustrates a switched capacitor implementation of block 209. In a conventional switched capacitor arrangement, two independent switched capacitors are
10 required to sample the first integrator output A_{in} and to implement the tri-level local feedback D/A conversion circuit 226. If g_2 equals to one, same capacitance capacitors can be used for both the sampling of A_{in} and the local feedback. Since
15 capacitance are identical, this means that a common (shared) capacitor can be used for both functions, with a proper switching scheme. Fig. 15 illustrates a switched capacitor integrator wherein sampling A_{in} and implementing the local feedback D/A conversion
20 of tri-level are both performed. During a time ϕ_1 , A_{in} is sampled by a capacitor Cs_1 . During a time ϕ_2 , the left side of the capacitor is connected to $\pm V_{ref}$ or 0 depending on the output of the quantizer in the local feedback, instead of ground.
25 By this sequence, the shared capacitor performs the sampling of A_{in} during the time ϕ_1 and tri-level D/A

converting during the time ϕ_2 . The charge corresponding to the difference between A_{in} and the tri-level D/A conversion circuit output will be transferred to an integrating capacitor C_{int} at the
5 time ϕ_2 . Since the component that determines the gain of sampled A_{in} and the gain of the tri-level D/A is common, no mismatch is present. This means that the amplifier g_2 of the local feedback is ideal. If so, the effect of the quantization noise leakage
10 in the second local feedback is eliminated.

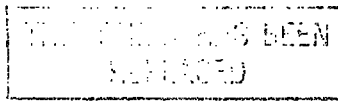
It will be appreciated by those skilled in the art having the benefit of this disclosure that the invention is believed to be capable of applications with any oversampled analog-to-digital converter.
15 Furthermore, it is also to be understood that the invention shown and described is to be taken as presently preferred embodiments. Various modifications and changes may be made to each and every processing components as would be obvious to a
20 person skilled in the art without departing from the spirit and scope of the invention as set forth in the claims. It is intended that the following claims be interpreted to embrace all such modifications and changes, and according, the
25 specification and drawings are to be regarded in an illustrative rather than a restrictive sense.



CLAIMS

1. A delta-sigma modulator comprising;
a first and a second integrators coupled in
5 series between an analog input node and a first
analog output node,
a first summing node coupled between said analog
input node and said first integrator,
a second summing node coupled between said first
10 integrator and said second integrator,
a local feedback loop including a first
quantizer for quantizing a signal at said first
analog output node, and a first reference voltage
selector for providing said second summing node with
15 a first analog signal based upon an output from said
first quantizer, and,
a plural-order feedback loop including a second
quantizer for quantizing said signal at said first
analog output node, and a second reference voltage
20 selector for providing at least said first summing
node with a second analog signal based upon an
output from said second quantizer.
2. A delta-sigma modulator set forth in claim 1;





wherein said first quantizer is configured for producing a digital signal capable of representing a tri-level logic value.

- 5 3. A delta-sigma modulator set forth in claim 1; further comprising a third summing node coupled to said first analog output node,

 at least a third integrator coupled between said third summing node and a second analog output node,
10 and,

 a feedback loop including a third quantizer for quantizing a signal at said second analog output node, and a third reference voltage selector for providing said third summing node with a third
15 analog signal based upon an output from said third quantizer.

4. A delta-sigma modulator set forth in claim 3; further comprising an interstage summing node
20 between said first analog output node and said third summing node, for adding an output signal at said first output node to an output signal from said second reference voltage selector.

- 25 5. A delta-sigma modulator set forth in claim 3;

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further comprising an amplifier with a scale factor of less than one, between said first analog output node and said third summing node.

5 6. A delta-sigma modulator set forth in claim 3;
further comprising a noise cancellation circuit for
receiving outputs from said first quantizer and said
second quantizer and said third quantizer, wherein
said noise cancellation circuit has a function of
10 canceling quantization noises generated by said
first and second quantizers.

7. A delta-sigma modulator comprising;
a first, a second and a third integrators
15 sequentially coupled in series between an analog
input node and a first analog output node,
a local feedback loop including a first
quantizer for quantizing a signal at said first
analog output node, and a first reference voltage
20 selector for providing a first analog signal based
upon an output from said first quantizer, wherein
said local feedback loop adds said first analog
signal to an input of said third integrator,
a plural-order feedback loop including a second
25 quantizer for quantizing a signal at said first
analog output node, and a second reference voltage



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selector for providing a second analog signal based
upon an output from said second quantizer, wherein
said plural-order feedback loop adds said second
signal at least to an input signal of said first
5 integrator,

an interstage summing node for adding an output
signal at said first output node to said second
analog signal,

at least a fourth integrator coupled between
10 said interstage summing node and a second analog
output node, and,

a feedback loop including a third quantizer for
quantizing a signal at said second analog output
node, and a third reference voltage selector for
15 providing said fourth integrator with a third analog
signal based upon an output from said third
quantizer, wherein said feedback loop adds said
third analog signal at least to an input signal of
said fourth integrator.

20

8. A delta-sigma modulator comprising;

plural integrators coupled in series between an
analog input node and an analog output node,

a quantizer for quantizing a signal at said
25 analog output node,

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a reference voltage selector for providing an analog signal based upon an output from said quantizer,

a summing node for adding an output signal from
5 said reference voltage selector to at least one of said plural integrators inputs, and,

a switched capacitor integrator configured for having a capacitor in common use both for sampling an input signal to said integrators, and for
10 sampling a reference voltage of said reference voltage selector.

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