

## DIRECT DIGITAL FREQUENCY SYNTHESIS ENABLING SPUR ELIMINATION

The present invention relates to direct digital frequency synthesis.

5 Direct digital frequency synthesis (DDFS) consists of generating a digital representation of a desired signal, using logic circuitry and/or a digital computer, and then converting the digital representation to an analog waveform using a digital-to-analog converter (DAC). Such systems can be compact, low power, and can provide very fine frequency resolution with virtually instantaneous switching of frequencies.

10 A known DDFS system is shown in Figure 1. A digital modulation signal is input to DDS accumulator logic, the output of which indexes into a read-only memory (ROM). An output signal of the ROM is converted to an analog signal by a DAC. An output signal of the DAC may be smoothed using a filter (not shown) to produce a periodic (e.g., sinusoidal) signal. The DDFS of Figure 1 is  
15 exemplified by U.S. Patent 4,746,880, incorporated herein by reference.

Other DDFS variations are shown in Figure 2, Figure 3 and Figure 4. In Figure 2, the DDFS of Figure 1 is incorporated into a conventional PLL structure including a phase/frequency detector (PFD), an analog loop filter and a voltage controlled oscillator (VCO). In Figure 3, the ROM and the DAC of Figure 2 are  
20 omitted, and the most significant bit (MSB) from the DDS block is input directly to the PFD. In Figure 4, an output signal of the DDS block is filtered using a direct time filter as described in U.S. Patent 5,247,469, incorporated herein by reference.

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One of the challenges of DDFS has been to generate a clean, precisely-modulated waveform. Because of limited time resolution and edge misalignment, spurious output signal transitions ("spurs") occur.

Precision modulation is also a problem in conventional analog frequency synthesizers using a PLL. The problem occurs that the PLL treats signal modulation as drift and attempts to cancel the modulation. Circuit arrangements devised in an attempt to overcome this problem are shown in Figure 5 and Figure 6. In Figure 5, a summing node is provided following the loop filter to which a modulation signal is applied. Details of the summing node are illustrated in exploded view. In Figure 6, showing the Ewart modulator, a resistive divider network is inserted into the ground reference of the loop filter, and a modulation signal is applied to the resistive divider network as shown. In effect, the ground reference of the loop filter is shifted by the modulation signal, resulting in an output signal of the loop filter being shifted by the amount of the modulation. In Figure 7, a modulation signal is capacitively coupled to a node of the loop filter circuit. The foregoing circuit arrangements do not enjoy the benefits of DDS.

There remains a need for a synthesizer having the benefits of DDS but that is capable of generating a clean, precisely-modulated waveform.

The present invention, generally speaking, provides improved methods of generating clean, precisely-modulated waveforms, at least partly using digital techniques. In accordance with one aspect of the invention, a "difference engine" is provided that produces a digital signal representing the frequency error between a numeric frequency and an analog frequency. The frequency error may be digitally integrated to produce a digital signal representing the phase error. The difference engine may be incorporated into a PLL, where the analog frequency is that of an output signal of a VCO of the PLL. Direct modulation of the PLL output signal may be performed numerically. By further providing an auxiliary modulation path and performing calibration between the direction modulation path and the auxiliary modulation path, modulation characteristics may be separated

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from loop bandwidth constraints. In particular, the loop bandwidth of the PLL may be made so low as to reduce spurs (usually associated with DDS techniques) to an arbitrarily low level. A loop filter of the PLL may be realized in digital form. Using a digital loop filter would ordinarily require use of a high-resolution DAC. Various techniques are described for reducing the resolution requirements of the DAC.

Figure 1 is a block diagram of a known DDFS;

Figure 2 is a block diagram of a known PLL using DDS;

Figure 3 is a block diagram of a known alternative PLL using DDS;

Figure 4 is a block diagram of a DDS synthesizer using a direct time filter;

Figure 5 is a circuit diagram of a portion of a synthesizer illustrating one known modulation technique;

Figure 6 is a circuit diagram of a portion of a synthesizer illustrating another known modulation technique;

Figure 7 is a circuit diagram of a portion of a synthesizer illustrating still another known modulation technique;

Figure 8 is a diagram of a digital "difference engine" for use in a synthesizer;

Figure 9 is a diagram illustrating in greater detail the DDS block of Figure 8;

Figure 10 is a diagram illustrating in greater detail the Data Sample block of Figure 8;

Figure 11 is a timing diagram illustrating operation of the Data Sample block of Figure 10;

Figure 12 is a timing diagram illustrating a possible temporary metastable condition of the Data Sample block of Figure 10;

Figure 13 is a diagram of a basic PLL structure using the difference engine of Figure 8;

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Figure 14 is a diagram of a PLL structure having a digital modulation input and an auxiliary modulation path;

Figure 15 is a diagram of a modified PLL structure;

5 Figure 16 is a diagram of a PLL structure having a digital loop filter followed by a DAC;

Figure 17 is a diagram of a PLL structure in which a digital FIR filter is used for calibration;

Figure 18 is a diagram of a PLL like that of Figure 16 but having an auxiliary modulation path coupled to the DAC;

10 Figure 19 is a diagram of a PLL structure using a differential DAC of comparatively low resolution;

Figure 20 is a diagram of an analog integrator that may be used in the PLL of Figure 19;

Figure 21 is a diagram of a PLL structure having a preset circuit;

15 Figure 22 is a diagram of a further PLL structure; and

Figure 23 is a diagram of an alternative construction of the PLL structure of Figure 22.

Referring now to Figure 8, a diagram is shown of a difference engine in accordance with one aspect of the present invention. The overall function of the  
20 difference engine is to produce digital data streams representing the frequency error and (optionally) the phase error between an analog frequency and a numeric frequency. A reference clock and a numeric frequency are input to a DDS block. In response to the reference clock and the numeric frequency, the DDS block outputs a digital stream representing the numeric frequency. Similarly, the  
25 reference clock and an analog frequency are input to a Data Sample block. In response, the Data Sample block outputs a digital stream representing the analog frequency. The two digital streams are summed with opposite polarities. The

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resulting summation is a digital stream representing the frequency error between the analog frequency and the numeric frequency, the digital stream having values of +1, -1 and 0. If the analog frequency and the numeric frequency are identical, then the digital stream representing the frequency error will be all zeros. Digital  
5 integration of the frequency error may be performed using a digital integrator to produce a digital stream representing the phase error between the analog frequency and the numeric frequency.

The DDS block may be realized as a simple accumulator, for example, as shown in Figure 9. Alternatively, the DDS block may be second order instead of  
10 first order. The Data Sample block may be realized as shown in Figure 10. In the illustrated embodiment, it is assumed that the ratio of the clock signals is such that no more than one rising edge of the faster clock will occur during a single period of the slower clock. In other embodiments, this assumption need not apply.

The capture circuit includes an input portion 1001 and an output portion  
15 1003. The input portion includes two sections Ch1 and Ch2 that must be carefully matched to minimize errors. Each section comprises a chain of two or more D flip-flops coupled in series. In the following description, the same reference numerals will be used to reference the respective flip-flops themselves and their respective output signals.

20 Within each section, the first flip-flop in the chain is clocked by a sampled clock signal  $F_x$ . The succeeding flip-flops in the chain are clocked by a sampling clock signal  $F_s$ . The D input of the first flip-flop Q1 in the upper section is coupled to the  $\overline{Q}$  output of the same. The D input of the first flip-flop in the lower section is coupled to the Q output of the first flip-flop in the upper section. The  
25 remaining flip-flops in both sections are coupled in series—i.e., Q to D, Q to D.

The function of the input portion is to 1) produce two signals, logical inverses of one another, that transition on rising edges of the clock signal  $F_x$ ; 2) to latch the values of the two signals on the rising edge of the clock signal  $F_s$ ; and 3) to detect transitions from one clock to the next. The intermediate stages Q3 and Q4

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may be required to minimize metastability resulting from the asynchrony of the two clock signals, and in fact multiple such stages may be desirable in a particular design.

The output portions includes, in an exemplary embodiment, three two-input  
5 NAND gates. Respective NAND gates N1 and N2 are coupled to the D and  $\bar{Q}$  signal of the final flip-flop stages of the input sections. Output signals of the NAND gates N1 and N2 are combined in the further NAND gate N3 to form the final output of the capture circuit.

The function of the output portion is to detect a change in the input clock  
10 signal level from one sample clock to the next in either of two channels formed by the two input sections. The two input sections function in a ping-pong fashion, alternately detecting changes in the input clock signal level.

Operation of the capture circuit of Figure 10 may be more fully appreciated  
with reference to the timing diagram of Figure 11. The first stages of the two  
15 channels form inverse signals Q1 and Q2 approximately coincident with (but slightly delayed from) rising edges of the input clock signal. The signals Q3 and Q4 are formed by sampling the signals Q1 and Q2, respectively, in accordance with the sample clock. The signals Q5 and Q6, respectively, are delayed replicas of the signals Q3 and Q4. The NAND gates together realize the logic function X  
20  $= Q3.\bar{Q5} \vee Q4.\bar{Q6}$ .

In the example of Figure 11, the illustrated signals are all idealized  
square-wave signals. In actuality, the signals will have finite rise and fall times.  
The possible effect of the finite rise and fall times of the signals Q1 and Q2 and  
the asynchrony of the circuit is metastability, as illustrated in Figure 12. Here, the  
25 signals Q3 and Q5 and the signals Q4 and Q6 are each in an indeterminate state for one cycle. The resulting output of the circuit may or may not be correct. However, because the decision was a "close call" to begin with, the effect of an occasional erroneous decision on the overall operation of the circuit is negligible. The time window of instability is reduced by increasing the overall gain in the path. If the

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gain in Q3 and Q9 is sufficient to reduce the probability of an error to an acceptable level, then no additional circuitry is required. If not, then additional circuitry will be required to increase the gain.

5 If the Data Sample block is realized as shown in Figure 10, then if the DDS block is second order, the digital streams will not match exactly even when the analog frequency and the numeric frequency exactly coincide. A second-order construction of the DDS block may nevertheless be beneficial in reducing tonal noise.

10 The difference engine of Figure 8 may be used to realize a basic PLL as shown in Figure 13. The phase error signal is input to a charge pump having a pull-up current source and a pull-down current source. Depending on the current value of the digital phase error stream, one or the other current source is activated, or neither current source is activated. An output signal of the charge pump is input to a loop filter. An output of the loop filter is input to a voltage-controlled  
15 oscillator (VCO). Finally, an output of the VCO is input to the Data Sample block as the analog frequency, closing the loop.

As compared to a PLL using a conventional phase/frequency detector (PFD), the PLL of Figure 13 has the advantage that it achieves smooth lock and will not "slip lock."

20 In the PLL of Figure 13, the numeric frequency may be modulated to achieve modulation. This "direct modulation" is subject to loop bandwidth constraints as described in relation to the prior art. Referring to Figure 14, a PLL having improved modulation properties is shown. A numeric modulation input is applied to the difference engine for direct modulation. In addition, the numeric  
25 modulation input is applied to a DAC. An output voltage produced by the DAC is applied to a node of the loop filter. The PLL of Figure 13 has the property that if the direct modulation gain is exactly matched in the auxiliary modulation path, then the output frequency of the PLL can be changed without changing the closed-loop modulation voltage  $V_{Mcl}$ . This property in turn implies that modulation

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is not subject to loop bandwidth constraints. The loop bandwidth may be set to an arbitrarily low level, for example, allowing DDS spurs to be filtered down to any desired level.

Referring to Figure 15, to allow the direct modulation gain to be matched  
5 in the auxiliary modulation path, a multiplier is provided. The multiplier applies a scale factor to the numeric modulation input prior to its application to the DAC. A method by which the appropriate scale factor may be determined is described hereafter.

Referring still to Figure 15, to achieve a low loop bandwidth (e.g., for spur  
10 reduction), large-valued capacitors are required to be used within the loop filter. Large capacitors are bulky and costly. Furthermore, the VI characteristics of large capacitors exhibit undesirable non-linearities due to dielectric absorption. A low loop bandwidth may be obtained instead using a digital loop filter followed by a DAC as shown in Figure 16, in which the separate modulation path has been  
15 omitted.

Referring to Figure 17, the scale factor described previously may be determined by measuring a maximum frequency step using a digital filter. To do so, the minimum numeric frequency is first applied to the difference engine. Then the maximum numeric frequency is applied. The frequency error signal produced  
20 by the difference engine is filtered using a finite impulse response filter (FIR), for example. The FIR filter measures the maximum frequency step. The appropriate scale factor may be determined by dividing the observed maximum frequency step by the desired maximum frequency step. Preferably, calculation of the scale factor is iterated multiple times. For each successive iteration, the value obtained for the  
25 scale factor will more closely approximate the scale factor required for exact matching. Calibration may be performed at power-on and may optionally be performed thereafter at intervals or as required.

Referring to Figure 18, in the case of a digital filter followed by a DAC, the auxiliary modulation path may be achieved using a summing DAC. An analog

modulation signal is input directly to the DAC along with the output of the digital loop filter. The embodiment of Figure 18 avoids the need for large-value capacitors. Depending on application requirements, however, the embodiment of Figure 18 may require a high-resolution DAC. In the case of a VCO having a sensitivity of 40MHz/V, for example, if accuracy is desired, then a 20-bit DAC would be required. Such resolution is difficult and expensive to achieve. Various different techniques may be used to reduce the resolution requirements of the DAC. Two such techniques are illustrated in Figure 19 and Figure 21, respectively.

Referring to Figure 19, the need for a high-resolution DAC may be avoided using a differentiating DAC followed by an analog integrator. As compared to a 20-bit DAC in Figure 18, in the embodiment of Figure 19, the DAC may be a 12-bit Sigma-Delta DAC, for example. The analog integrator may be realized as a charge pump coupled to an integrating capacitor as shown in Figure 20.

Referring to Figure 21, a charge pump has associated with it a tuning capacitor and a PRESET input. A voltage from a modulation DAC is applied through a resistive divider to a bottom plate of the tuning capacitor. If the voltage from the modulation DAC is highly attenuated by the resistive divider, then the DAC may be of comparatively low resolution, e.g., 14 bits. In Figure 21, as in Figure 19, the upper (main loop) DAC is a differential DAC that produces a derivative of the desired voltage, which derivative is integrated by operation of the charge pump and capacitor to produce a voltage that is applied to the VCO. The circuit of Figure 21 is especially well-suited for cellular applications, for example, in which the transmitter jumps to a particular band in order to transmit a short burst. To do so, a preset signal is applied to the preset circuit to cause the PLL to jump to the desired band. The preset signal is then removed, after which a burst is then transmitted. The same sequence of events then repeats some time later. The circuit of Figure 21 assumes a time-multiplexed manner of operation, since

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leakage from the tuning capacitor will result in frequency drift over prolonged periods of time.

Better noise characteristics and lower driver requirements may be achieved using a modified circuit, shown in Figure 22. The circuit of Figure 22 uses a modulation injection scheme similar to that of Figure 7. Referring to Figure 22, a difference engine receives an analog frequency produced by a VCO and a modulated numeric frequency bitstream. An output signal of the difference engine is filtered using a digital filter, which is followed by a DAC. In an exemplary embodiment, the DAC is a Sigma-Delta DAC that outputs a waveform the period of which is modulated in accordance with the applied voltage. The output signal of the DAC is applied through a resistor to an integrating capacitor C2 (no charge pump current sources are used). The voltage stored on the integrating capacitor is applied to the VCO.

A separate modulation path is used to inject a modulation voltage into the circuit in accordance with the principles previous elucidated. A digital modulation signal is applied to a modulation DAC (also Sigma-Delta). An output signal of the modulation DAC is applied through a resistor to a capacitor C<sub>1</sub>, which forms a capacitive divider network with the integrating capacitor C<sub>2</sub>, after the manner of Figure 7. The series RC combination in the modulation path has a desirable filtering effect on the output signal of the modulation DAC.

Note that modulation is injected at two different points in the circuit, through the main loop and through the separate modulation path. When the modulation is changed, it is changed at these two different points at the same time. To ensure proper operation, it becomes necessary to "dose" part of the modulation signal from the separate modulation path to the main loop. To accomplish this dosing, the modulation input signal of the separate modulation path is scaled by a factor K and input to the summing DAC of the main loop. In an exemplary embodiment,  $K = C_1 / (C_1 + C_2)$ .

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Referring to Figure 23, in an alternative embodiment, the foregoing dosing may be performed in analog fashion using a resistor R2 coupled from the output of the DAC in the modulation path to the top plate of the integrating capacitor. In an exemplary embodiment,  $R_1/R_2 = C_1/C_2$ .

**Claims:**

1. A method of synthesizing an analog signal, comprising:  
using digital logic to produce a first digital bit stream in response to  
a numeric frequency;  
5           sampling an analog frequency signal to produce a second digital bit  
stream; and  
              combining the first and second bits streams to produce a digital  
signal representing at least one of a frequency difference and a phase  
difference between the numeric frequency and the analog frequency.
- 10           2. The method of Claim 1, comprising using said digital signal to  
drive a forward loop of a phase lock loop having a controlled oscillator, wherein  
the controlled oscillator produces said analog frequency signal.
3. The method of Claim 2, comprising coupling an auxiliary  
modulation path to a circuit node within the forward loop.
- 15           4. The method of Claim 3, wherein the auxiliary modulation path  
includes a scaling operation, further comprising performing calibration to  
determine a scale factor and using the scale factor in the scaling operation.
5. The method of Claim 4, wherein the scale factor is determined such  
that a direct modulation gain of the phase lock loop and a gain of the auxiliary  
20           modulation path are substantially equal.
6. The method of Claim 3, wherein the phase lock loop includes an  
analog loop filter, comprising coupling the auxiliary modulation path to a node  
within the analog loop filter.



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7. The method of Claim 3, wherein the phase lock loop includes a digital loop filter, comprising coupling the auxiliary modulation path to a node following the digital loop filter.

5 8. The method of Claim 7, wherein the phase lock loop includes a digital to analog converter coupled to an output signal of the digital loop filter, comprising coupling the auxiliary modulation path to an input of the digital to analog converter.

10 9. The method of Claim 8, wherein the phase lock loop includes a preset signal and a tuning capacitor, further comprising coupling an output signal of the digital to analog converter to one plate of the tuning capacitor.

10. The method of Claim 9, comprising attenuating the output signal of the digital to analog converter prior to coupling the output signal to the tuning capacitor.

15 11. The method of Claim 8, wherein the digital to analog converter is a differential digital to analog converter that produces an output signal substantially proportional to a rate of change of its input signal, further comprising performing analog integration of the output signal.

20 12. A frequency synthesis circuit comprising:  
digital logic for producing a first digital bit stream in response to a numeric frequency;  
means for sampling an analog frequency signal to produce a second digital bit stream; and



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means for combining the first and second bits streams to produce a signal representing at least one of a frequency difference and a phase difference between the numeric frequency and the analog frequency.

13. The apparatus of Claim 12, further comprising a phase lock loop  
5 having a controlled oscillator, wherein the digital signal is used to drive a forward loop of the phase lock loop and the controlled oscillator produces said analog frequency signal.

14. The apparatus of Claim 13, further comprising an auxiliary modulation path coupled to a circuit node within the forward loop.

10 15. The apparatus of Claim 14, wherein the auxiliary modulation path includes a scaler for matching a direct modulation gain of the phase lock loop and a gain of the auxiliary modulation path.

16. The apparatus of Claim 14, wherein the phase lock loop includes an analog loop filter and the auxiliary modulation path is coupled to a node within the  
15 analog loop filter.

17. The apparatus of Claim 14, wherein the phase lock loop includes a digital loop filter and the auxiliary modulation path is coupled to a node following the digital loop filter.

18. The apparatus of Claim 17, wherein the phase lock loop includes a  
20 digital to analog converter coupled to an output signal of the digital loop filter and the auxiliary modulation path is coupled to an input of the digital to analog converter.



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19. The apparatus of Claim 18, wherein the phase lock loop includes a preset signal and a tuning capacitor, and an output signal of the digital to analog converter is coupled to a plate of the tuning capacitor.

5 20. The apparatus of Claim 19, wherein the output of the digital to analog converter is coupled to the tuning capacitor through a resistive divider.

21. The apparatus of Claim 19, wherein the preset circuit includes a tuning capacitor and the output signal of the digital to analog converter is coupled to a plate of the tuning capacitor.

10 22. The apparatus of Claim 18, wherein the digital to analog converter is a differential digital to analog converter, further comprising an analog integrator that performs analog integration of an output signal of the digital to analog converter.

15 23. A phase lock loop, comprising:  
means responsive to an analog waveform having a frequency attribute and an input bitstream representing a desired waveform for producing an output bitstream representing a difference quantity between the analog waveform and the desired waveform;  
a filter and a digital to analog converter cooperating to produce a  
20 filtered analog difference signal;  
a controlled oscillator that produces the analog waveform; and  
a first capacitor coupling the filtered analog difference signal and an input terminal of the controlled oscillator.

24. The apparatus of Claim 23, wherein the filter is a digital filter.



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25. The apparatus of Claim 23, wherein the first capacitor is a shunt capacitor having one plate coupled to a circuit reference potential.

26. The apparatus of Claim 23, further comprising a separate modulation path for injecting a modulation signal into a main loop of the phase lock loop, a modulation signal produced within the separate modulation path being coupled to an input terminal of the controlled oscillator by at least said first capacitor.

27. The apparatus of Claim 26, further comprising a second capacitor that together with said first capacitor forms a capacitive divider, wherein the modulation signal is applied to the input terminal of the controlled oscillator through the capacitive divider.

28. The apparatus of Claim 27, wherein the second capacitor is a series capacitor.

29. The apparatus of Claim 28, further comprising a resistor coupled in series with the second capacitor.

30. The apparatus of Claim 29, wherein the filtered analog difference signal is applied through a resistor to the first capacitor.

31. The apparatus of Claim 26, further comprising a bypass path between the separate modulation path and the main loop of the phase lock loop, the bypass path bypassing the second capacitor.

32. The apparatus of Claim 31, wherein the bypass path comprises a digital scaler.



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33. The apparatus of Claim 31, wherein the bypass path comprises a resistor.