Claims

What is claimed is:

1. Wireless circuitry comprising:

a first mixer communicatively configured to convert a signal between a first frequency and a second frequency based on a first clock signal;

a second mixer configured to be communicatively coupled between the first mixer and an antenna and configured to convert the signal between the second frequency and a third frequency based on a second clock signal at a higher frequency than the first clock signal;

a reference oscillator;

a first phase-locked loop (PLL) having an input coupled to an output of the reference oscillator;

a second PLL having an input coupled to an output of the first PLL and configured to generate the second clock signal;

a third PLL configured to generate the first clock signal; and

a switch having a first terminal coupled to the output of the reference oscillator, a second terminal coupled to the output of the first PLL, and a third terminal coupled to an input of the third PLL.

2. The wireless circuitry of claim 1, wherein the second PLL is switchable between a high side injection mode and a low side injection mode.

3. The wireless circuitry of claim 2, wherein the switch is configured to couple the output of the first PLL to the input of the third PLL concurrent with the second PLL being in the high side injection mode.

4. The wireless circuitry of claim 3, wherein the switch is configured to couple the output of the reference oscillator to the input of the third PLL concurrent with the second PLL being in the low side injection mode.

5. The wireless circuitry of claim 4, further comprising:

one or more processors configured to switch the second PLL between the high side injection mode and the low side injection mode based on a frequency resource assigned to the electronic device.

6. The wireless circuitry of claim 1, wherein the reference oscillator comprises a crystal oscillator or a micro-electro-mechanical systems (MEMS) oscillator.

7. The wireless circuitry of claim 1, wherein the reference oscillator is configured to generate a third clock signal, the first PLL is configured to generate a fourth clock signal based on the third clock signal, and the second PLL is configured to generate the second clock signal based on the fourth clock signal.

8. The wireless circuitry of claim 7, wherein the switch is switchable between a first state in which the first terminal is coupled to the third terminal and the second terminal is decoupled from the third terminal and a second state in which the second terminal is coupled to the third terminal and the first terminal is decoupled from the third terminal.

9. The wireless circuitry of claim 8, wherein the third PLL is configured to generate the first clock signal based on the third clock signal while the switch is in the first state and is configured to generate the first clock signal based on the fourth clock signal while the switch is in the second state.

10. The wireless circuitry of claim 9, further comprising:

one or more processors configured to place the switch in the first state concurrent with the second clock signal being at a lower frequency than the third frequency and configured to place the switch in the second state concurrent with the second clock signal being at a higher frequency than the third frequency.

11. The wireless circuitry of claim 10, wherein the first frequency is a baseband frequency, the second frequency is higher than the baseband frequency, the third frequency is greater than or equal to 10 GHz, the third clock signal is at a fourth frequency less than or equal to 100 MHz, and the fourth clock signal is at a fifth frequency greater than the fourth frequency.

12. The wireless circuitry of claim 1, further comprising:

a frequency divider coupled between the output of the first PLL and the second terminal of the switch.

13. A wireless transceiver configured to convey a signal at a first frequency, the wireless transceiver comprising:

a first mixer configured to convert the signal between the first frequency and a second frequency lower than the first frequency;

a second mixer configured to convert the signal between the second frequency and a third frequency lower than the second frequency;

a first phase-locked loop (PLL) having an output coupled to the first mixer;

a second PLL having an output coupled to the second mixer;

a third PLL having an output coupled to an input of the first PLL; and

a switch coupled between the output of the third PLL and an input of the second PLL, the switch having a state that is based on an injection mode of the first mixer.

14. The wireless transceiver of claim 13, wherein the first mixer is configured to convert the signal in a high side injection (HSI) mode or a low side injection (LSI) mode, the switch is configured to couple the output of the third PLL to the input of the second PLL concurrent with the first mixer converting the first signal in the HSI mode, and the switch is configured to decouple the output of the third PLL from the input of the second PLL concurrent

with the first mixer converting the first signal in the LSI mode.

15. The wireless transceiver of claim 13, further comprising:

a reference oscillator having an output coupled to the switch and an input of the third PLL.

16. The wireless transceiver of claim 15, wherein the switch has a first state in which the switch couples the output of the reference oscillator to the input of the second PLL and a second state in which the switch couples the output of the third PLL to the input of the second PLL.

17. The wireless transceiver of claim 13, further comprising:

a frequency divider coupled between the switch and the output of the third PLL.

18. A method of operating an circuitry to wirelessly convey a signal, the method comprising:

generating, using a reference oscillator, a first clock signal;

upconverting, using a first phase-locked loop (PLL), the first clock signal to produce a second clock signal;

upconverting, using a second PLL, the second clock signal to produce a third clock signal;

mixing, using a first mixer, a first signal with the third clock signal, the third clock signal being higher in frequency than the first signal;

upconverting, using a third PLL, the second clock signal to produce a fourth clock signal lower in frequency than the third clock signal;

coupling, using a switch, an input of the third PLL to an output of the reference oscillator or an output of the first PLL; and

mixing, using a second mixer, the signal with the fourth clock signal.

19. The method of claim 18, further comprising:

upconverting, using the second PLL, the second clock signal to produce a fifth clock signal lower in frequency than the first signal;

mixing, using the first mixer, a second the signal with the fifth clock signal;

upconverting, using the third PLL, the first clock signal to produce a sixth clock signal lower in frequency than the fifth clock signal; and

mixing, using the second mixer, the second signal with the sixth clock signal.

20. The method of claim 19, further comprising:

toggling, using one or more processors, the switch between production of the fourth clock signal and the fifth clock signal by the third PLL, the switch having a first input terminal coupled to an output of the reference oscillator, a second input terminal coupled to an output of the first PLL, and an output terminal coupled to an input of the third PLL.