

LOW-POWER WIRELESS DIVERSITY RECEIVER WITH MULTIPLE RECEIVE PATHS

BACKGROUND

[0001] The present Application for Patent claims priority to Provisional Application No. 60/531,241, entitled “Low-Power Wireless Diversity Receiver with Multiple Receive Paths” filed December 18, 2003, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

I. Field

[0002] The present invention relates generally to electronics, and more specifically to a diversity receiver for wireless communication.

II. Background

[0003] In a wireless communication system, a transmitter modulates data onto a radio frequency (RF) carrier signal to generate an RF modulated signal that is more suitable for transmission. The transmitter then transmits the RF modulated signal via a wireless channel to a receiver. The transmitted signal may reach the receiver via one or more propagation paths (e.g., a line-of-sight path and/or reflected paths). The characteristics of the propagation paths may vary over time due to various phenomena such as fading and multipath. Consequently, the transmitted signal may experience different channel conditions and may be received with different amplitudes and/or phases over time.

[0004] To provide diversity against deleterious path effects, multiple antennas may be used to receive the RF modulated signal. At least one propagation path typically exists between the transmit antenna and each of the receive antennas. If the propagation paths for different receive antennas are independent, which is generally true to at least an extent, then diversity increases and the received signal quality improves when multiple antennas are used to receive the RF modulated signal.

[0005] A multi-antenna receiver conventionally has one RF receiver processing path (or simply, “receive path”) for each receive antenna. Each receive path includes various circuit blocks (e.g., amplifiers, filters, mixers, and so on) used to condition and process a received

signal from an associated antenna. The circuit blocks are designed to meet various system requirements such as linearity, dynamic range, sensitivity, out-of-band rejection, and so on, as is known in the art. In conventional diversity receiver designs, the receive path is typically replicated for each receive antenna. The replication of the receive paths with identical circuitry results in higher power consumption, larger area, and higher cost for the multi-antenna receiver, all of which are undesirable. For a portable wireless device, the higher power consumption adversely impacts standby time and reduces talk time between battery recharges.

[0006] There is therefore a need in the art for a low-power diversity receiver.

SUMMARY

[0007] A low-power diversity receiver having good performance is described herein. The diversity receiver includes two or more receive paths, each of which is designated as a primary or secondary receive path. A primary receive path is compliant with applicable system requirements (e.g., IS-98D, cdma2000, GSM and/or W-CDMA requirements). A secondary receive path is designed for low power but is not fully compliant with the system requirements. For example, the secondary receive path may be designed to meet requirements for dynamic range and sensitivity but not for certain out-of-band rejection of large amplitude "jammers", which are undesired signals outside of the RF channel of interest. The relaxed requirements allow the secondary receive path to be implemented with lower power consumption, less area, and lower cost. The second receive path can provide good performance under most operating conditions. For a multi-antenna receiver, the primary and secondary receive paths may be used to simultaneously process two received signals from two antennas. For a single-antenna receiver, either the primary or secondary receive path may be selected, e.g., depending on whether or not jammers are detected, to process a single received signal from one antenna.

[0008] In an exemplary embodiment, a wireless device with two receive paths for one frequency band is described. The first (primary) receive path includes (1) a first amplifier that amplifies a first input signal and provides a first amplified signal and (2) a first downconverter that translates the first amplified signal in frequency (e.g., from RF down to baseband) and provides a first baseband signal. The second (secondary) receive path includes (1) a second amplifier that amplifies a second input signal and provides a second amplified signal and (2) a second downconverter that translates the second amplified signal

in frequency and provides a second baseband signal. The first receive path is compliant with system requirements, and the second receive path is non-compliant with some or all of the system requirements. A jammer detector detects for the presence of large amplitude jammers in the first and/or second input signal. If only one receive path is needed, then the first receive path is selected if jammers are detected and the second receive path is selected for use if jammers are not detected. The wireless device may include additional receive paths for additional frequency bands and/or GPS.

[0009] Various aspects and embodiments of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The features and nature of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

[0011] FIG. 1 shows a wireless communication system;

[0012] FIG. 2 shows a single-antenna terminal with two receive paths;

[0013] FIG. 3 shows a dual-antenna terminal with two receive paths;

[0014] FIG. 4 shows a dual-antenna terminal with five receive paths for two frequency bands and GPS;

[0015] FIG. 5 shows a dual-path receiver with a direct-to-baseband architecture;

[0016] FIG. 6 shows a dual-path receiver with a super-heterodyne architecture;

[0017] FIGS. 7 and 8 show two dual-path receivers that may also be used for the dual-antenna terminal in FIG. 3;

[0018] FIG. 9 shows a lowpass filter;

[0019] FIG. 10 shows a jammer detector; and

[0020] FIG. 11 shows a process for operating two receive paths in a wireless terminal.

DETAILED DESCRIPTION

[0021] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment or design described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0022] FIG. 1 shows a wireless communication system 100 in which a number of wireless terminals communicate with a number of base stations. For simplicity, only two

terminals 110a and 110b and two base stations 120a and 120b are shown in FIG. 1. Each terminal 110 may receive signals from any number of transmitting sources at any given moment via line-of-sight paths and/or reflected paths. A reflected path is created when a transmitted signal reflects off a reflection source (e.g., a building, tree, or some other obstruction) and arrives at the terminal via a different path than the line-of-sight path. A terminal may also be referred to as a remote station, a mobile station, an access terminal, a user equipment (UE), a wireless communication device, a cellular phone, or some other terminology. Terminal 110a is equipped with a single antenna, and terminal 110b is equipped with two antennas. A base station is a fixed station and may also be referred to as an access point, a Node B, or some other terminology. A mobile switching center (MSC) 140 couples to the base stations and provides coordination and control for these base stations.

[0023] A terminal may or may not be capable of receiving signals from satellites 130. Satellites 130 may belong to a satellite positioning system such as the well-known Global Positioning System (GPS). Each GPS satellite transmits a GPS signal encoded with information that allows GPS receivers on earth to measure the time of arrival of the GPS signal. Measurements for a sufficient number of GPS satellites can be used to accurately estimate a three-dimensional position of a GPS receiver. A terminal may also be capable of receiving signals from other types of transmitting sources such as a Bluetooth transmitter, a wireless local area network (WLAN) transmitter, an IEEE 802.11 (Wi-Fi) transmitter, and so on.

[0024] In FIG. 1, each terminal 110 is shown as receiving signals from multiple transmitting sources simultaneously, where a transmitting source may be a base station or a satellite. In general, a terminal may receive signals from zero, one, or multiple transmitting sources at any given moment. For multi-antenna terminal 110b, the signal from each transmitting source is received by each of the multiple antennas at the terminal, albeit at different amplitudes and/or phases.

[0025] System 100 may be a Code Division Multiple Access (CDMA) system, a Time Division Multiple Access (TDMA) system, or some other wireless communication system. A CDMA system may implement one or more CDMA standards such as IS-95, IS-2000 (also commonly known as "1x"), IS-856 (also commonly known as "1xEV-DO"), Wideband-CDMA (W-CDMA), and so on. A TDMA system may implement one or more TDMA standards such as Global System for Mobile Communications (GSM). The W-CDMA

standard is defined by a consortium known as 3GPP, and the IS-2000 and IS-856 standards are defined by a consortium known as 3GPP2. These standards are known in the art.

[0026] Low-power diversity receivers that can provide good performance are described herein. A diversity receiver is a receiver with at least two receive paths, with each receive path being capable of conditioning (e.g., amplifying and/or filtering) an RF signal and frequency downconverting the signal to baseband. The low-power diversity receivers may be used for terminals with a single antenna as well as terminals with multiple antennas. Some exemplary low-power diversity receivers are described below.

[0027] FIG. 2 shows a block diagram of an embodiment of single-antenna terminal 110a. In this embodiment, terminal 110a includes a single antenna 212 and two receive paths 220a and 220b. Antenna 212 receives RF modulated signals from base stations 120 and provides a received signal (Prx) that includes versions of the RF modulated signals transmitted by these base stations. A low noise amplifier (LNA) 216 performs low noise amplification on the received signal and provides an input signal (Pin) to both receive paths 220a and 220b. Receive path 220a is designated as the primary receive path, and receive path 220b is designated as the secondary receive path.

[0028] Each receive path 220 processes the input signal from LNA 216 and provides a respective output baseband signal. Receive path 220a is designed to meet applicable system requirements (e.g., for sensitivity, dynamic range, linearity, out-of-band rejection, and so on) and may be used for all operating conditions. Receive path 220b is designed for low power and with less stringent requirements and may be used for most operating conditions. Exemplary designs for receive paths 220a and 220b are described below.

[0029] An analog-to-digital converter (ADC) 230a receives and digitizes the first output baseband signal (Pout1) from receive path 220a and provides a first stream of data samples to a data processor 240 for further processing. Similarly, an ADC 230b receives and digitizes the second output baseband signal (Pout2) from receive path 220b and provides a second stream of data samples to data processor 240. Although not shown in FIG. 2 for simplicity, each output baseband signal and each data sample stream may be a complex signal/stream having an inphase (I) component and a quadrature (Q) component.

[0030] For the embodiment shown in FIG. 2, a signal detector 242 detects for the signal level of the desired signal, which is the signal within an RF channel of interest. The desired signal detection may be performed in various manners known in the art. For example, an automatic gain control (AGC) loop is typically used to adjust the gains of variable gain

amplifiers (VGAs) located within the receive paths so that output baseband signals at the proper amplitude are provided to the ADCs. The gain control signals for these VGAs are indicative of, and may be mapped to, the desired signal level. A jammer detector 250 receives a first detector input signal (D1) from receive path 220a and a second detector input signal (D2) from receive path 220b, detects for the presence of large amplitude jammers in the received signal, and provides a jammer status signal indicating whether or not large amplitude jammers are present in the received signal. A control unit 252 receives the jammer status signal from jammer detector 250 and a Mode control signal from data processor 240 and provides the Enb1 and Enb2 signals used to enable receive paths 220a and 220b, respectively. For example, control unit 252 may select (1) receive path 220a if large amplitude jammers are detected in the received signal and (2) receive path 220b otherwise.

[0031] In one configuration, either receive path 220a or 220b is selected for use at any given moment, depending on the operating conditions. In another configuration, both receive paths 220a and 220b may be active at the same time to simultaneously process signals from two different systems. ADC 230b may be omitted, and a switch may be used to provide the output baseband signal from either receive path 220a or 220b to ADC 230a.

[0032] FIG. 3 shows a block diagram of an embodiment of multi-antenna terminal 110b. In this embodiment, terminal 110b includes two antennas 312a and 312b and two receive paths 320a and 320b. The two antennas 312a and 312b may be formed in various manners at terminal 110b (e.g., with printed traces on a circuit board, wire conductors, and so on), as is known in the art. An LNA 316a amplifies a first received signal (Prx) from antenna 312a and provides a first input signal (Pin) to receive path 320a. Similarly, an LNA 316b amplifies a second received signal (Srx) from antenna 312b and provides a second input signal (Sin) to receive path 320b. Receive path 320a is designated as the primary receive path, and receive path 320b is designated as the secondary/diversity receive path. LNAs 316a and 316b may also be considered as part of receive paths 320a and 320b, respectively.

[0033] Each receive path 320 processes the input signal from one LNA 316 and provides a respective output baseband signal. Receive path 320a is designed to meet applicable system requirements and may be used for all operating conditions. Receive path 320b is designed for low power and with less stringent requirements and may be used for most operating conditions. In one configuration, either receive path 320a or 320b is selected for use at any given moment, depending on the operating conditions. In another configuration, both receive paths 320a and 320b are active at the same time to simultaneously process two

received signals for the same wireless system in order to achieve diversity. In yet another configuration, both receive paths 320a and 320b simultaneously process signals for two different systems. Exemplary designs for receive paths 320a and 320b are described below.

[0034] ADC 330a receives and digitizes the first output baseband signal (Pout) from receive path 320a and provides a first data sample stream to a data processor 340. Similarly, an ADC 330b receives and digitizes the second output baseband signal (Sout) from receive path 320b and provides a second data sample stream to data processor 340. A signal detector 342 detects for the desired signal level. A jammer detector 350 detects for the presence of large amplitude jammers in the first and/or second received signal and provides a jammer status signal. A control unit 352 enables one or both receive paths 320a and 320b based on the jammer status signal from jammer detector 350 and the Mode control signal from data processor 340.

[0035] A wireless terminal may be a single-band terminal or a multi-band terminal. A single-band terminal supports operation on one specific frequency band. A multi-band terminal supports operation on multiple frequency bands and typically operates on one of the supported bands at any given moment. A multi-band terminal can communicate with different wireless communication systems operating on different frequency bands. Table 1 lists various frequency bands commonly used for wireless communication as well as the frequency band for GPS.

Table 1

Frequency Band	Frequency Range
Personal Communication System (PCS)	1850 to 1990 MHz
Cellular	824 to 894 MHz
Digital Cellular System (DCS)	1710 to 1880 MHz
GSM900	890 to 960 MHz
International Mobile Telecommunications-2000 (IMT-2000)	1920 to 2170 MHz
CDMA450	411 to 493 MHz
JCDMA	832 to 925 MHz
KPCS	1750 to 1870 MHz
GPS	1574.4 to 1576.4 MHz

The PCS band is also known as GSM1900, the DCS band is also known as GSM1800, and the cellular band is also known as an Advanced Mobile Phone System (AMPS) band. A wireless communication system may also operate on a frequency band that is not listed in Table 1.

[0036] For each of the frequency bands listed in Table 1 except for GPS, one frequency range is used for the forward link (i.e., downlink) from the base stations to the terminals, and another frequency range is used for the reverse link (i.e., uplink) from the terminals to the base stations. As an example, for the cellular band, the 824 to 849 MHz range is used for the reverse link, and the 869 to 894 MHz range is used for the forward link.

[0037] FIG. 4 shows a block diagram of an embodiment of dual-band plus GPS, multi-antenna terminal 110c (not shown in FIG. 1). Terminal 110c supports operation on two frequency bands, which for clarity are the cellular and PCS bands in the following description. In the embodiment shown in FIG. 4, terminal 110c includes two antennas 412a and 412b and five receive paths 420a through 420e. The received signal (Prx) from antenna 412a is provided to a diplexer 414a, which provides a first cellular signal to an LNA 416a and a first PCS signal to an LNA 416b. LNAs 416a and 416b perform low noise amplification on their signals and provide Pin1 and Pin2 input signals to receive paths 420a and 420b, respectively. Similarly, the received signal (Srx) from antenna 412b is provided to a diplexer 414b, which provides a second cellular signal to an LNA 416c and a second PCS signal to an LNA 416d. LNAs 416c and 416d perform low noise amplification on their signals and provide Sin1 and Sin2 input signals to receive paths 420c and 420d, respectively. An LNA 416e performs low noise amplification on a received GPS signal (Grx) and provides a Gin input signal to receive path 420e. LNAs 416a through 416e may also be considered as part of receive paths 420a through 420e, respectively.

[0038] Each receive path 420 conditions and frequency downconverts its input signal and provides a respective baseband signal. Receive paths 420a and 420b are designated as primary receive paths and are designed to meet applicable system requirements. Receive paths 420c and 420d are designated as secondary receive paths and are designed for low power and with less stringent requirements. Receive paths 420c and 420d may be implemented with circuit blocks that consume less power, occupy smaller area, and cost less than those of receive paths 420a and 420b.

[0039] For the embodiment shown in FIG. 4, receive paths 420a and 420b share baseband circuit blocks, and receive paths 420c, 420d, and 420e share baseband circuit

blocks. A lowpass filter 440a filters the baseband signal from either receive path 420a or 420b and provides a first filtered baseband signal and the D1 detector input signal. A lowpass filter 440b filters the baseband signal from receive path 420c, 420d, or 420e and provides a second filtered baseband signal and the D2 detector input signal. Amplifiers 442a and 442b amplify and buffer the first and second filtered baseband signals and provide the first and second output baseband signals, Pout and Sout, respectively.

[0040] A jammer detector 450 receives the first and second detector input signals (D1 and D2) from lowpass filters 440a and 440b, respectively, detects for the presence of large amplitude jammers in the received signal, and provides the jammer status signal. A control unit 452 receives the jammer status signal and the Mode control signal and provides enable signals used to enable receive paths 420a through 420e. For example, control unit 452 may select (1) primary receive path 420a or 420b if large amplitude jammers are present, (2) secondary receive path 420c or 420d if large amplitude jammers are not present, (3) both receive paths 420a and 420c for the cellular band or both receive paths 420b and 420d for the PCS band, for the diversity mode, (4) receive path 420a or 420b for wireless communication and receive path 420e for GPS, and so on.

[0041] Receive paths 420a and 420c are designed for the cellular band, receive paths 420b and 420d are designed for the PCS band, and receive path 420e is designed for GPS frequency. Receive paths 420a and 420b may be implemented with narrowband circuit blocks that are tuned to the cellular and PCS bands, respectively. Receive paths 420c and 420d may be implemented with narrowband and/or wideband circuit blocks to achieve the desired performance. For example, the circuit blocks in receive paths 420c and 420d may be implemented with resistors or low quality inductors, whereas the circuit blocks for receive paths 420a and 420b may be implemented with high quality inductors.

[0042] The primary receive paths (receive path 220a in FIG. 2, receive path 320a in FIG. 3, and receive paths 420a and 420b in FIG. 4) are designed to meet applicable system requirements. For CDMA, IS-98D and cdma2000 specify a two-tone test and a single-tone test. For the two-tone test, two tones (or jammers) are located at +900 KHz and +1700 KHz (or at -900 KHz and -1700 KHz) from the center frequency of a CDMA waveform and are 58 dB higher in amplitude than the CDMA signal level. For the single-tone test, a single tone is located at +900KHz from the center frequency of the CDMA waveform and is 72 dB higher in amplitude than the CDMA signal level. These tests define the linearity and dynamic range requirements for the receive path. In most systems, jammers are present for

only a small fraction of the time and rarely reach the +58 or +72 dB level as specified by IS-98D and cdma2000. Nevertheless, the primary receive paths may be designed to be IS-98D and cdma2000 compliant so that they can provide the specified performance for all operating conditions.

[0043] The secondary receive paths (receive path 220b in FIG. 2, receive path 320b in FIG. 3, and receive paths 420c and 420d in FIG. 4) are designed to be low-power and with less stringent requirements. For example, the secondary receive paths may be designed to meet dynamic range and sensitivity requirements, albeit assuming that large amplitude jammers are not present in the received signal. With the relaxed requirements, the secondary receive paths may be designed to consume only a fraction (e.g., 50% or 25%) of the power consumed by the corresponding primary receive paths. The secondary receive paths can still provide good performance most of the time since large amplitude jammers are present intermittently. The secondary receive paths can provide substantial power savings if they are used in place of the primary receive paths.

[0044] When not operating in the diversity mode, either the primary or secondary receive path is selected for use depending on one or more criteria. These criteria may include (1) presence or absence of large amplitude jammers in the received signal and (2) the desired signal level. Table 2 shows an embodiment for selecting receive path based solely on jammer detection.

Table 2

Jammers	Receive Path
Present in the received signal	Primary receive path
Not present in the received signal	Secondary receive path

Table 3 shows an embodiment for selecting receive path based on jammer detection and desired signal level.

Table 3

Jammers	Desired Signal	Receive Path
Present	Weak	Primary receive path
Present	Strong	Secondary or primary receive path depending on power level of jammer
Not present	Weak	Secondary receive path
Not present	Strong	Secondary receive path

Large amplitude jammers may be deemed to be present in the received signal if their signal level exceeds a particular threshold, as described below. The desired signal may be deemed to be strong if it exceeds a particular signal level. This signal level may be dependent on the actual performance of the secondary path and may be circuit and implementation dependent. The selection of receive path may also be based on other criteria (e.g., received signal quality or signal-to-noise ratio (SNR), pilot received signal strength, power control bits, and so on), and this is within the scope of the invention.

[0045] A receive path may be implemented with a super-heterodyne architecture or a direct-to-baseband architecture. In the super-heterodyne architecture, the received signal is frequency downconverted in multiple stages, e.g., from RF to an intermediate frequency (IF) in one stage, and then from IF to baseband in another stage. In the direct-to-baseband architecture, the received signal is frequency downconverted from RF directly to baseband in one stage. The super-heterodyne and direct-to-baseband architectures may use different circuit blocks and/or have different circuit requirements.

[0046] FIG. 5 shows a block diagram of a dual-path receiver 500, which implements the direct-to-baseband architecture and may be used for both single-antenna terminal 110a and multi-antenna terminal 110b in FIG. 1. Receiver 500 includes two receive paths 520a and 520b that may be used for receive paths 220a and 220b, respectively, in FIG. 2. In this case, both receive paths 520a and 520b are provided with the same input signal, Pin (not shown in FIG. 5). Receive paths 520a and 520b may also be used for receive paths 320a and 320b, respectively, in FIG. 3. In this case, receive paths 520a and 520b are provided with different input signals, Pin and Sin, respectively, as shown in FIG. 5. The RF portion of receive paths

520a and 520b may be used for receive paths 420a and 420c, respectively, and for receive paths 420b and 420d, respectively, in FIG. 4, as described below. Receive path 520a is the primary receive path, and receive path 520b is the secondary/diversity receive path.

[0047] Within receive path 520a, a VGA 524a amplifies the input signal (Pin) with a first variable gain (Gp1). A filter 526a filters the signal from VGA 524a to pass signal components in the band of interest and remove out-of-band noise and undesired signals. For two-way communication, signals are transmitted simultaneously on the forward link and reverse link. The transmitted signal sent by the terminal on the reverse link is typically much larger in amplitude than the received signal for the forward link. Filter 526a may pass the RF components for the receive frequency range (e.g., from 869 to 894 MHz for cellular band) and filter out and suppress the RF components for the transmit frequency range (e.g., from 824 to 849 MHz for the cellular band). Filter 526a may thus have a passband that corresponds to an entire frequency range/band of interest (e.g., cellular). Because of the potentially large difference in the transmit and receive signal levels, filter 526a needs to provide a large amount of out-of-band rejection in order to meet system requirements. Filter 526a may be implemented with a surface acoustic wave (SAW) filter (which has a sharp roll-off and is often used for applications requiring large attenuation of out-of-band signals), a ceramic filter, or some other type of filter.

[0048] A VGA 528a amplifies the signal from filter 526a with a second variable gain (Gp2) and provides a first conditioned signal having the desired signal level. VGAs 524a and 528a provide the required amplification for the Pin signal, which may vary by 90 dB or more. Additional gain may be provided by other circuit blocks in the receive path. A downconverter 530a receives and frequency downconverts the first conditioned signal with a first LO signal and provides a first baseband signal. The frequency of the first LO signal is selected such that the signal component in the RF channel of interest is downconverted to baseband or near-baseband. For CDMA, each frequency band covers many RF channels, and each RF channel has a bandwidth of 1.23 MHz. A wireless terminal typically receives signal on one RF channel at any given moment.

[0049] A lowpass filter 540a filters the first baseband signal to pass the signal components in the RF channel of interest and to remove noise and undesired signals that may be generated by the downconversion process. For the direct-to-baseband architecture, filter 526a may pass the entire frequency band of interest, and lowpass filter 540a would then pass the RF channel of interest. Lowpass filter 540a may be implemented with various filter types

(e.g., Butterworth, elliptical, Chebychev, and so on), with the proper filter order and bandwidth, and with sufficient bias current to meet linearity and dynamic range requirements. Lowpass filter 540a provides a first filtered baseband signal and the D1 signal for the jammer detector. An amplifier 542a amplifies and buffers the first filtered baseband signal and provides the first output baseband signal (Pout).

[0050] An LO generator 546a provides the first LO signal used to downconvert the Pin signal from RF to baseband. LO generator 546a may be implemented with a voltage controlled oscillator (VCO) or some other type of oscillator. The frequency of the LO signal is selected such that the signal component in the RF channel of interest is downconverted to baseband or near-baseband. A phase locked loop (PLL) 548a receives the first LO signal and generates a control signal for LO generator 546a such that the frequency and/or phase of the first LO signal is locked to a reference signal (not shown in FIG. 5).

[0051] Receive path 520b processes the Sin signal and provides the second output baseband signal (Sout), in similar manner as receive path 520a. For each receive path, the frequency downconversion may be performed in various manners. For example, frequency downconversion may be performed by mixing the RF input signal down to baseband, as shown in FIG. 5. The frequency downconversion may also be performed by sampling or digitizing the RF input signal and using the aliasing property of data sampling to generate samples at baseband. Frequency downconverters 530a and 530b may be implemented with mixers, ADCs, mixer (e.g., for downconverter 530a) and ADC (e.g., for downconverter 530b), and so on. RF sampling may be more readily implemented on the secondary receive path 520b since the specifications are simpler.

[0052] FIG. 5 shows a specific design for receive paths 520a and 520b. In general, a receive path may perform signal conditioning using one or more stages of amplifier, filter, mixer, and so on, which may be arranged in a different manner from that shown in FIG. 5. Moreover, a receive path may employ other circuit blocks not shown in FIG. 5 for signal conditioning.

[0053] FIG. 5 shows receive paths 520a and 520b having the same circuit blocks. However, different circuit designs may be used for the circuit blocks in receive paths 520a and 520b because of the different requirements and objectives for the primary and secondary receive paths.

[0054] Receive path 520a is designed to meet applicable system requirements, e.g., linearity, dynamic range, and sensitivity requirements. To achieve this, the RF circuit blocks

in receive path 520a are typically narrowband circuits tuned to a specific frequency band (e.g., cellular or PCS band). For example, VGAs 524a and 528a and downconverter 530a may be implemented with narrowband circuits to achieve the desired linearity over a wide dynamic range. The narrowband circuit blocks may use matching and tuned circuits, inductive degeneration, and other circuit techniques known in the art to achieve the desired performance. Lowpass filter 540a may be designed with a relatively sharp roll-off (e.g., as a 5-th order elliptical filter) in order to attenuate large amplitude jammers in the input signal. These jammers can take up a large portion of the dynamic range of the subsequent ADC if they are not sufficiently filtered. LO generator 546a is designed to have good phase noise performance. In general, good performance for the circuit blocks within receive path 520a typically requires the use of larger-size circuit components (e.g., larger capacitors, inductors and/or transistors) and large amounts of bias current.

[0055] Receive path 520b is designed for low-power and with less stringent requirements, which assumes that large amplitude jammers are not present in the received signal. Because of the less stringent requirements, VGAs 524b and 528b, downconverter 530b, filter 540b, and amplifier 542b may be designed with smaller-size circuit components (e.g., smaller capacitors) and smaller amounts of bias current. VGAs 524b and 528b and downconverter 530b may be implemented without using inductors (which typically occupy a large area) or by using inductors of lower quality (which can occupy a smaller area). Filter 526b may be implemented with on-chip circuit components instead of an external SAW filter (which may be needed for filter 526a). Because large amplitude jammers are assumed to be absent for receive path 520b, the overall gain may be distributed differently for the secondary receive path in a manner to further reduce power consumption, area, and cost. Lowpass filter 540b may be implemented with a lower order (e.g., as a 3-rd order elliptical filter) than lowpass filter 540a. Using these various circuit design techniques, receive path 520b may be designed to consume only a fraction (e.g., 50% or 25%) of the power and occupy only a small fraction of the area required by receive path 520a.

[0056] FIG. 6 shows a block diagram of a dual-path receiver 600, which implements the super-heterodyne architecture and may also be used for both single-antenna terminal 110a and multi-antenna terminal 110b. Receiver 600 includes two receive paths 620a and 620b that may be used for receive paths 220a and 220b, respectively, in FIG. 2, and for receive paths 320a and 320b, respectively, in FIG. 3. The RF portion of receive paths 620a and 620b

may be used for receive paths 420a and 420c, respectively, and for receive paths 420b and 420d, respectively, in FIG. 4.

[0057] Within receive path 620a, the input signal (Pin) is amplified by a VGA 614a, filtered by a filter 616a, and downconverted from RF to IF by a frequency downconverter 622a. The IF signal from downconverter 622a is further amplified by a VGA 624a, filtered by a bandpass filter 626a, amplified and buffered by an amplifier 628a, and downconverted from IF to baseband by a frequency downconverter 630a. The baseband signal from downconverter 630a is filtered by a lowpass filter 640a and amplified and buffered by an amplifier 642a to obtain the first output baseband signal (Pout).

[0058] For the super-heterodyne architecture, bandpass filter 626a may be implemented with a SAW filter and may perform RF channel selection (i.e., may have a passband corresponding to one RF channel, instead of an entire frequency band). If the RF channel selection is performed by bandpass filter 626a, then the requirements for lowpass filter 640a may be relaxed.

[0059] An LO generator 646a provides a first LO signal used for RF to IF downconversion and a second LO signal used for IF to baseband downconversion. Typically, the IF is fixed, the frequency of the first LO signal is selected such that the signal component in the RF channel of interest is downconverted to the fixed IF, and the frequency of the second LO signal is also fixed.

[0060] Receive path 620b processes the Sin signal and provides the second output baseband signal (Sout), in similar manner as receive path 620a. Receive path 620b may be implemented with circuit blocks that consume less power, occupy smaller area, and are lower cost than those of receive path 620a.

[0061] Referring back to FIG. 4, receive paths 420a through 420e may be implemented with the direct-to-baseband architecture or the super-heterodyne architecture. For the direct-to-baseband architecture, each of receive paths 420a through 420e may be implemented with VGAs 524 and 528, filter 526, and frequency downconverter 530 in FIG. 5. For the super-heterodyne architecture, each of receive paths 420a through 420e may be implemented with VGAs 614 and 624, amplifier 628, filters 616 and 626, and frequency downconverters 622 and 630 in FIG. 6.

[0062] Two LO generators operating independently, as shown in FIGS. 5 and 6, may be used for the primary and secondary receive paths. This design allows the primary and secondary receive paths to operate simultaneously and independently to process two signals

on two different RF channels. This capability may be useful for various applications. For example, a terminal with this capability can receive two simultaneous transmissions on two RF channels from one or two systems. As another example, a terminal with this capability can perform mobile-assisted hand-off (MAHO) to select the best base stations to communicate with. The terminal can receive a transmission from a serving base station with the primary receive path and can simultaneously search for signals from other base stations with the secondary receive path. This would then allow the terminal to initiate a hand-off to another base station that is better than the serving base station, if one is found. If independent operation of the primary and secondary receive paths is not needed, then one LO generator may be shared by both receive paths.

[0063] Although not indicated in FIGS. 2 through 6 for simplicity, the primary receive paths (receive path 220a in FIG. 2, receive path 320a in FIG. 3, receive paths 420a and 420b in FIG. 4, receive path 520a in FIG. 5, and receive path 620a in FIG. 6) may be designed with multiple power modes, e.g., a high power mode and a low power mode. In the high power mode, the circuit blocks (e.g., amplifiers, mixers, and so on) within the primary receive paths may be biased with high current to meet applicable system requirements under the worst-case operating condition, such as those specified by IS-98D or cdma2000. In the low power mode, the circuit blocks within the primary receive paths may be biased with less current that can still meet applicable system requirements under more moderate operating condition, e.g., with no jammers or low amplitude jammers. The primary receive paths may also be designed with more than two power modes, with more current being used for more severe operating condition.

[0064] Many wireless systems have an open loop transmit power specification that dictates the amount of transmit power to use at the start of a transmission based on the received power level. A terminal typically does not know the transmit power level needed for reliable communication when the terminal is first powered on or first starts to transmit. In this case, the forward and reverse links may be assumed to be reciprocal of one another, i.e., the path loss for the reverse link is assumed to be equal to the path loss for the forward link. The terminal can estimate the path loss for the forward link based on a pilot received from a base station and can determine the amount of transmit power to use for the reverse link transmission based on the forward link measurement. However, if the terminal is equipped with multiple antennas, then the received power level may change abruptly when

different antennas are selected for use. This open loop power disturbance may result in the wrong transmit power level being used for the reverse link transmission.

[0065] FIG. 7 shows a block diagram of a dual-path receiver 700 that may be used for dual-antenna terminal 110b in FIG. 3. Receiver 700 includes two receive paths 720a and 720b. Receive path 720a is the primary receive path and couples to a duplexer 714a, which further couples to a transmitter unit (TMTR) 710 and an antenna 712a. Duplexer 714a routes the transmit signal from transmitter unit 710 to antenna 712a and further routes the received signal from antenna 712a to receive path 720a. Receive path 720b is the secondary receive path and couples to a SAW filter 714b, which further couples to an antenna 712b. For this embodiment, the terminal only transmits from antenna 712a and not antenna 712b. Antenna 712a may be a whip/dipole antenna or some other type of antenna. Antenna 712b may be an internal antenna, a printed antenna, or some other type of antenna.

[0066] Receive path 720a includes an LNA 716a, a switch 722a, a filter 726a, a VGA 728a, a frequency downconverter 730a, a lowpass filter 740a, and an amplifier 742a, all of which function as described above for FIGS. 2 through 6. Receive path 720b includes the same circuit blocks as receive path 720a. The circuit blocks for receive path 720a may be designed and biased to be spec-compliant, and the circuit blocks for receive path 720b may be designed and biased for low power. The circuit blocks for receive path 720a may also be designed with multiple power modes, as described above.

[0067] In a first operating mode, both receive paths 720a and 720b are selected for use to achieve diversity. For this mode, switches 722a and 722b are both switched to the "A" position and pass the output of LNAs 716a and 716b, respectively, to filters 726a and 726b, respectively. If diversity is not needed, then either receive path 720a or 720b may be selected for use depending on the operating condition. In a second operating mode, receive path 720a is selected for use if large amplitude jammers are detected. For this mode, switch 722a is switched to the "A" position, and the entire receive path 720b may be powered down. In a third operating mode, receive path 720b is selected for use if no jammers or low amplitude jammers are detected. For this mode, switches 722a and 722b are both switched to the "B" position, and the output of LNA 716a is routed to filter 726b. LNA 716b in receive path 720b and all of the circuit blocks after switch 722a in receive path 720a may be powered down. LNA 716a may also be biased with less current to conserve power. For all three operating modes, the received signal power can be measured from antenna 712a. The overall gain from switch 722 to amplifier 742 may be determined for each receive path and used to

account for the received signal power measurements. Switches 722a and 722b can mitigate open loop power disturbance.

[0068] FIG. 8 shows a block diagram of a dual-path receiver 702 that may also be used for dual-antenna terminal 110b in FIG. 3. Receiver 702 includes two receive paths 721a and 721b. Each receive path 721 includes all of the circuit blocks in receive path 720 in FIG. 7. However, switches 722a and 722b are placed after filters 726a and 726b, respectively, in receive paths 721a and 721b, respectively. If filter 726a has better electrical characteristics than filter 726b, then improved performance may be obtained by using filter 726a instead of filter 726b. In general, switch 722a may be located anywhere within receive path 721a, and switch 722b may be located anywhere within receive path 721b.

[0069] FIG. 9 shows an embodiment of a lowpass filter 940, which may be used for each of the lowpass filters shown in FIGS. 4, 5 and 6. Lowpass filter 940 includes a single-pole filter section 942 and bi-quad filter sections 944 and 946. Single-pole filter section 942 implements one real pole. Each of bi-quad filter sections 944 and 946 implements a pair of complex poles. A 5-th order (e.g., elliptical, Butterworth, Bessel, or Chebychev) filter may be implemented with all three filter sections 942, 944, and 946.

[0070] The lowpass filters for the receive paths may also be implemented with other filter designs. Furthermore, the lowpass filters for the primary and secondary receive paths may be implemented with the same or different filter designs. For example, a 5-th order lowpass filter may be used for the primary receive path, and a 3-rd order lowpass filter may be used for the secondary receive path.

[0071] As noted above, when not operating in the diversity mode, either the primary or secondary receive path for the desired frequency band is selected for use depending on whether or not jammers are detected in the received signal. Jammers are large amplitude, undesired out-of-band signals that can distort the desired in-band signal. The detector input signals used for jammer detection may be obtained from various points along the receive path but should include out-of-band signal components. The detector input signals may be broadband signals with a flat frequency response that gives equal weight to signal components at different frequencies. However, jammers that are closer in-band (i.e., closer to the desired RF channel) tend to be more detrimental to the desired signal than jammers that are farther away in frequency. Thus, the detector input signals may be rolled off (e.g., with a first-order lowpass filter response) to allow for discrimination of the frequency offset

of the jammers. This would then give jammers closer in more weight and jammers farther away less weight.

[0072] For the embodiments shown in FIGS. 4, 5 and 6, the lowpass filters also provide the detector input signals (D1 and D2) used to detect for the presence of jammers in the received signals. In an embodiment, the detector input signals are taken after single-pole filter section 942 in the lowpass filters.

[0073] **FIG. 10** shows a block diagram of a jammer detector 1050, which may be used for the jammer detectors in FIGS. 2, 3 and 4. The D1 and D2 signals for the primary and secondary receive paths are rectified by rectifiers 1052a and 1052b, filtered by lowpass filters 1054a and 1054b, and provided to comparators 1056a and 1056b, respectively. Each rectifier 1052 converts its detector input signal from a sinusoidal signal (with positive and negative amplitude) to a single-ended signal (with only positive amplitude) and may be implemented with a diode. Each lowpass filter 1054 may be implemented, for example, with a single-order lowpass filter of an appropriate bandwidth (e.g., several hundred Hertz). Each comparator 1056 compares its filtered signal against a threshold level (V_{th}) and provides an output signal, which is (1) logic high ('1') if the filtered signal amplitude is larger than the threshold level, indicating the presence of large amplitude jammers in the received signal, and (2) logic low ('0') otherwise. Detector logic 1058 combines the output signals of comparators 1056a and 1056b and provides the jammer status signal to control unit 252, 352, or 452.

[0074] In general, jammer detection may be performed based on (1) only the D1 signal, (2) only the D2 signal, or (3) both the D1 and D2 signals. The filtered signals from lowpass filters 1054a and 1054b may be compared against the threshold level as shown in FIG. 10 to obtain a 1-bit output signal. These filtered signals may also be digitized with an ADC to obtain multiple bits of resolution. The jammer status signal may be used to select either the primary or secondary receive path. The jammer status signal may also be used to adjust (e.g., the gains and/or bias currents of) the circuit blocks in the primary and/or secondary receive paths.

[0075] **FIG. 11** shows a flow diagram of a process 1100 for operating two receive paths in a wireless terminal. The presence of large amplitude jammers in a first input signal or a second input signal is detected (block 1112). The first and second input signals may be from (1) one antenna for a single-antenna terminal or (2) two antennas for a multi-antenna terminal. The primary receive path (which is spec-compliant, e.g., IS-98D compliant) is

enabled to process the first input signal if large amplitude jammers are detected (block 1114). The secondary receive path (which is not fully spec-compliant) is enabled to process the second input signal if large amplitude jammers are not detected (block 1116). The primary and secondary receive paths are both enabled if the multi-antenna terminal is operating in a diversity mode and the received signals from both antennas are to be processed simultaneously. Electrical characteristics (e.g., gains, bias currents, and so on) of the circuit blocks in the enabled receive path(s) may also be adjusted based on the detected jammer signal level and/or the desired signal level (block 1118).

[0076] The low-power diversity receiver described herein can provide good performance for both single-antenna and multi-antenna terminals under most operating conditions. The worst-case operating condition occurs when (1) the desired signal is near “sensitivity”, which is the lowest detectable received signal level, and (2) the jammers are at maximum signal level and located at a small frequency offset away from the desired signal. This worst-case condition is a low probability event. For the single-antenna terminal, the low-power secondary receive path may be used for most operating conditions. For the multi-antenna terminal, the diversity mode is typically needed for only 20 to 50 percent of the time. For the remaining 50 to 80 percent of the time, a single receive path may be used, and the secondary receive path may be selected if large amplitude jammers are not detected. For both single-antenna and multi-antenna terminals that are portable, the secondary receive path consumes less power and improves both standby time between battery recharges and talk time.

[0077] The low-power diversity receiver described herein may be used for a wireless terminal to receive forward link transmissions from base stations. The low-power diversity receiver may also be used for a base station to receive reverse link transmissions from user terminals.

[0078] The low-power diversity receiver described herein may be used for various wireless communication systems such as a CDMA system, a TDMA system, a GSM system, an AMPS system, a multiple-input multiple-output (MIMO) system, an orthogonal frequency division multiplexing (OFDM) system, an orthogonal frequency division multiple access (OFDMA) system, a wireless local area network, and so on.

[0079] A large portion of a diversity receiver (possibly all circuit blocks except SAW filters, control units 252, 352, and 452, and data processors 240 and 340) may be implemented on one or more RF integrated circuits (RFICs). The diversity receiver may also be fabricated with various IC process technologies such as complementary metal oxide

semiconductor (CMOS), bipolar junction transistor (BJT), bipolar-CMOS (BiCMOS), silicon germanium (SiGe), gallium arsenide (GaAs), and so on.

[0080] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

[0081] WHAT IS CLAIMED IS:

CLAIMS

1. A wireless device comprising:
a first receive path operable to receive, amplify, and frequency downconvert a first input signal to provide a first baseband signal, the first receive path being compliant with system requirements for a receiver; and
a second receive path operable to receive, amplify, and frequency downconvert a second input signal to provide a second baseband signal, the first and second input signals being for same frequency band, and the second receive path being non-compliant with the system requirements for the receiver.
2. The device of claim 1, wherein the first and second input signals are from one antenna.
3. The device of claim 1, wherein the first and second input signals are from first and second antennas, respectively.
4. The device of claim 3, wherein the first and second receive paths concurrently process the first and second input signals, respectively, for diversity mode.
5. The device of claim 1, wherein the first and second receive paths each comprises at least one amplifier, at least one filter, and at least one mixer.
6. The device of claim 5, wherein the first and second receive paths each further comprises at least one switch for routing an intermediate signal from the first receive path to the second receive path.
7. The device of claim 5, wherein the first and second receive paths are coupled to first and second antennas, respectively, and wherein the device is operable to measure signal power of a received signal from the first antenna regardless of whether the first or second receive path is selected for use.

8. The device of claim 1, further comprising:

a third receive path operable to receive, amplify, and frequency downconvert a third input signal to provide a third baseband signal, the third receive path being compliant with the system requirements for the receiver; and

a fourth receive path operable to receive, amplify, and frequency downconvert a fourth input signal to provide a fourth baseband signal, the fourth receive path being non-compliant with the system requirements for the receiver, and wherein the first and second input signals are for a first frequency band and the third and fourth input signals are for a second frequency band.

9. The device of claim 8, wherein the first frequency band is a Cellular band and the second frequency band is a Personal Communication System (PCS) band.

10. The device of claim 1, further comprising:

a third receive path operable to receive, amplify, and frequency downconvert a Global Positioning System (GPS) signal to provide a downconverted GPS signal.

11. The device of claim 1, further comprising:

a detector operative to detect for presence of large amplitude undesired signals in the first or second input signal; and

a control unit operative to select the first receive path for use if the large amplitude undesired signals are detected and to select the second receive path for use if the large amplitude undesired signals are not detected.

12. The device of claim 11, wherein the detector is operative to detect for the presence of the large amplitude undesired signals based on a detector input signal.

13. The device of claim 12, wherein signal components in the detector input signal with larger frequency offsets from a desired signal are attenuated relative to signal components with smaller frequency offsets from the desired signal.

14. The device of claim 13, wherein the signal components in the detector input signal are attenuated by a first-order lowpass filter response.

15. The device of claim 1, further comprising:
a first detector operative to detect for presence of large amplitude undesired signals in the first or second input signal;
a second detector operative to detect for signal level of a desired signal in the first or second input signal; and
a control unit operative to select the first or second receive path for use based on outputs of the first and second detectors.
16. The device of claim 1, wherein the first and second receive paths are operable to downconvert the first and second input signals directly from radio frequency (RF) to baseband.
17. The device of claim 1, wherein the first receive path is operable in one of multiple power modes, each power mode corresponding to different amounts of bias current for circuit blocks within the first receive path.
18. The device of claim 17, wherein the first receive path is operable in a low power mode if jammers are not detected or have low amplitude.
19. The device of claim 1, wherein power consumption of the second receive path is less than fifty percent of power consumption of the first receive path.
20. The device of claim 1, wherein power consumption of the second receive path is less than power consumption of the first receive path.
21. The device of claim 1, wherein the system requirements are specified by a single-tone test and a two-tone test in IS-98D.
22. The device of claim 1, wherein the system requirements are specified by cdma2000, Wideband-CDMA (W-CDMA), or Global System for Mobile Communications (GSM).

23. An integrated circuit comprising:

a first receive path that is compliant with system requirements for a receiver and comprising

a first amplifier operable to receive and amplify a first input signal and provide a first amplified signal, and

a first downconverter operable to frequency downconvert the first amplified signal and provide a first baseband signal; and

a second receive path that is non-compliant with the system requirements for the receiver and comprising

a second amplifier operable to receive and amplify a second input signal and provide a second amplified signal, the first and second input signals being for same frequency band, and

a second downconverter operable to frequency downconvert the second amplified signal and provide a second baseband signal.

24. The integrated circuit of claim 23, further comprising:

a third receive path comprising

a third amplifier operable to receive and amplify a third input signal and provide a third amplified signal, and

a third downconverter operable to frequency downconvert the third amplified signal and provide a third baseband signal; and

a fourth receive path comprising

a fourth amplifier operable to receive and amplify a fourth input signal and provide a fourth amplified signal, and

a fourth downconverter operable to frequency downconvert the fourth amplified signal and provide a fourth baseband signal, and

wherein the first and second input signals are for a first frequency band and the third and fourth input signals are for a second frequency band.

25. The integrated circuit of claim 24, wherein the first frequency band is a Cellular band and the second frequency band is a Personal Communication System (PCS) band.

26. The integrated circuit of claim 23, further comprising:
a third receive path comprising
a third amplifier operable to receive and amplify a Global Positioning System (GPS) signal and provide an amplified GPS signal, and
a third downconverter operable to frequency downconvert the amplified GPS signal and provide a downconverted GPS signal.
27. The integrated circuit of claim 23, wherein the first and second signals are from one antenna.
28. The integrated circuit of claim 23, wherein the first and second signals are from first and second antennas, respectively.
29. The integrated circuit of claim 23, further comprising:
a detector operative to detect for presence of large amplitude undesired signals in the first or second input signal, and wherein the first receive path is selected for use if the large amplitude undesired signals are detected and the second receive path is selected for use if the large amplitude undesired signals are not detected.
30. The integrated circuit of claim 23, further comprising:
a first lowpass filter operable to filter the first baseband signal and provide a first filtered signal; and
a second lowpass filter operable to filter the second baseband signal and provide a second filtered signal.
31. The integrated circuit of claim 30, wherein the second lowpass filter has a lower filter order and lower power consumption than the first lowpass filter.
32. The integrated circuit of claim 23, wherein the second amplifier and the second downconverter for the second receive path are biased with less current than the first amplifier and the first downconverter, respectively, for the first receive path.

33. The integrated circuit of claim 23, wherein the second amplifier and the second downconverter for the second receive path are implemented with smaller-size circuit components than the first amplifier and the first downconverter, respectively, for the first receive path.

34. An apparatus comprising:

means for amplifying a first input signal to provide a first amplified signal;

means for frequency downconverting the first amplified signal to provide a first baseband signal, the means for amplifying the first input signal and the means for frequency downconverting the first amplified signal being compliant with system requirements for a receiver;

means for amplifying a second input signal to provide a second amplified signal; and

means for frequency downconverting the second amplified signal to provide a second baseband signal, the first and second input signals being for same frequency band, and the means for amplifying the second input signal and the means for frequency downconverting the second amplified signal being non-compliant with the system requirements for the receiver.

35. The apparatus of claim 34, further comprising:

means for detecting for presence of large amplitude undesired signals in the first or second input signal;

means for selecting the means for amplifying the first input signal and the means for frequency downconverting the first amplified signal if the large amplitude undesired signals are detected; and

means for selecting the means for amplifying the second input signal and the means for frequency downconverting the second amplified signal if the large amplitude undesired signals are not detected.

36. A method of operating multiple receive paths in a wireless device, comprising:

detecting for presence of large amplitude undesired signals in a first input signal or a second input signal, the first and second input signals being for same frequency band;

enabling a first receive path to process the first input signal if the large amplitude undesired signals are detected, the first receive path being compliant with system requirements for the wireless device; and

enabling a second receive path to process the second input signal if the large amplitude undesired signals are not detected, the second receive path being non-compliant with the system requirements for the wireless device.

37. The method of claim 36, further comprising:

detecting for signal level of a desired signal in the first or second input signal, and wherein the first or second receive path is further enabled based on the signal level of the desired signal.