CLAIMS

1. A codeword synchronization method comprising:

receiving a data sequence, wherein the data sequence comprises a plurality of bits;

determining a candidate bit from among the plurality of bits based on a characteristic value of at least one group of first test data blocks, wherein each group of the at least one group of the first test data blocks comprises multiple first test data blocks, and wherein an interval between a start position of each first test data block in a first group of the at least one group of the first test data blocks and the candidate bit is an integer multiple of a length of a codeword; and

determining a synchronization position based on the candidate bit, wherein the synchronization position indicates a start position of a codeword in the data sequence.

2. The codeword synchronization method of claim 1, wherein determining the synchronization position further comprises:

performing verification based on the candidate bit; and determining that a position of the candidate bit is the synchronization position when the verification is successful.

3. The codeword synchronization method of claim 1, wherein determining the synchronization position further comprises:

obtaining multiple second test data blocks from the data sequence based on the candidate bit, wherein the position of the candidate bit is a start position of the multiple second test data or is a position where several data blocks are between the start position of the multiple second test data blocks and the candidate bit;

performing verification on a characteristic value of the multiple second test data blocks; and

determining that the position of the candidate bit is the synchronization position when the verification of the characteristic value of the multiple second test data blocks is successful.

4. The codeword synchronization method of claim 1, wherein determining the synchronization position further comprises using a position of the candidate bit as the

synchronization position.

5. The codeword synchronization method of claim 3, wherein determining the candidate bit from among the plurality of bits in the data sequence further comprises determining a first candidate bit in a first subsequence of the data sequence, wherein the multiple second test data blocks is obtained from a second subsequence of the data sequence, wherein the first subsequence and the second subsequence are different subsequences.

6. The codeword synchronization method of claim 1, wherein after determining the synchronization position based on the candidate bit, the codeword synchronization method further comprises determining an updated synchronization position of the data sequence when the data sequence is in an out-of-lock state.

7. The codeword synchronization method of claim 6, wherein determining the updated synchronization position of the data sequence further comprises:

determining another candidate bit among the plurality of bits in the data sequence;

determining another synchronization position based on the another candidate bit to obtain a start position of another codeword in the data sequence; and

using the another synchronization position as the updated synchronization position.

8. The codeword synchronization method of claim 6, wherein after determining the synchronization position based on the candidate bit and before determining the updated synchronization position of the data sequence, the codeword synchronization method further comprises:

obtaining a plurality of synchronization codewords from the data sequence based on the synchronization position, wherein the synchronization position is a start position of the plurality of synchronization codewords;

performing verification on characteristic values of the plurality of synchronization codewords; and

determining that the data sequence is in the out-of-lock state when the verification is a failure.

9. The codeword synchronization method of claim 1, wherein the data sequence is a linear block code.

10. A communication device comprising:

at least one memory; and

at least one processor coupled to the at least one memory and configured to:

receive a data sequence, wherein the data sequence comprises a plurality of bits;

determine a candidate bit from among the plurality of bits based on a characteristic value of at least one group of first test data blocks, wherein each group of the at least one group of the first test data blocks comprises multiple first test data blocks, and wherein an interval between a start position of each first test data block in a first group of the at least one group of the first test data blocks and the candidate bit is an integer multiple of a length of a codeword; and

determine a synchronization position based on the candidate bit, wherein the synchronization position indicates a start position of a codeword in the data sequence.

11. The communication device of claim 10, wherein the at least one processor is further configured to:

perform verification based on the candidate bit; and

determine that a position of the candidate bit is the synchronization position when the verification is successful.

12. The communication device of claim 11, wherein the at least one processor is further configured to:

obtain, multiple second test data blocks from the data sequence based on the candidate bit, wherein the position of the candidate bit is a start position of the multiple second test data blocks or is a position where several data blocks are between the start position of the multiple second test data blocks and the candidate bit;

perform verification on a characteristic value of the multiple second test data blocks; and

determine that the position of the candidate bit is the synchronization position when the verification on the characteristic value of the multiple second test data blocks is successful.

13. The communication device of claim 10, wherein the at least one processor is further configured to use a position of the candidate bit as the synchronization position.

14. The communication device of claim 12, wherein the at least one processor is further configured to:

determine the candidate bit from among the plurality of bits in a first subsequence of the data sequence; and

obtain, the multiple second test data blocks from a second subsequence of the data sequence based on the candidate bit, wherein the first subsequence and the second subsequence are comprised in the data sequence, and wherein the second subsequence is either the same as the first subsequence, partially the same as the first subsequence, or different from the first subsequence.

15. The communication device of claim 10, wherein the at least one processor is further configured to: determine an updated synchronization position of the data sequence when the data sequence is in an out-of-lock state.

16. The communication device of claim 15, wherein the at least one processor is further configured to:

determining another candidate bit among the plurality of bits in the data sequence;

determining another synchronization position based on the another candidate bit to obtain a start position of another codeword in the data sequence; and

using the another synchronization position as the updated synchronization position.

17. A chip, comprising:

at least one processor,

wherein the at least one processor is configured to:

receive a data sequence, wherein the data sequence comprises a plurality of bits;

determine a candidate bit from among the plurality of bits based on a characteristic value of at least one group of first test data blocks, wherein each group of the at least one group of the first test data blocks comprises multiple first test data blocks, and wherein an interval between a start position of each first test data block in a first group of the at least one group of the first test data

blocks and the candidate bit is an integer multiple of a length of a codeword; and

determine a synchronization position based on the candidate bit, wherein the synchronization position indicates a start position of a codeword in the data sequence.

18. The chip of claim 17, wherein the at least one processor is further configured to:

perform verification based on the candidate bit; and

determine that a position of the candidate bit is the synchronization position when the verification is successful.

19. The chip of claim 18, wherein the at least one processor is further configured to:

obtain, multiple second test data blocks from the data sequence based on the candidate bit, wherein the position of the candidate bit is a start position of the multiple second test data blocks or is a position where several data blocks are between the start position of the multiple second test data blocks and the candidate bit;

perform verification on a characteristic value of the multiple second test data blocks; and

determine that the position of the candidate bit is the synchronization position when the verification on the characteristic value of the multiple second test data blocks is successful.

20. The chip of claim 17, wherein the at least one processor is further configured to use a position of the candidate bit as the synchronization position.

21. The chip of claim 18, wherein the at least one processor is further configured to:

determine the candidate bit in a first subsequence of the data sequence; and

obtain, the multiple second test data blocks from a second subsequence of the data sequence based on the candidate bit, wherein the first subsequence and the second subsequence are comprised in the data sequence, and wherein the second subsequence is either the same as the first subsequence, partially the same as the first subsequence, or different from the first subsequence.

22. The chip of claim 17, wherein the at least one processor is further configured to determine an updated synchronization position of the data sequence when the data sequence is in an out-of-lock state.

23. The chip of claim 22, wherein the at least one processor is further configured to:

determining another candidate bit among the plurality of bits in the data sequence;

determining another synchronization position based on the another candidate bit to obtain a start position of another codeword in the data sequence; and

using the another synchronization position as the updated synchronization position.

24. The codeword synchronization method of claim 3, wherein performing the verification on the characteristic value of the multiple second test data blocks comprises sequentially accumulating a characteristic value of each of the multiple second test data blocks to obtain a cumulative value, wherein the verification is successful when the cumulative value meets a synchronization condition.

25. The codeword synchronization method of claim 1, wherein the characteristic value is a quantity of all-zero syndromes.

26. The communication device of claim 12, wherein the at least one processor is further configured to sequentially accumulate a characteristic value of each of the multiple second test data blocks to obtain a cumulative value, wherein the verification is successful when the cumulative value meets a synchronization condition.

27. The communication device of claim 10, wherein the characteristic value is a quantity of all-zero syndromes.

28. The chip of claim 19, wherein the at least one processor is further configured to sequentially accumulate a characteristic value of each of the multiple second test data blocks to obtain a cumulative value, wherein the verification is successful when the cumulative value meets a synchronization condition.

29. The chip of claim 17, wherein the characteristic value is a quantity of all-zero syndromes.

30. The communication device of claim 10, wherein a length of the first test data block is a length of the codeword.