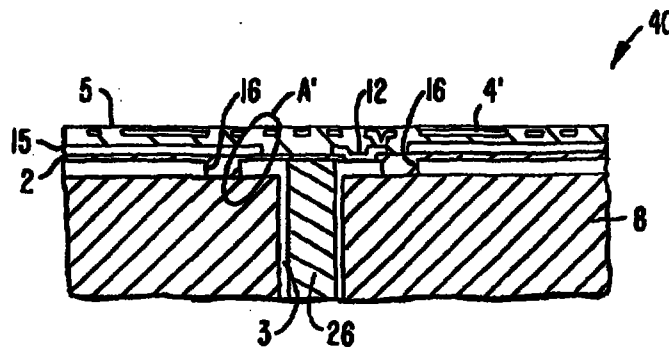




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| <b>(21) International Application Number:</b> PCT/US99/17430<br><b>(22) International Filing Date:</b> 30 July 1999 (30.07.99)<br><b>(30) Priority Data:</b><br>09/127,579      31 July 1998 (31.07.98)      US<br><b>(71) Applicant:</b> KULICKE & SOFFA HOLDINGS, INC. [US/US];<br>2101 Blair Mill Road, Willow Grove, PA 19090 (US).<br><b>(72) Inventors:</b> WESTBROOK, Scott, M.; 1161 Seena Avenue,<br>Los Altos, CA 94024 (US). STRANDBERG, Jan, I.; 1405<br>Cedarmeadow Court, San Jose, CA 95131 (US).<br><b>(74) Agents:</b> BROOKS, Kenneth, C. et al.; Townsend and<br>Townsend and Crew LLP, 8th floor, Two Embarcadero<br>Center, San Francisco, CA 94111-3834 (US). | <b>(81) Designated States:</b> AE, AL, AM, AT, AU, AZ, BA, BB, BG,<br>BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB,<br>GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG,<br>KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK,<br>MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI,<br>SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZA, ZW,<br>ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG,<br>ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ,<br>TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI,<br>FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent<br>(BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE,<br>SN, TD, TG).<br><br><b>Published</b><br><i>With international search report.</i> |                                                                                                                                             |

**(54) Title:** A METHOD FOR CONTROLLING STRESS IN THIN FILM LAYERS DEPOSITED OVER A HIGH DENSITY INTERCONNECT COMMON CIRCUIT BASE

**(57) Abstract**

A method for forming a high density interconnect printed wiring board substrate (40) that has a first patterned conductive layer formed over an upper surface of the substrate that includes multiple conductive lines (6) having edges (16) that define the boundaries of the conductive lines (6) and a dielectric layer (2) formed over the patterned conductive layer and between the edges (16) of the conductive lines (6). The method includes forming a thin film conductive layer (4) over the dielectric layer (2), and patterning the thin film conductive layer (4) such that, after the patterning step, the thin film conductive layer (4) overlies each of the edges (16) of the conductive lines (6). In a preferred embodiment, the thin film conductive layer (4) is patterned such that, after the patterning step, the layer overlies the edges (16) of the conductive lines (6) by at least 10 microns. In another aspect of the invention, a method for strengthening thin film build-up layers deposited over a high density interconnect common circuit base (80) is taught. According to this aspect, a photo-definable thin film dielectric layer (5) having a coefficient of expansion of less than about 10 % is formed over a patterned conductive layer (6) and a thin film conductive layer (4) is formed over the photo-definable thin film dielectric layer (5). The thin film conductive layer is then patterned to include a plurality of signal lines (18) and a plurality of thieving lines (10) with the thieving lines (10) being placed between nonuniformly spaced signal lines (18) to provide a substantially uniform combined pattern of signal lines (18) and thieving lines (10).