FIG. 1

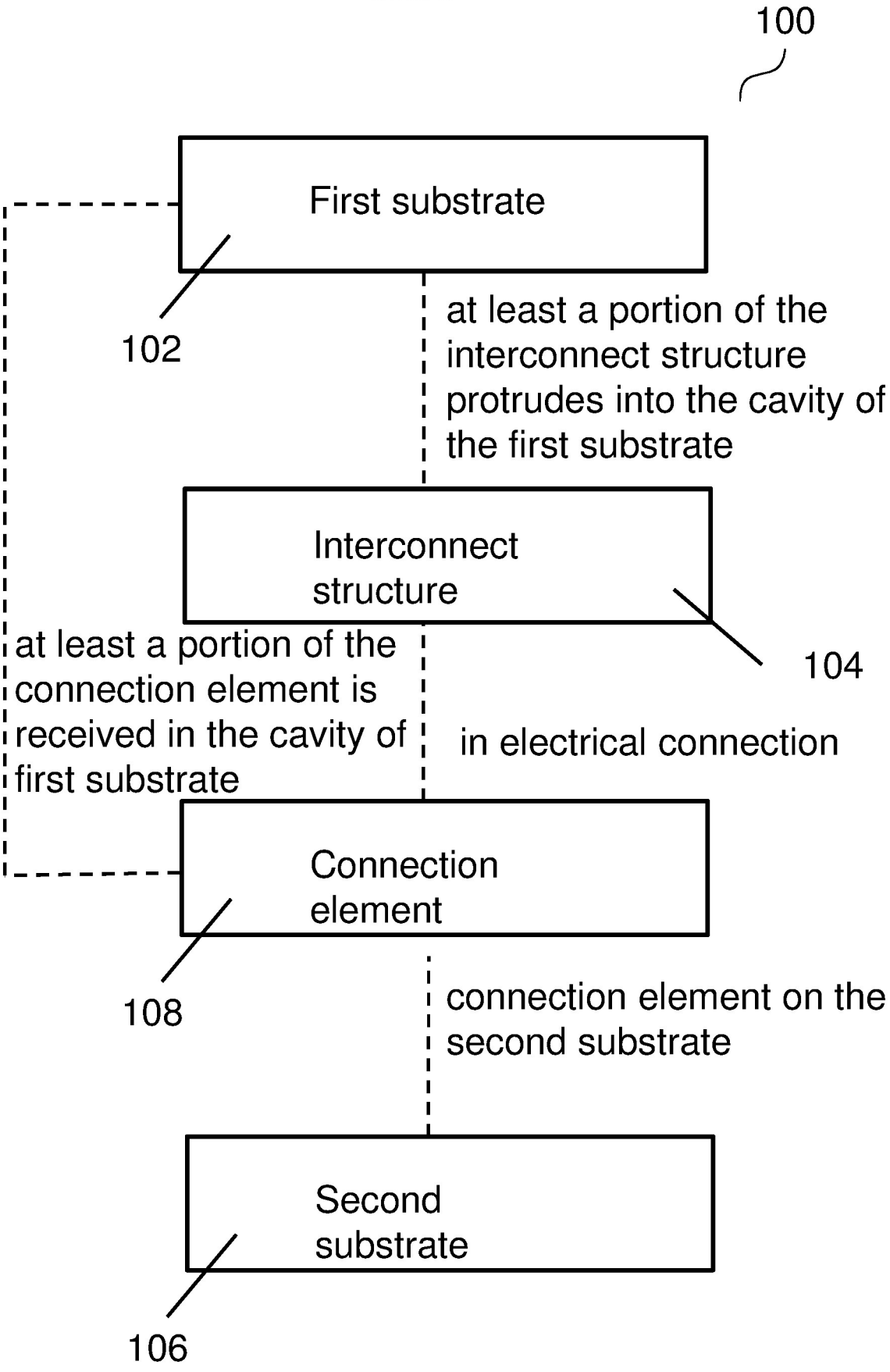

100
First substrate
102
at least a portion of the interconnect structure protrudes into the cavity of the first substrate
Interconnect structure
104
at least a portion of the connection element is received in the cavity of first substrate
in electrical connection
Connection element
108
connection element on the second substrate
Second substrate
106

FIG. 2

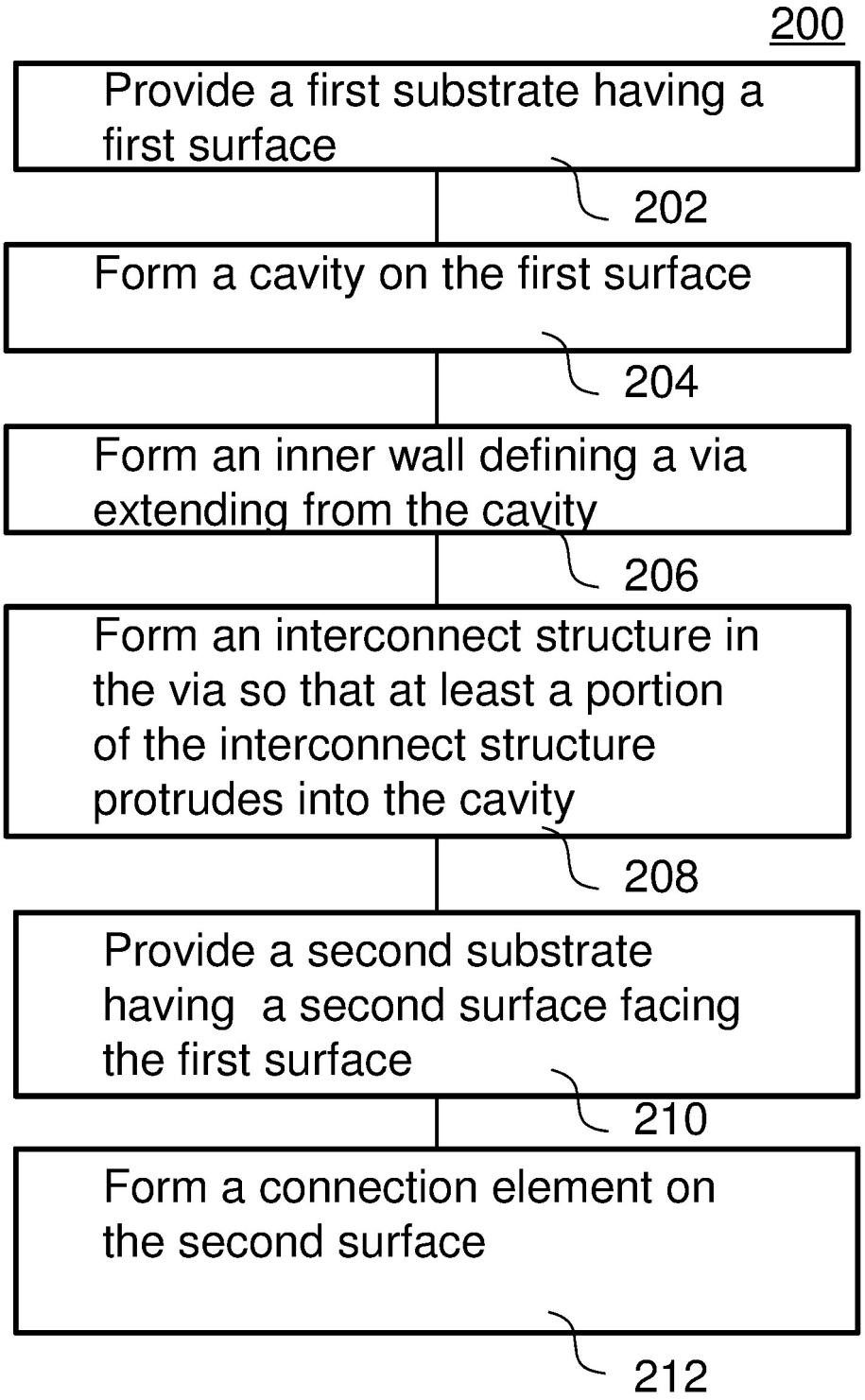

200
Provide a first substrate having a first surface
202
Form a cavity on the first surface
204
Form an inner wall defining a via extending from the cavity
206
Form an interconnect structure in the via so that at least a portion of the interconnect structure protrudes into the cavity
208
Provide a second substrate having a second surface facing the first surface
210
Form a connection element on the second surface
212

FIG. 3A

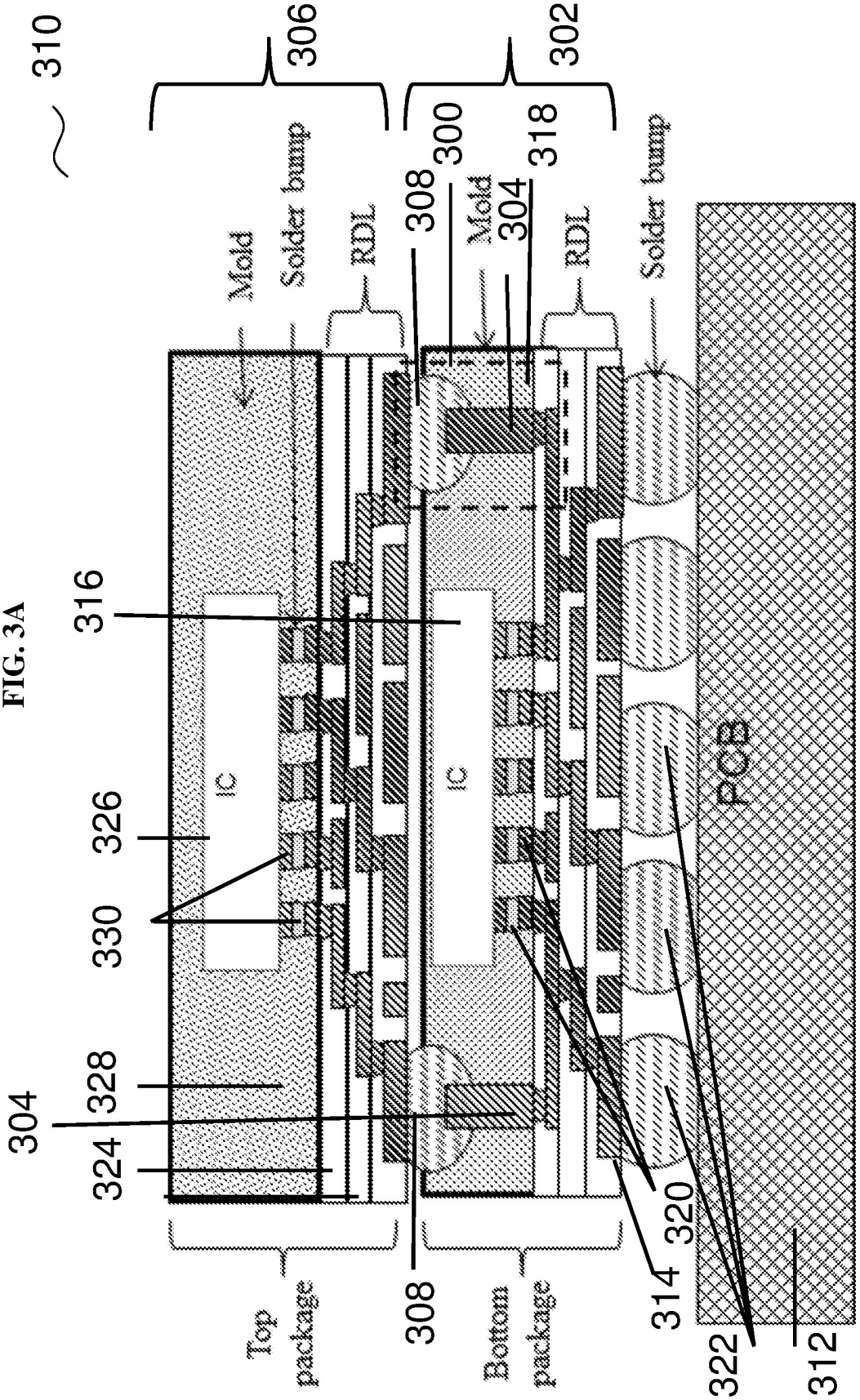

310
306
302
Mold
Solder bump
RDL
308
300
Mold
304
318
RDL
Solder bump
316
326
330
328
304
324
IC
IC
PCB
Top package
308
Bottom package
314
320
322
312

FIG. 3B

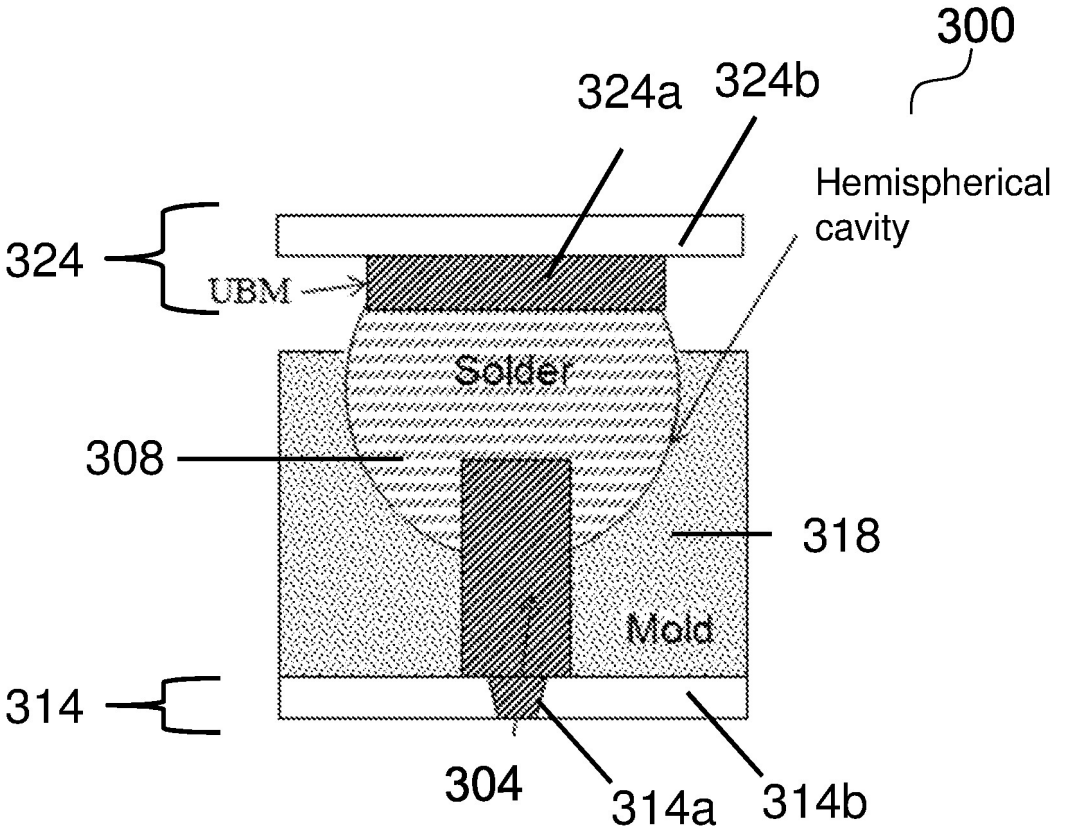

300
324a
324b
Hemispherical cavity
324
UBM
Solder
308
318
Mold
314
304
314a
314b

FIG. 3C

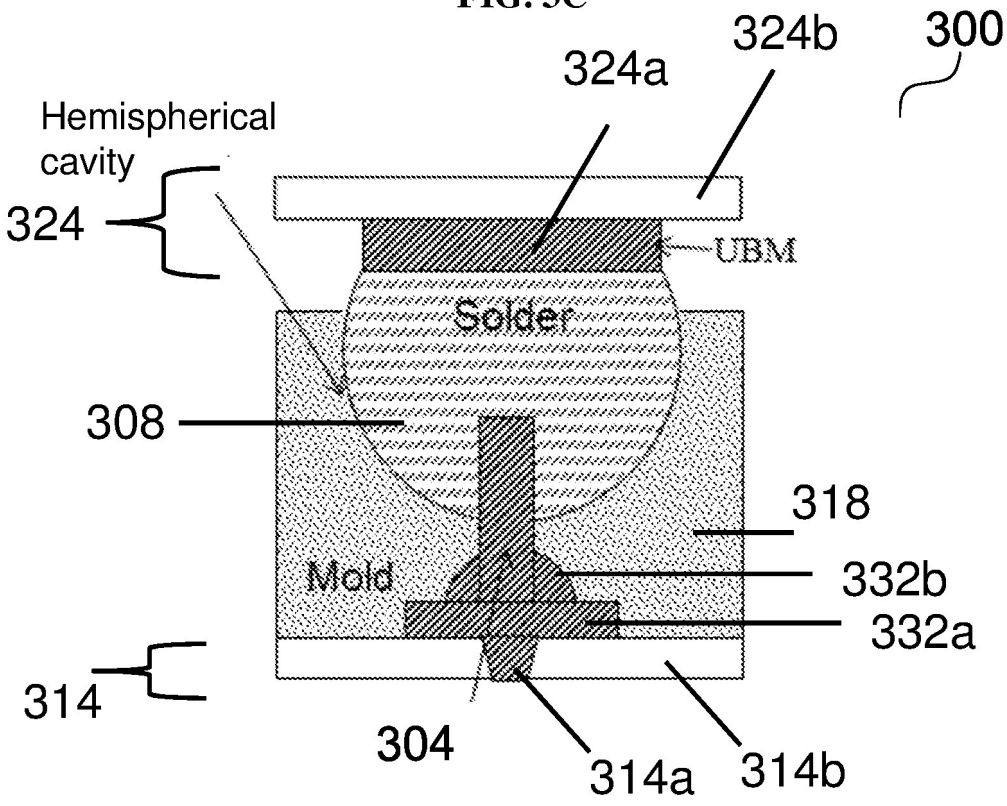

300
324b
324a
Hemispherical cavity
324
UBM
Solder
308
318
332b
332a
Mold
314
304
314a
314b

FIG. 3D

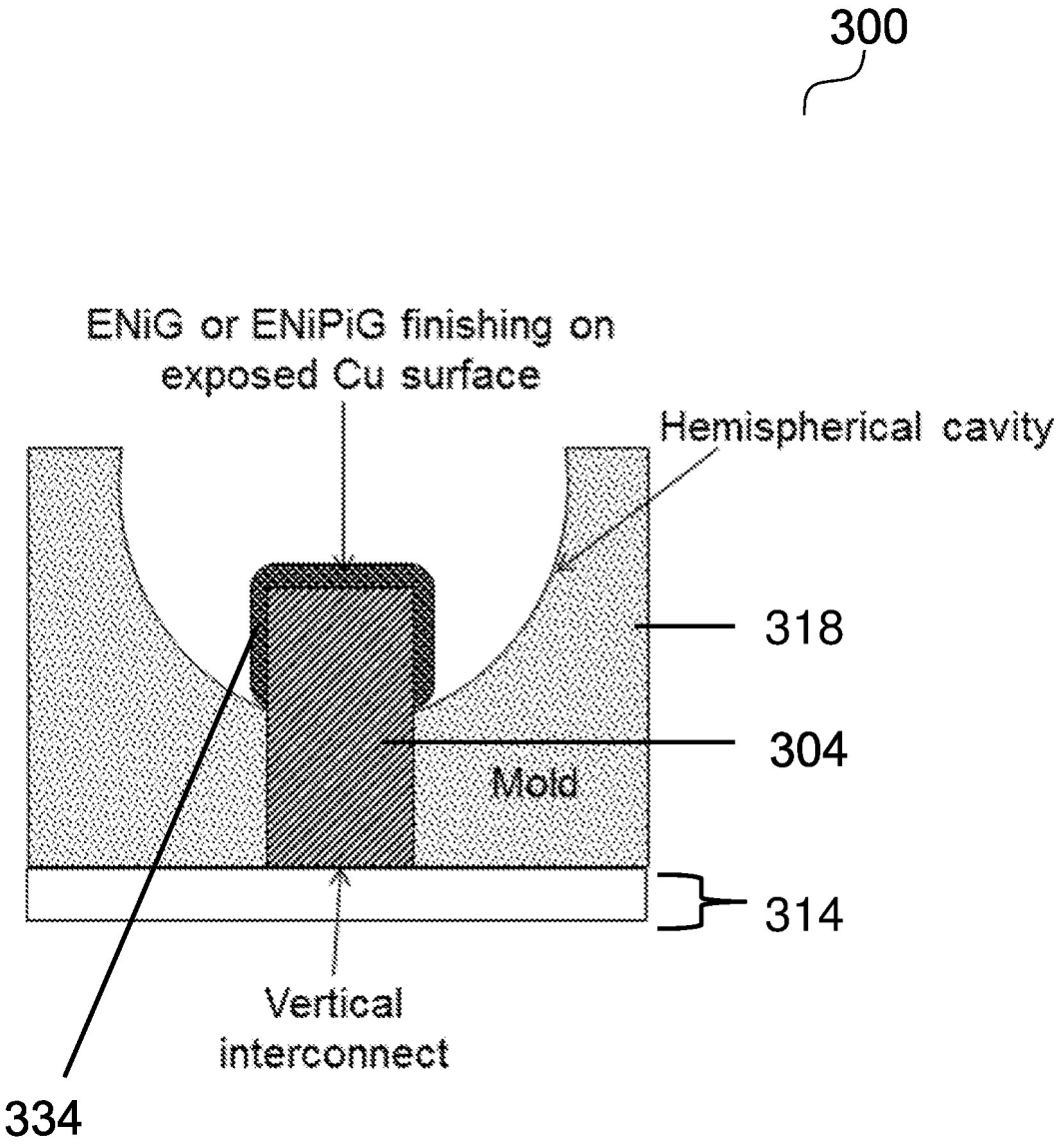

300
ENiG or ENiPiG finishing on exposed Cu surface
Hemispherical cavity
318
304
Mold
314
Vertical interconnect
334

FIG. 3E

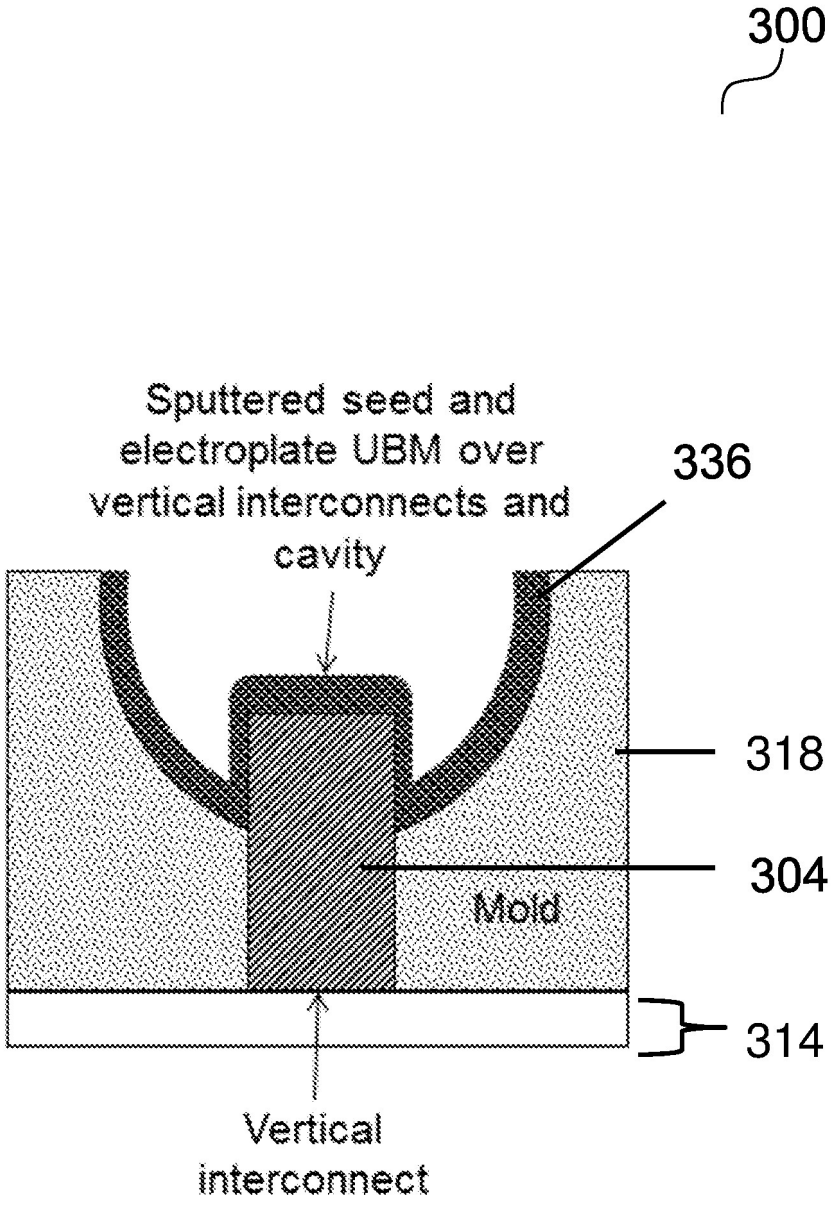

300
Sputtered seed and electroplate UBM over vertical interconnects and cavity
336
318
304
Mold
314
Vertical interconnect

FIG. 4

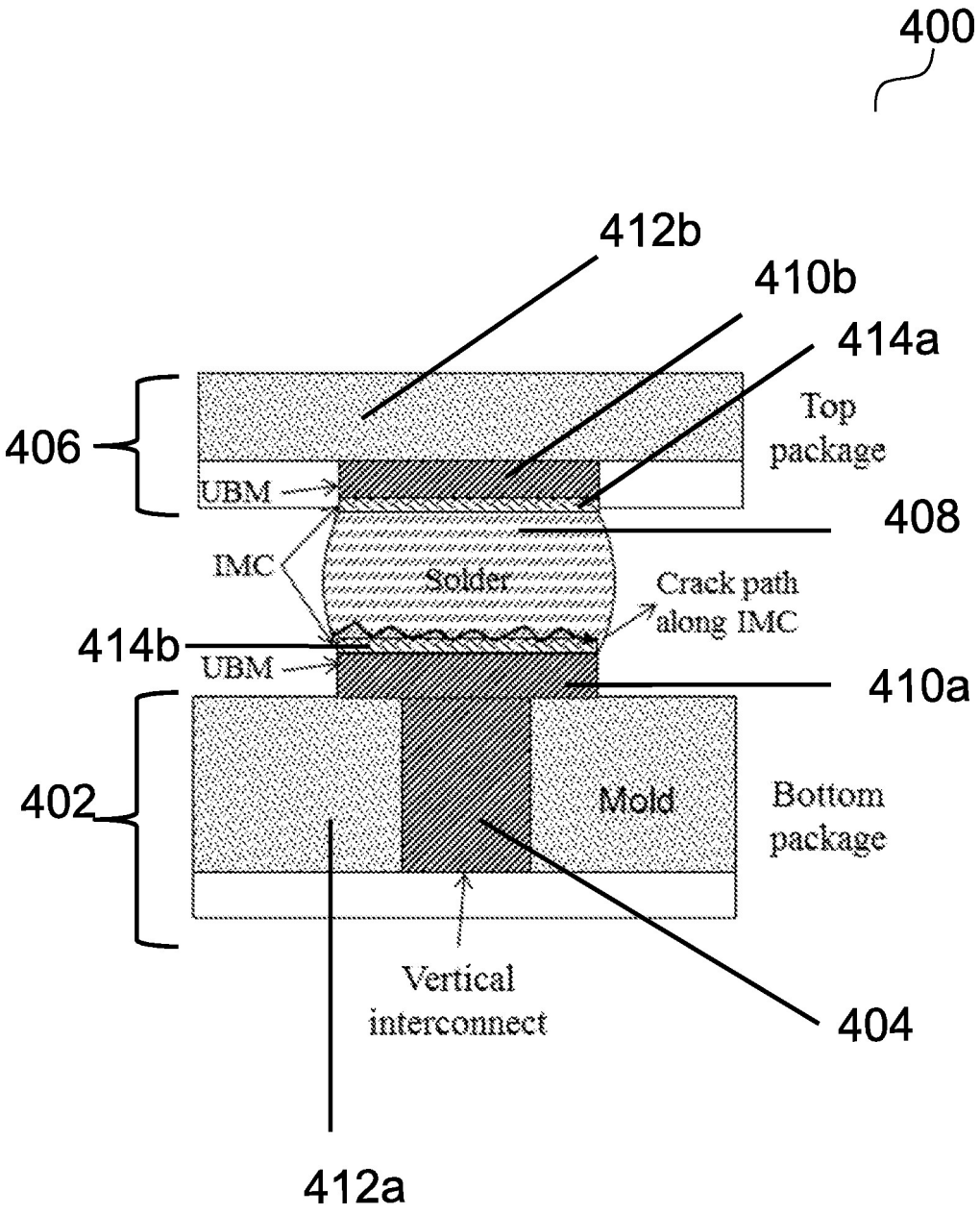

400
412b
410b
414a
406
Top package
UBM
408
IMC
Solder
Crack path along IMC
414b
UBM
410a
402
Mold
Bottom package
Vertical interconnect
404
412a

FIG. 5A

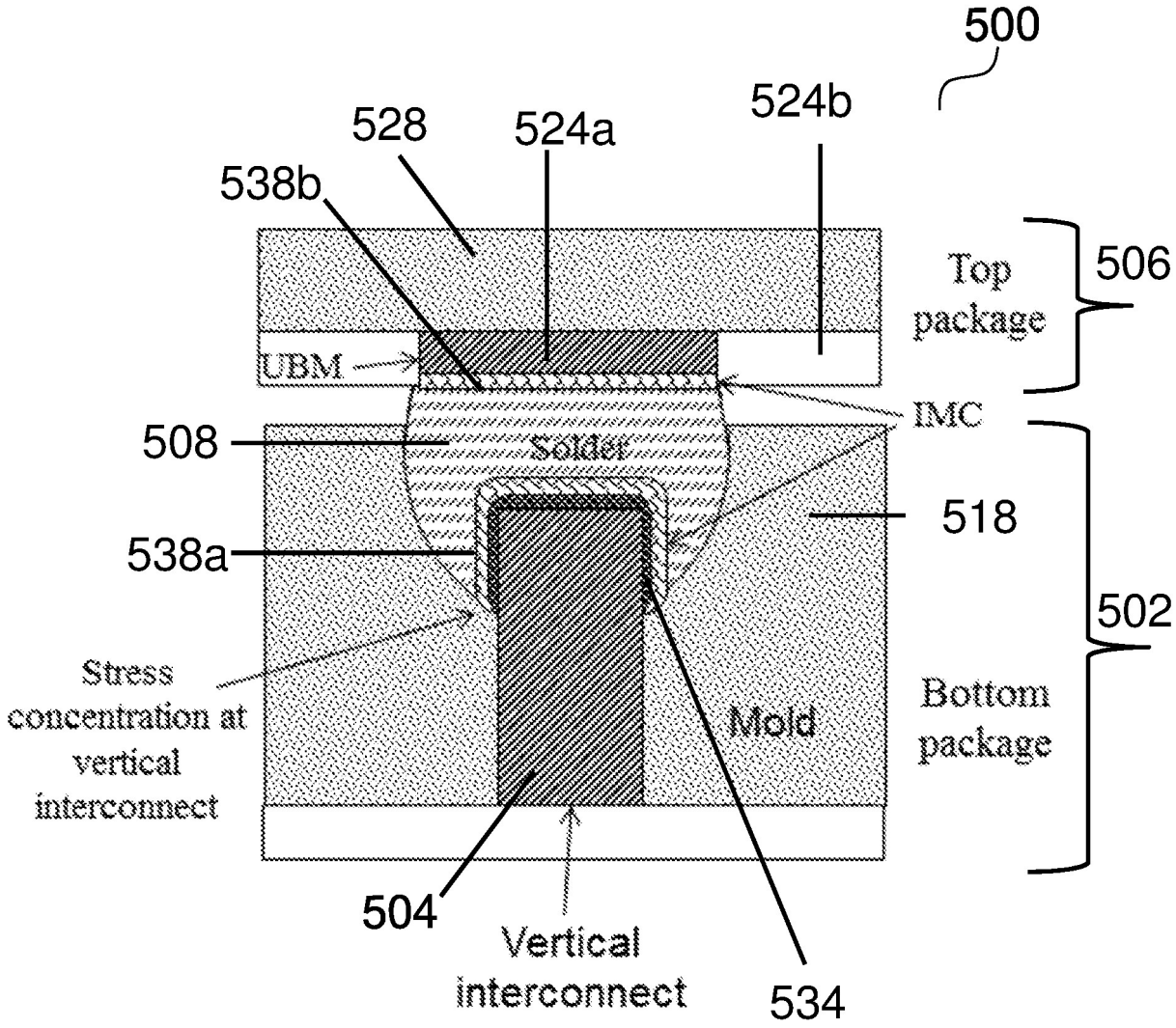

500
528
524a
524b
538b
Top package
506
UBM
IMC
508
Solder
518
538a
502
Stress concentration at vertical interconnect
Bottom package
Mold
504
Vertical interconnect
534

FIG. 5B

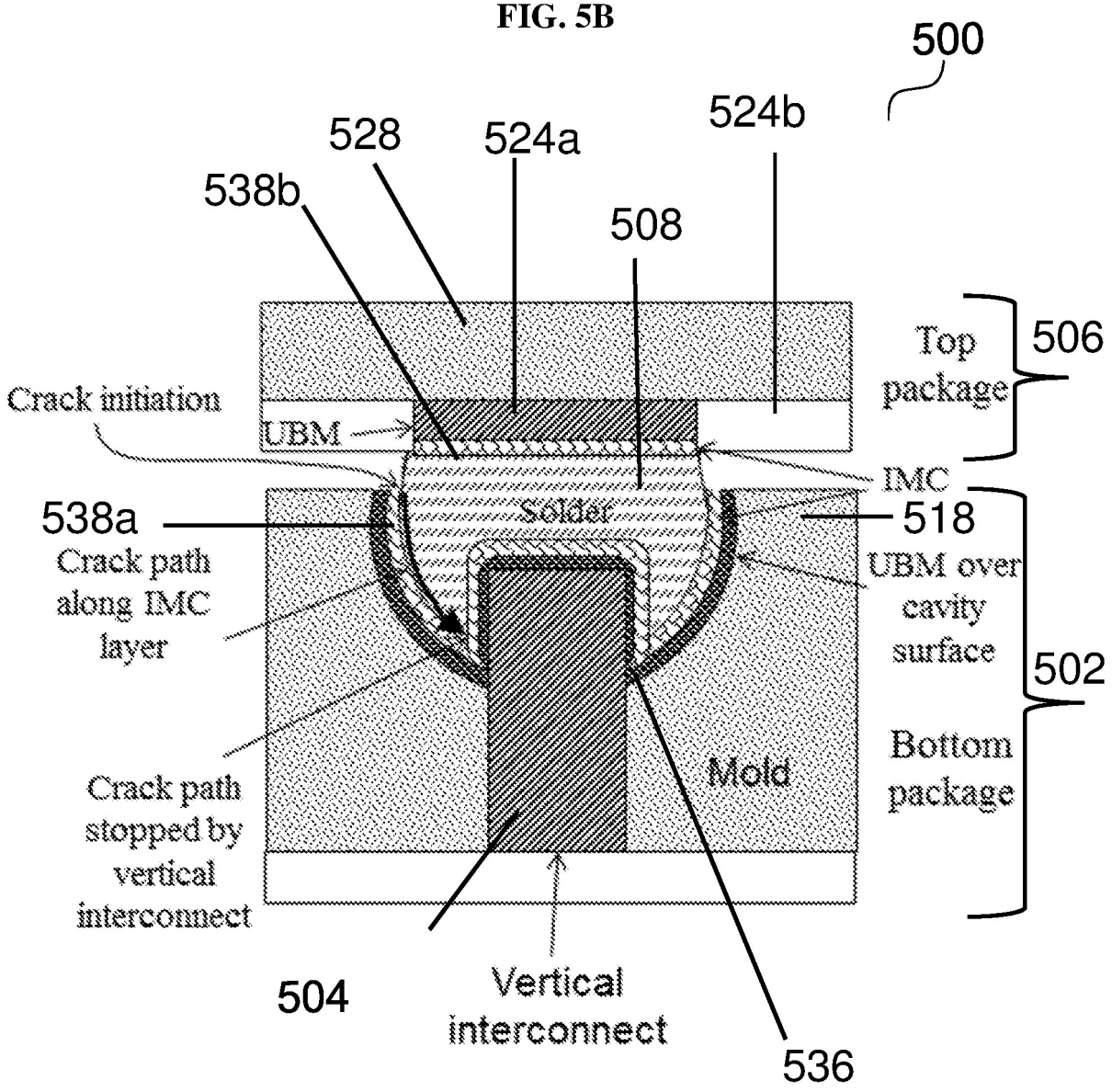

500
528
524a
524b
538b
508
Top package
506
Crack initiation
UBM
IMC
Solder
538a
518
Crack path along IMC layer
UBM over cavity surface
502
Bottom package
Mold
Crack path stopped by vertical interconnect
504
Vertical interconnect
536

FIG. 6A

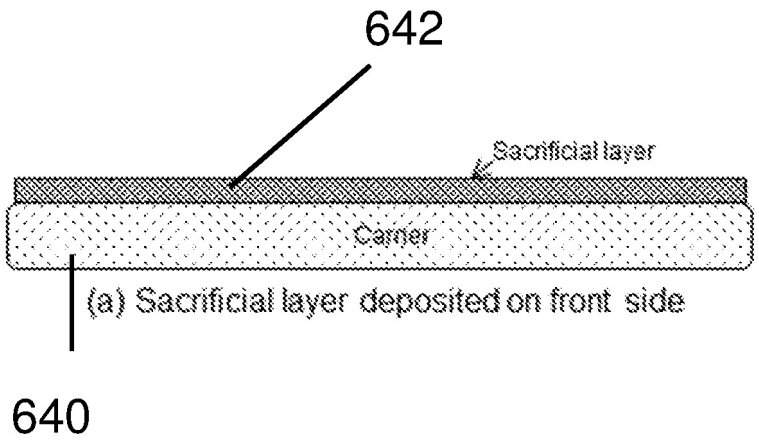

642
Sacrificial layer
Carrier
(a) Sacrificial layer deposited on front side
640

FIG. 6B

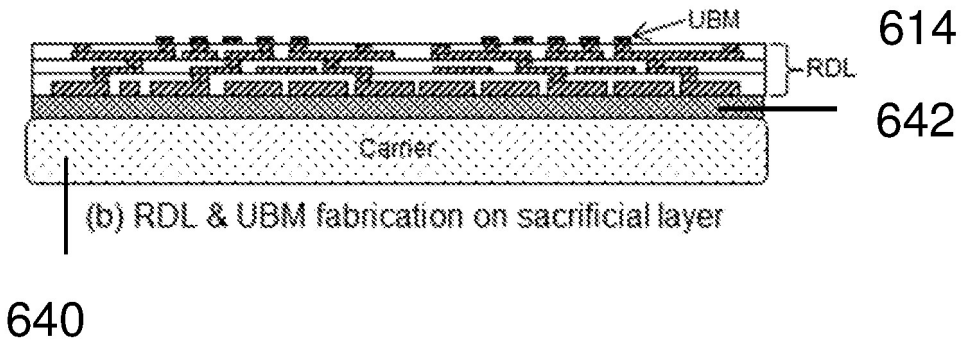
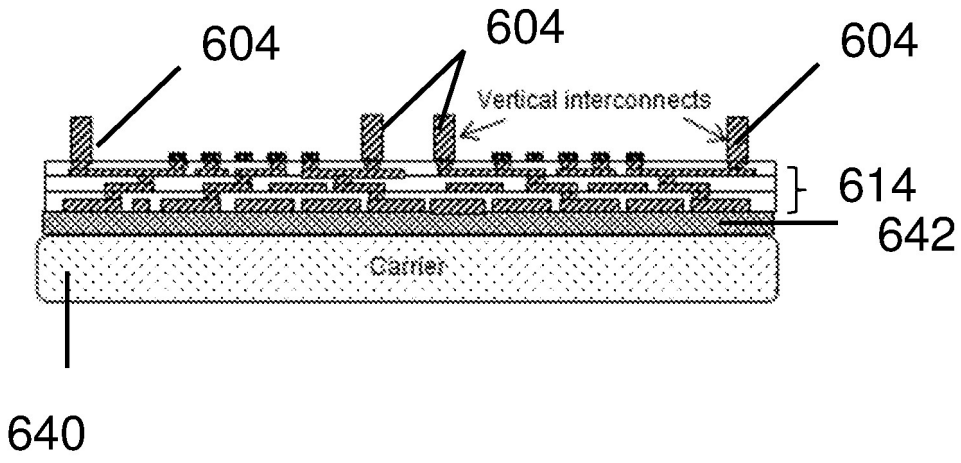
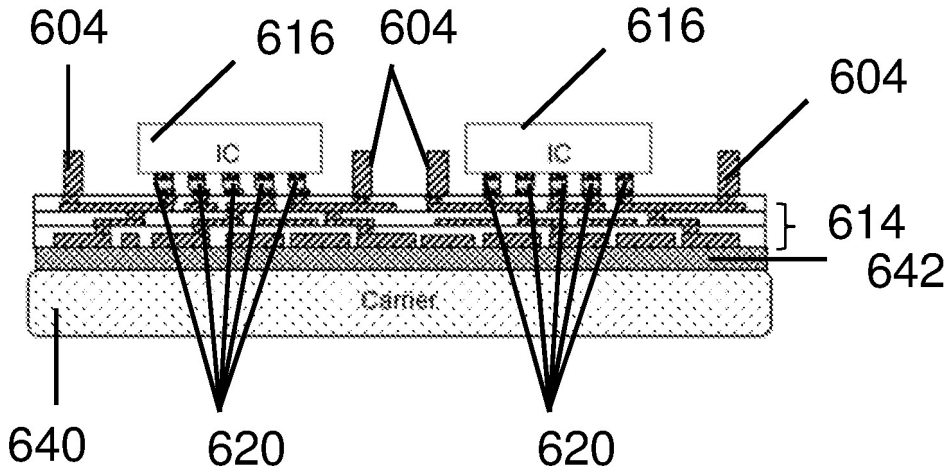

UBM
614
RDL
642
Carrier
(b) RDL & UBM fabrication on sacrificial layer
640

FIG. 6C



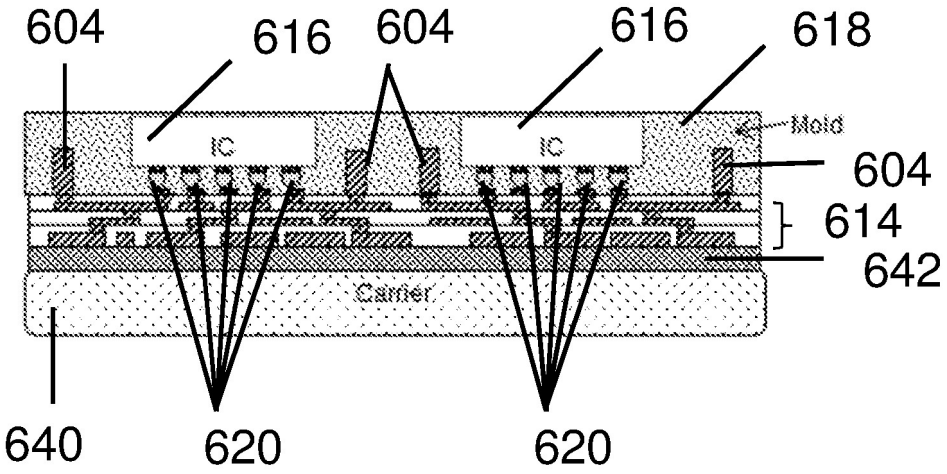
(c) Vertical interconnect formation (Cu wire or pillar)

FIG. 6D



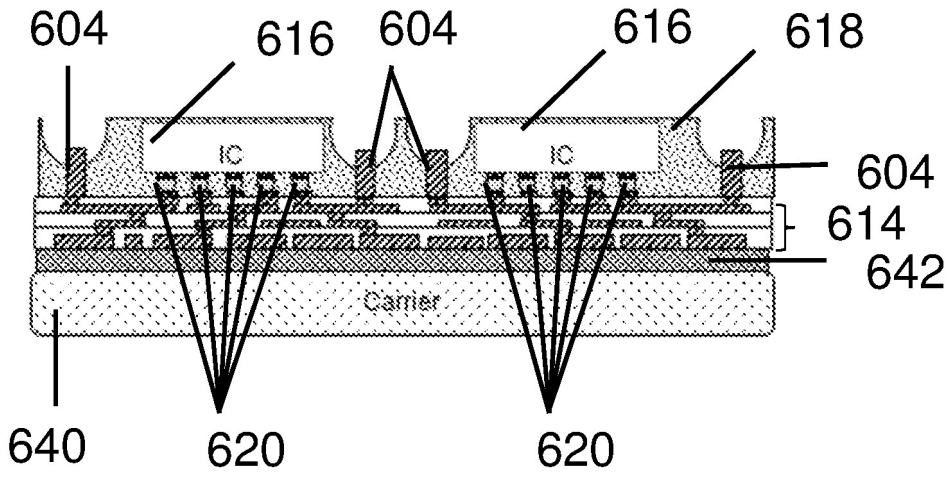
(d) Chip 2 wafer assembly

FIG. 6E



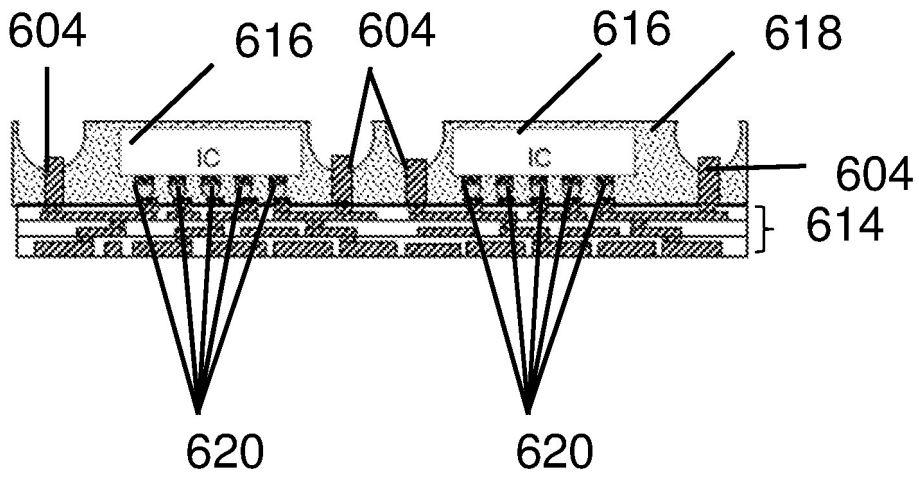
(e) Wafer level compression molding

FIG. 6F



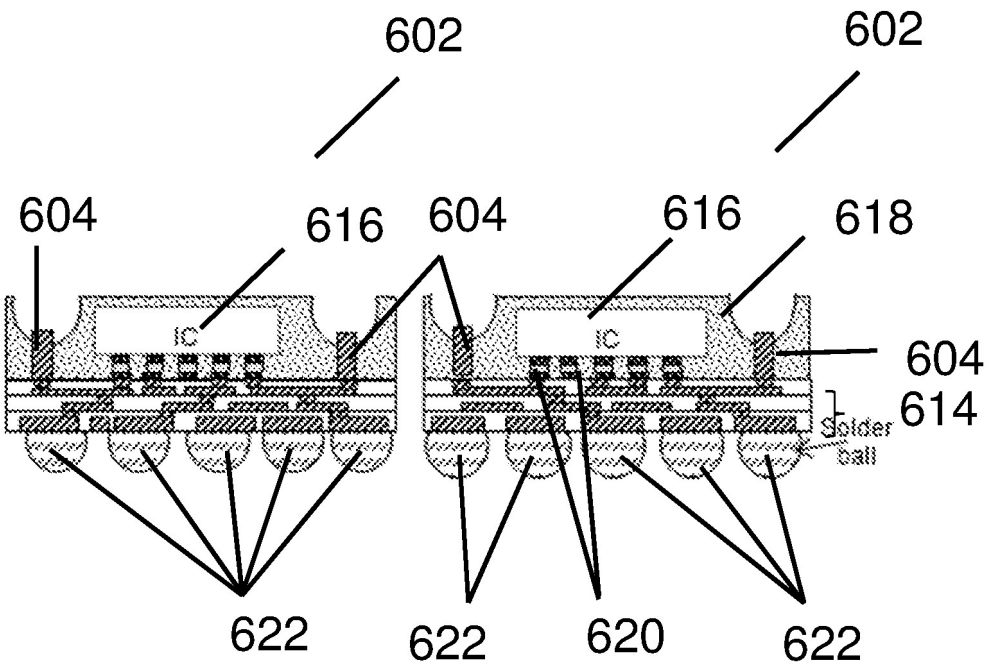
(f) Formation of hemispherical cavity on top of vertical interconnect & optional surface finishing

FIG. 6G



(g) Wafer de-bond from glass wafer

FIG. 6H



(h) Singulation & solder balls drop

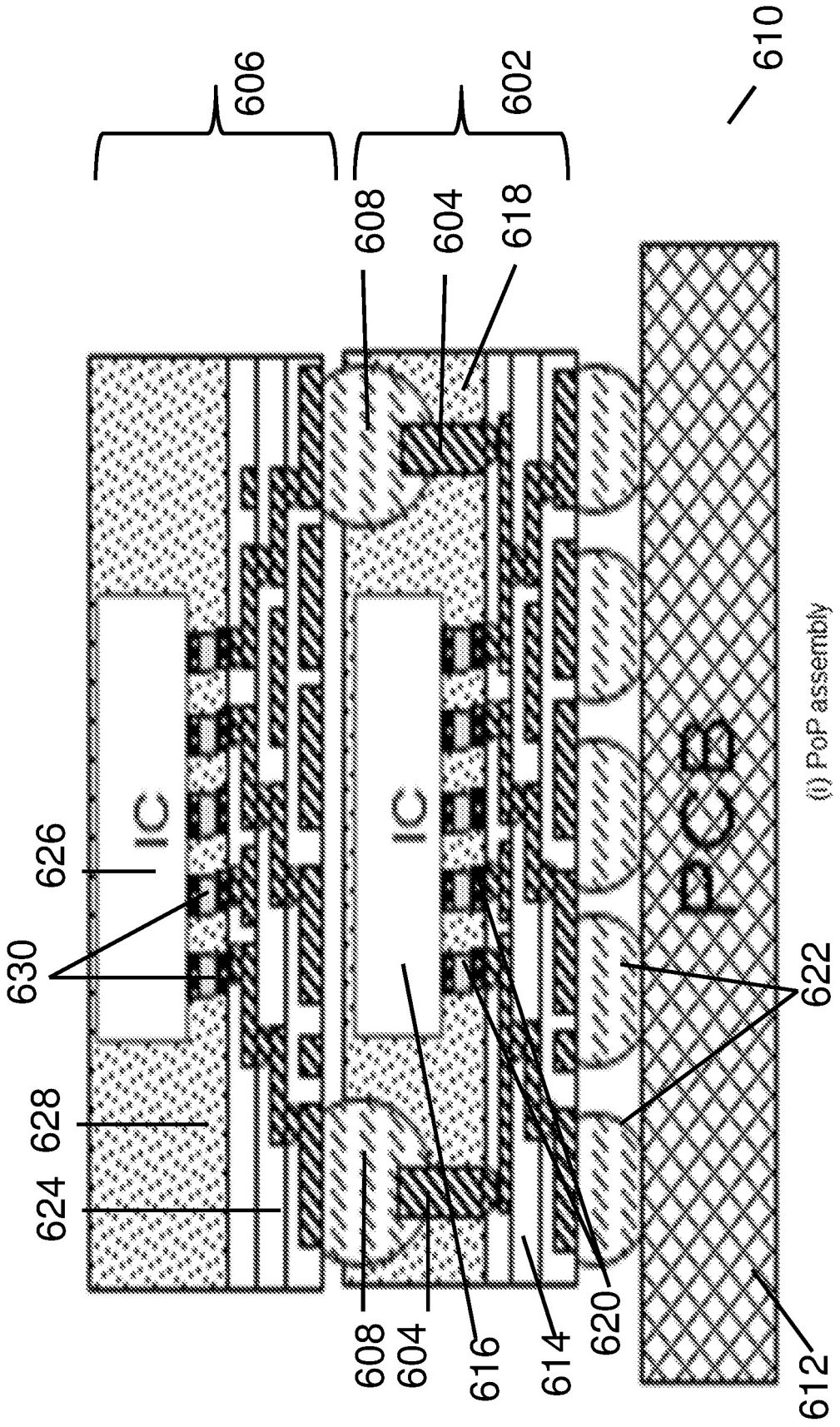

606
602
610
608
604
618
IC
IC
626
630
628
624
PCB
622
(i) PoP assembly
608
604
616
614
620
612

FIG. 6I