CLAIMS:

1. An apparatus, comprising:

a pattern dependent delay circuit including:

a pattern detector to detect a switching pattern of at least three data signals on respective wires, wherein individual data signals of the at least three data signals switch between at least three logic states; and

a delay module coupled to the pattern detector to adaptively change delays of the at least three data signals based on the detected switching pattern, wherein the delay module comprises a plurality of delay controllers and a plurality of samplers, wherein individual delay controllers are paired with individual samplers to receive a clock signal and add a delay to the clock signal to cause delay of respective individual data signals of the at least three data signals; and

a transmitter, coupled to the pattern dependent delay circuit, to transmit the at least three data signals, wherein the transmitter is a channel physical layer (C-PHY) transmitter.

2. The apparatus of claim 1, wherein the at least three data signals are in different logic states.

3. The apparatus of claim 1, wherein the pattern detector is to detect the switching pattern based on a prior logic state and a current logic state of the at least three data signals.

4. The apparatus of claim 1, wherein the pattern detector is to send one or more control signals to the delay module to change the delays of the at least three data signals when the pattern detector detects that the at least three data signals are each undergoing a state transition during a same time period.

5. The apparatus of claim 1, wherein the delay module is to cause different delays for each of the at least three data signals.

6. The apparatus of claim 1, wherein the pattern dependent delay circuit is to adaptively change the delays of the at least three data signals before the transmitter transmits the at least three data signals to reduce a switching jitter associated with the at least three data signals.

7. The apparatus of claim 1, wherein the pattern dependent delay circuit is to reduce a C-PHY switching jitter.

8. A system, comprising:

a processor;

a controller coupled to the processor to output data processed by the processor;

a transmitter coupled to the controller to transmit the data using at least three data signals, wherein individual data signals of the at least three data signals switch between at least three logic states; and

a pattern dependent delay circuit, coupled to the transmitter, to detect a switching pattern of the at least three data signals and adaptively reduce a switching jitter based on the detected switching pattern, wherein the pattern dependent delay circuit includes a plurality of delay controllers and a plurality of samplers, wherein individual delay controllers are paired with individual samplers to receive a clock signal and add a delay to the clock signal to cause delay of respective individual data signals of the at least three data signals, and wherein at least one of the samplers has an operating frequency of at least 2.5 giga-samples per second (Gsps).

9. The system of claim 8, wherein the pattern dependent delay circuit is to reduce a channel physical layer (C-PHY) switching jitter by changing delays on the at least three data signals before the transmitter transmits the at least three data signals.

10. The system of claim 8, wherein the transmitter is a physical layer transmitter to deliver at least 2.28 bits per symbol over a set of three wires using 3-phase encoding.

11. A method, comprising:

detecting, by a pattern dependent delay circuit, a switching pattern of at least three data signals on respective wires, wherein individual data signals of the at least three data signals switch between at least three logic states;

causing, by the pattern dependent delay circuit, a delay on one or more of the at least three data signals based on the detected switching pattern, wherein the causing the delay includes receiving, by a delay controller and a sampler of the pattern dependent delay circuit, a clock signal and adding a delay to the clock signal to cause delay of a respective data signal of the three or more data signals, wherein the sampler has an operating frequency of at least 2.5 giga-samples per second (Gsps); and

transmitting the at least three data signals including the delay on the one or more of the at least three data signals.

12. The method of claim 11, wherein the detecting comprises detecting a logic state of individual data signals of the at least three data signals, wherein the logic state is one of the at least three logic states.

13. The method of claim 11, wherein the detecting comprises detecting the switching pattern based on a prior logic state and a current logic state of the at least three data signals.

14. The method of claim 11, wherein the causing the delay is responsive to a detection that each of the at least three data signals switches to a different logic state from a prior logic state.

15. The method of claim 11, wherein the causing comprises changing delays on each of the at least three data signals based on the switching pattern.

16. The method of claim 11, wherein the causing comprises causing different delays on each of the at least three data signals based on the switching pattern.

17. The method of claim 11, wherein the causing comprises reducing a channel physical layer (C-PHY) switching jitter.

18. The method of claim 17, wherein the causing comprises reducing the channel physical layer (C-PHY) switching jitter by adjusting a switching timing for the at least three data signals based on the delay.

19. The method of claim 11, wherein the transmitting comprises transmitting the at least three data signals to a peripheral device using 3-phase symbol encoding over a set of 3 wires.

20. An apparatus, comprising:

a pattern dependent delay circuit including:

a pattern detector to detect a switching pattern of at least three data signals on respective wires, wherein individual data signals of the at least three data signals switch between at least three logic states; and

a delay module coupled to the pattern detector to adaptively change delays of the at least three data signals based on the detected switching pattern, wherein the delay module comprises a plurality of delay controllers and a plurality of samplers, wherein individual delay controllers are paired with individual samplers to receive a clock signal and add a delay to the clock signal to cause delay of respective individual data signals of the at least three data

signals, and wherein at least one of the samplers has an operating frequency of at least 2.5 giga-samples per second (Gsps); and

a transmitter, coupled to the pattern dependent delay circuit, to transmit the at least three data signals.