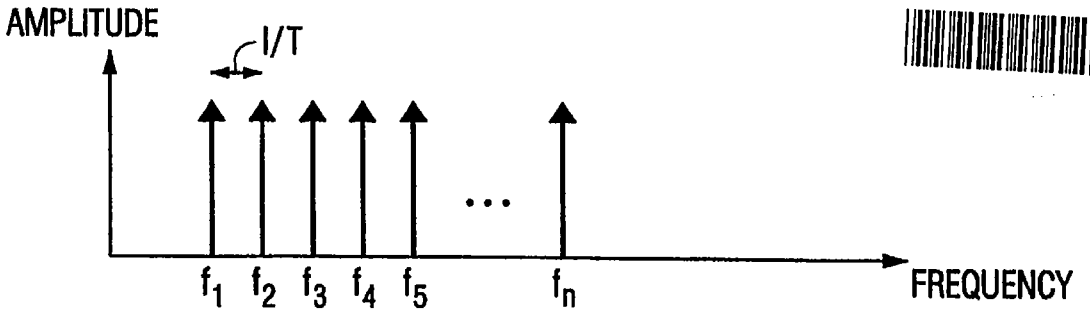


FIG. 1a

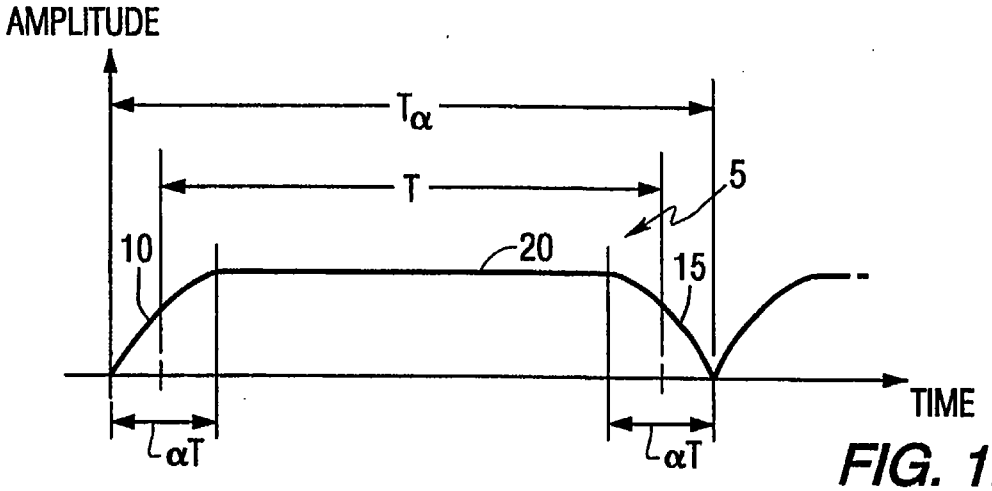


FIG. 1b

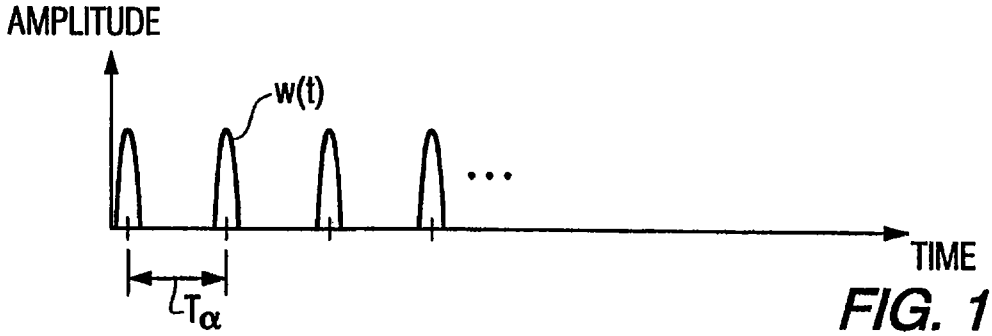


FIG. 1c

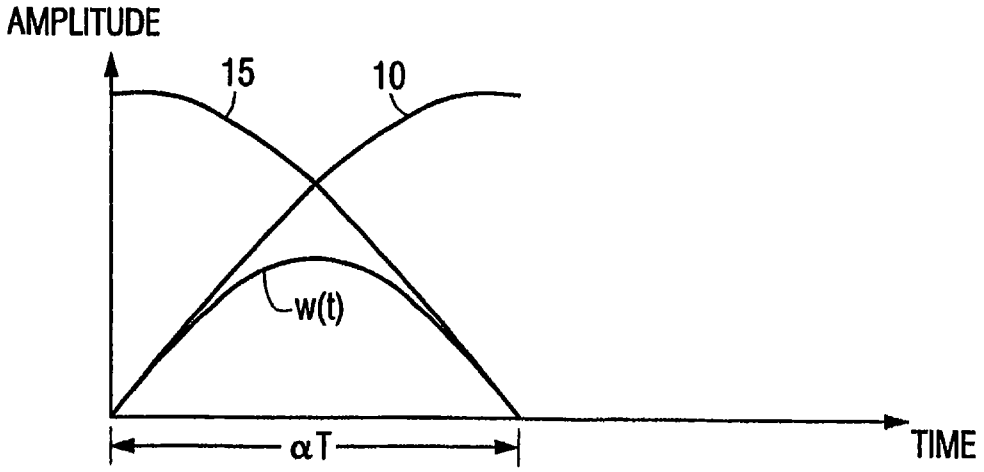


FIG. 1d

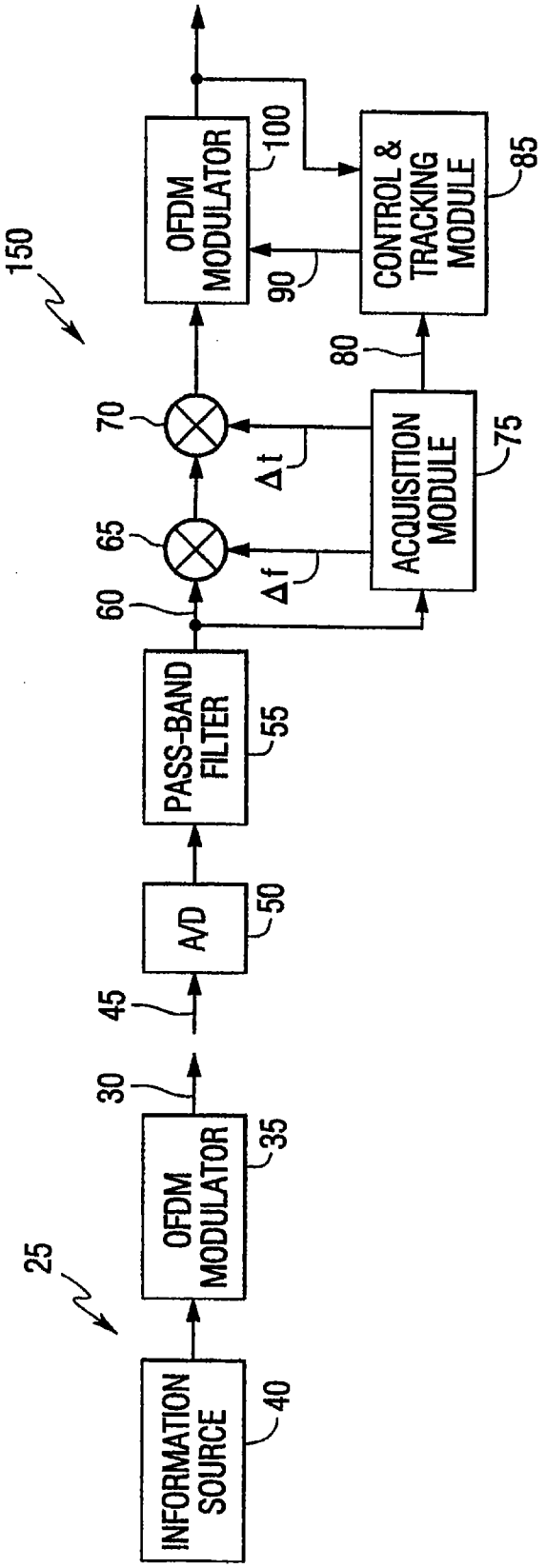

150
25
INFORMATION SOURCE
40
OFDM MODULATOR
35
30
45
A/D
50
PASS-BAND FILTER
55
60
65
70
Δf
Δt
ACQUISITION MODULE
75
80
CONTROL & TRACKING MODULE
85
90
OFDM MODULATOR
100

FIG. 2

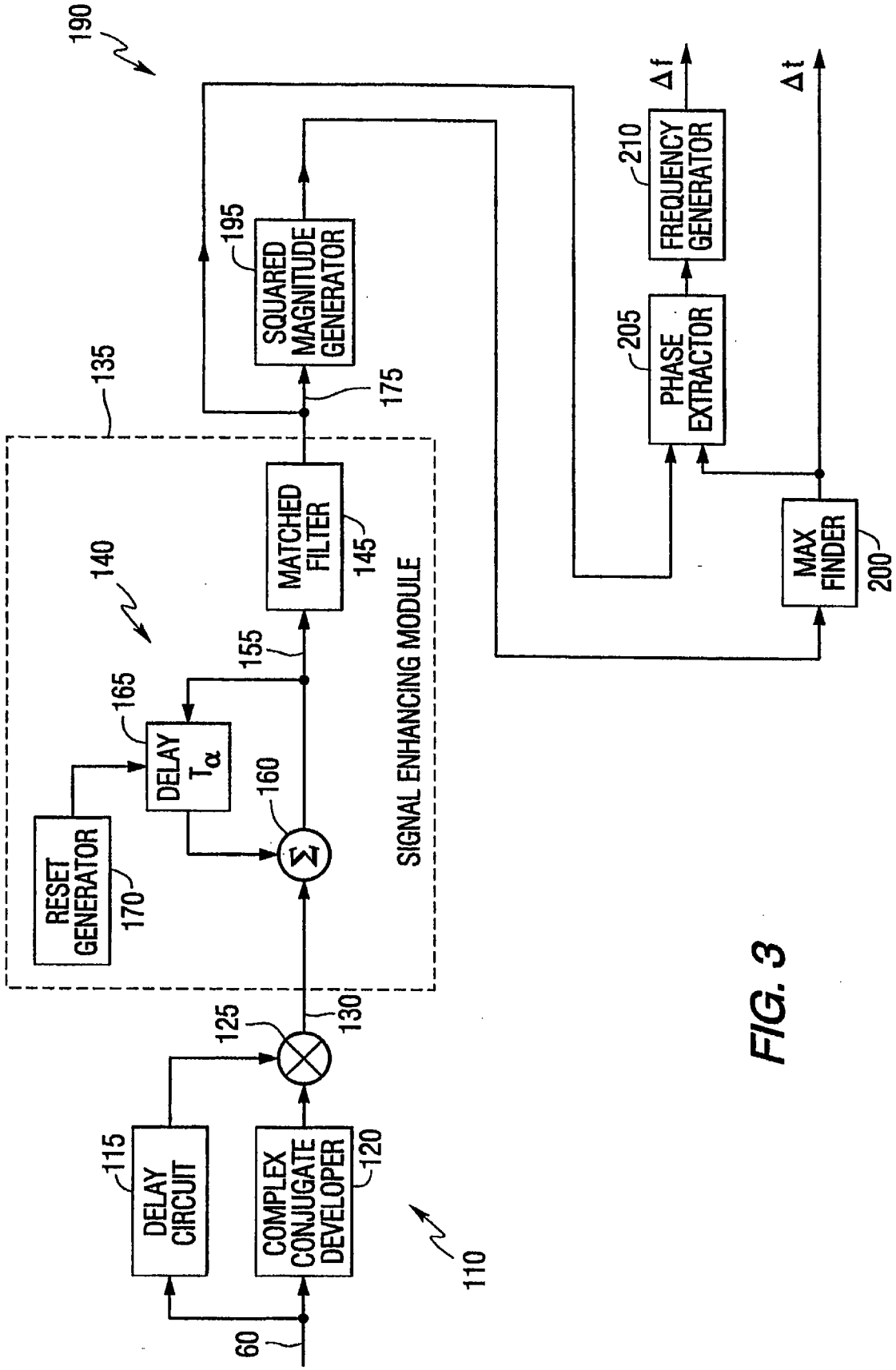

190
195
SQUARED MAGNITUDE GENERATOR
210
FREQUENCY GENERATOR
Δf
Δt
205
PHASE EXTRACTOR
135
175
MATCHED FILTER
145
MAX FINDER
200
140
SIGNAL ENHANCING MODULE
155
165
DELAY T_α
160
RESET GENERATOR
170
125
130
115
DELAY CIRCUIT
COMPLEX CONJUGATE DEVELOPER
120
110
60

FIG. 3

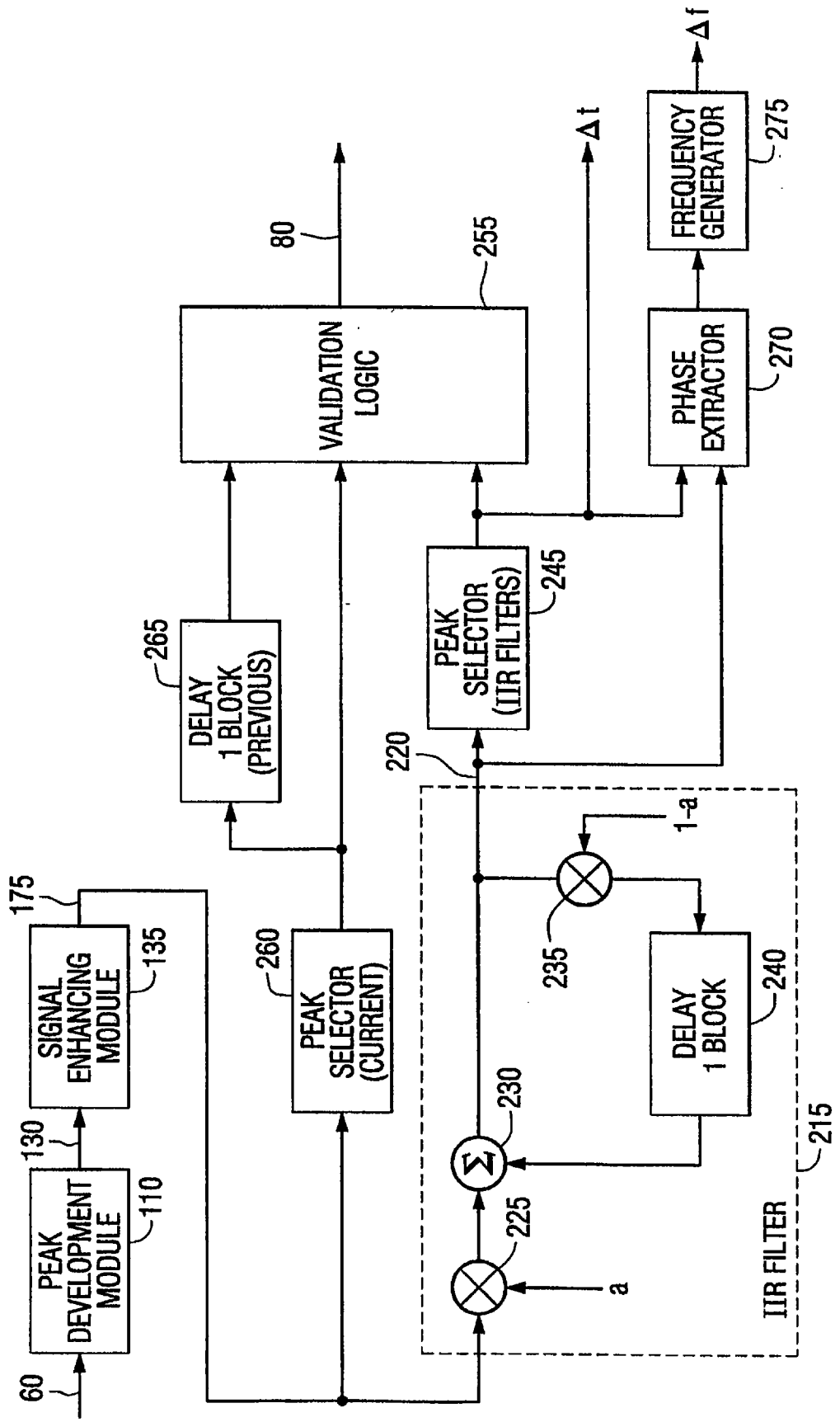

60
PEAK DEVELOPMENT MODULE
110
130
SIGNAL ENHANCING MODULE
135
175
PEAK SELECTOR (CURRENT)
260
DELAY 1 BLOCK (PREVIOUS)
265
VALIDATION LOGIC
255
80
Δ t
Δ f
FREQUENCY GENERATOR
275
PHASE EXTRACTOR
270
PEAK SELECTOR (IIR FILTERS)
245
220
IIR FILTER
215
1-a
235
DELAY 1 BLOCK
240
230
Σ
225
a

FIG. 4

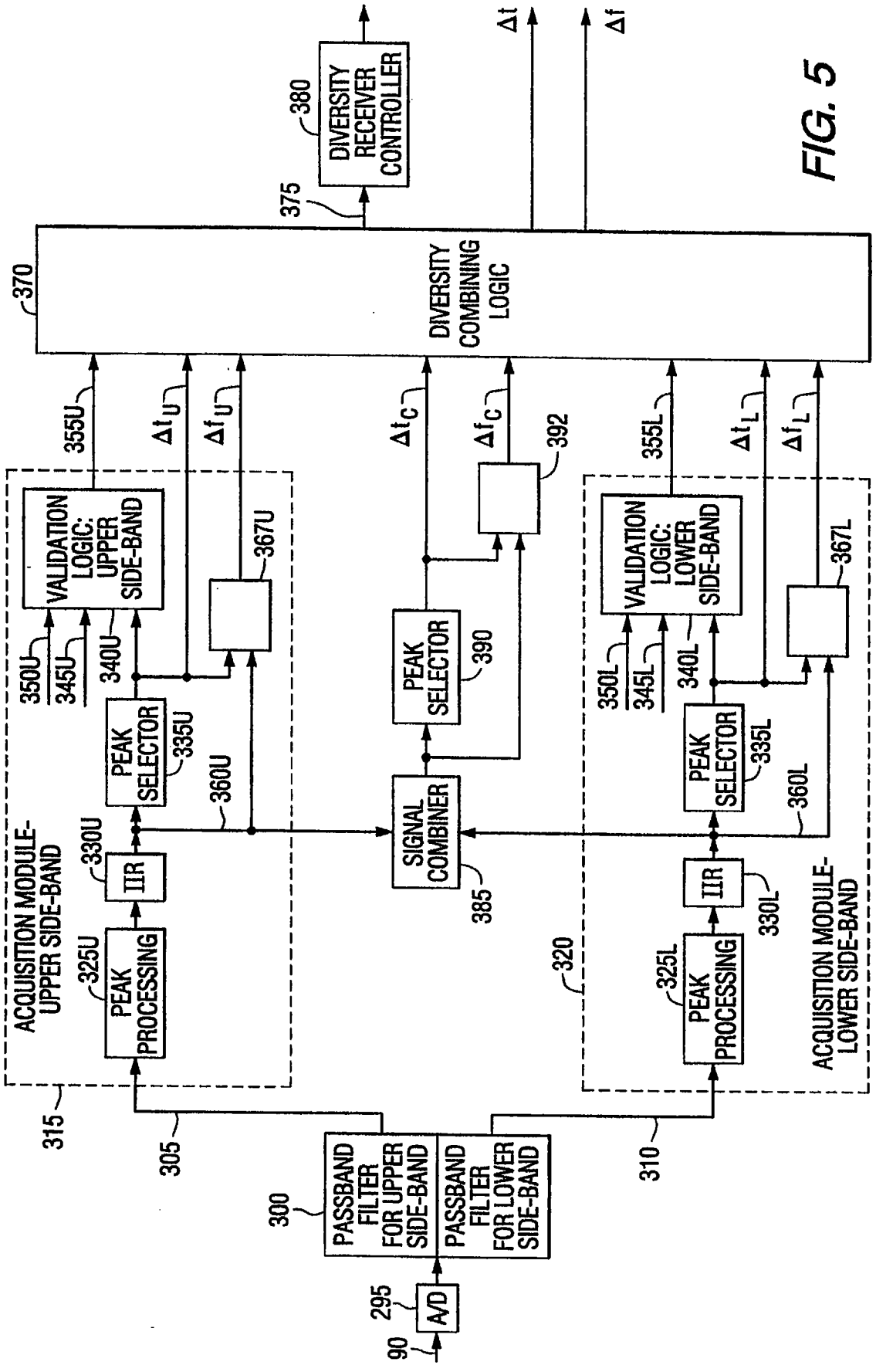

DIVERSITY RECEIVER CONTROLLER
380
375
Δt
Δf
DIVERSITY COMBINING LOGIC
370
355U
Δt_U
Δf_U
Δt_C
Δf_C
392
355L
Δt_L
Δf_L
VALIDATION LOGIC: UPPER SIDE-BAND
367U
PEAK SELECTOR
390
VALIDATION LOGIC: LOWER SIDE-BAND
367L
350U
345U
340U
335U
360U
330U
IIR
325U
PEAK PROCESSING
SIGNAL COMBINER
385
350L
345L
340L
335L
360L
330L
325L
ACQUISITION MODULE-UPPER SIDE-BAND
315
320
ACQUISITION MODULE-LOWER SIDE-BAND
305
310
300
PASSBAND FILTER FOR UPPER SIDE-BAND
PASSBAND FILTER FOR LOWER SIDE-BAND
295
A/D
90

FIG. 5

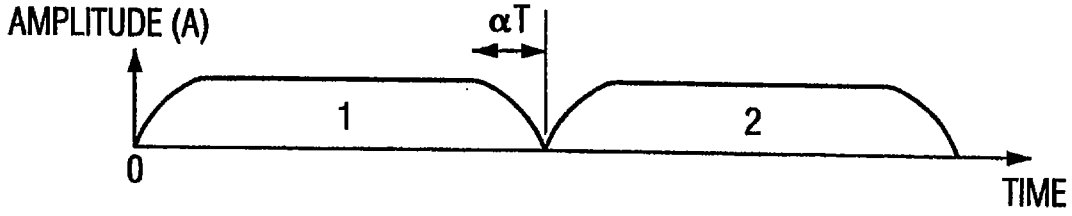


FIG. 6a

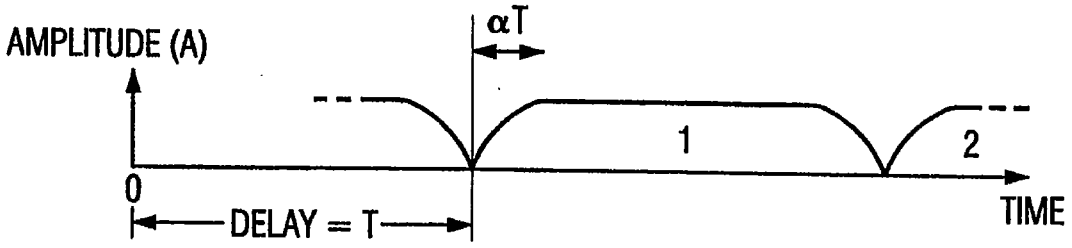


FIG. 6b

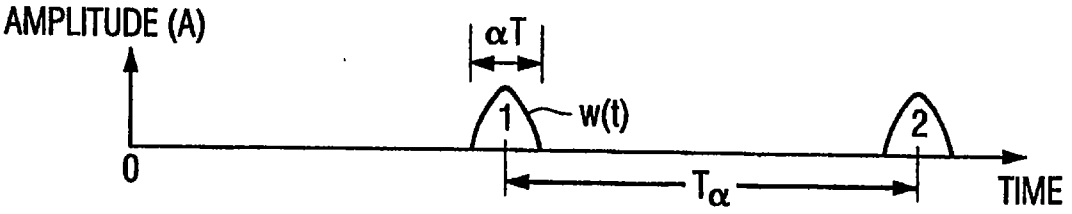


FIG. 6c

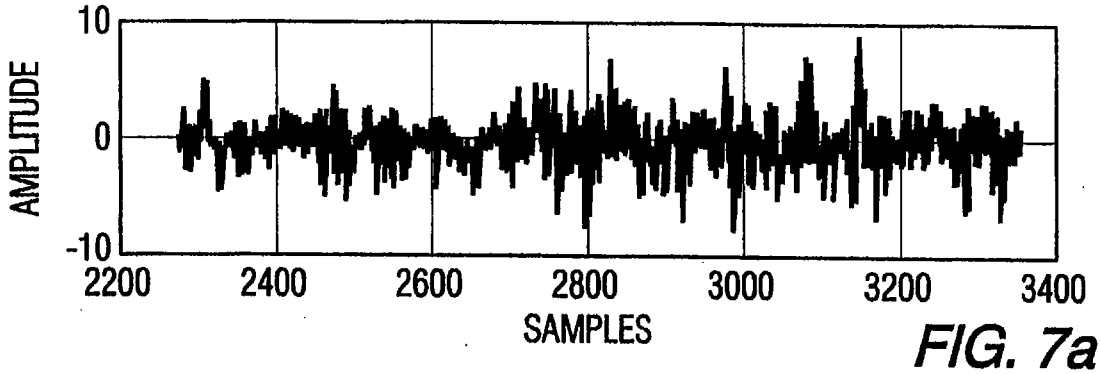


FIG. 7a

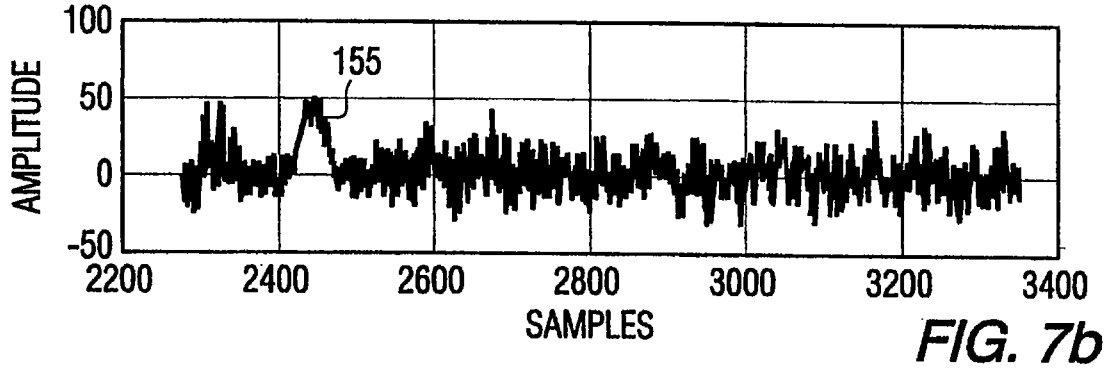


FIG. 7b

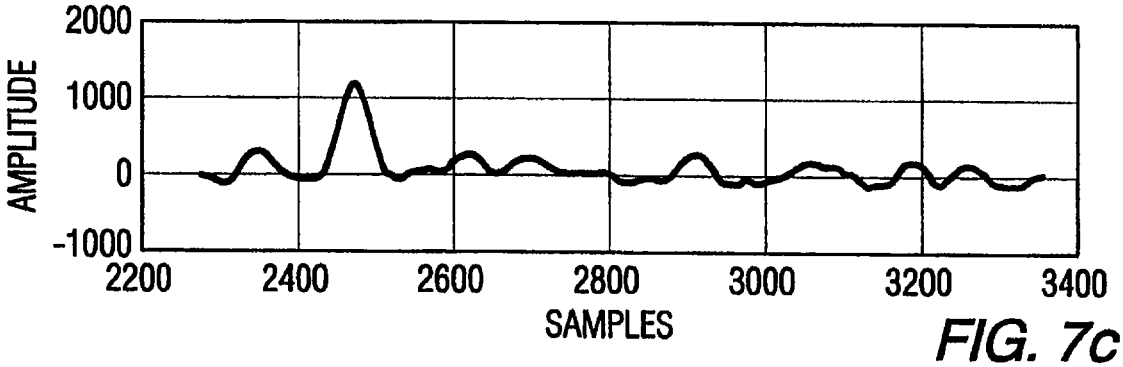


FIG. 7c

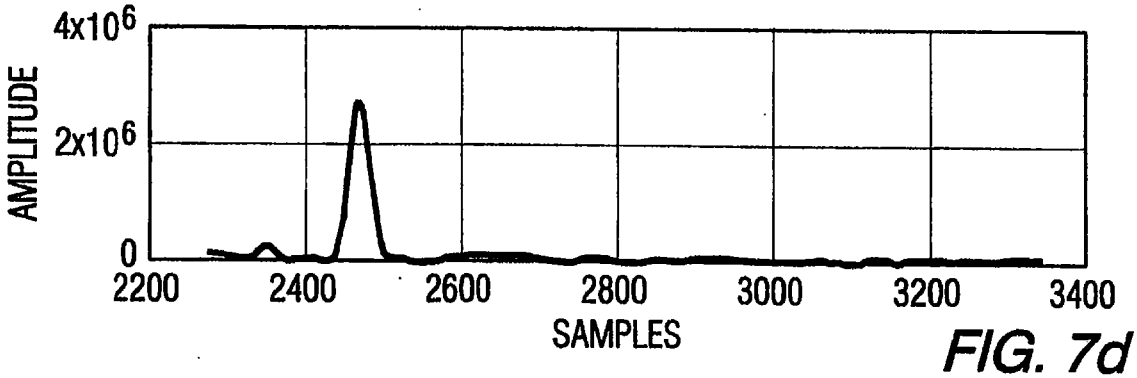


FIG. 7d

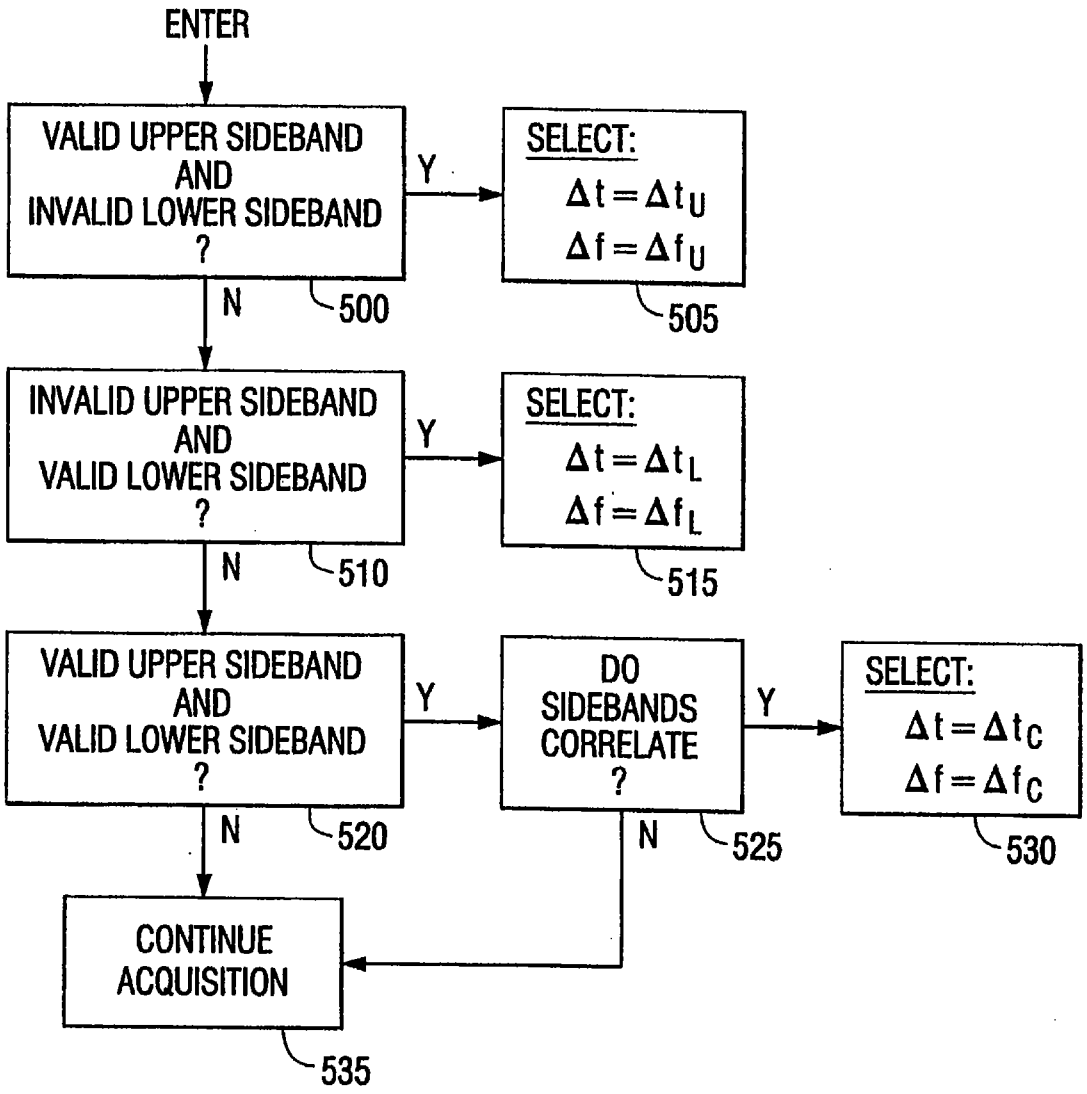

ENTER
VALID UPPER SIDEBAND AND INVALID LOWER SIDEBAND ?
Y
SELECT: Δt = Δt_U Δf = Δf_U
505
N
500
INVALID UPPER SIDEBAND AND VALID LOWER SIDEBAND ?
Y
SELECT: Δt = Δt_L Δf = Δf_L
515
N
510
VALID UPPER SIDEBAND AND VALID LOWER SIDEBAND ?
Y
DO SIDEBANDS CORRELATE ?
Y
SELECT: Δt = Δt_C Δf = Δf_C
530
N
520
N
525
CONTINUE ACQUISITION
535

FIG. 8