

CLAIMS

1. A memory device, comprising:

a substrate;

5 a structure including a plurality of conductive layers stacked on the substrate; and

a pillar arranged inside the structure, the pillar including:

a core layer;

10 a semiconductor layer extending in a direction perpendicular to a surface of the substrate and including a first portion on a side of an upper portion of the structure, and a second portion in contact with an outer surface of the core layer between the first portion of the semiconductor layer and the substrate; and

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a reformed layer having a lower end in contact with the first portion of the semiconductor layer.

2. The memory device according to claim 1, wherein

20 the reformed layer includes at least one selected from a nitride, oxide, and carbide of silicon.

3. The memory device according to claim 1, wherein

the first portion of the semiconductor layer includes a third portion below the reformed layer and a fourth portion above the third portion of the semiconductor layer, and

5 the reformed layer includes an inner side surface in contact with the fourth portion of the semiconductor layer.

4. The memory device according to claim 1, wherein the reformed layer includes an outer side surface in
10 contact with the first portion of the semiconductor layer.

5. The memory device according to claim 1, wherein the pillar further includes a memory layer extending in the direction perpendicular to the surface of the
15 substrate, and

the reformed layer includes an outer side surface in contact with the memory layer.

6. The memory device according to claim 1, wherein
20 the reformed layer has a cylindrical or annular shape.

7. The memory device according to claim 1, wherein the pillar at an upper end of the first portion of the semiconductor layer has a diameter smaller than a diameter

of the pillar at a lower end of the first portion of the semiconductor layer.

8. The memory device according to claim 1, wherein
5 the first portion of the semiconductor layer has a reverse tapered shape.

9. The memory device according to claim 1, wherein
the pillar includes an air gap arranged inside the
10 core layer, and
a top end of the air gap in the direction perpendicular to the surface of the substrate is positioned on a side of the substrate with respect to the first portion of the semiconductor layer.