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(54) Title: A STACK ARRANGEMENT

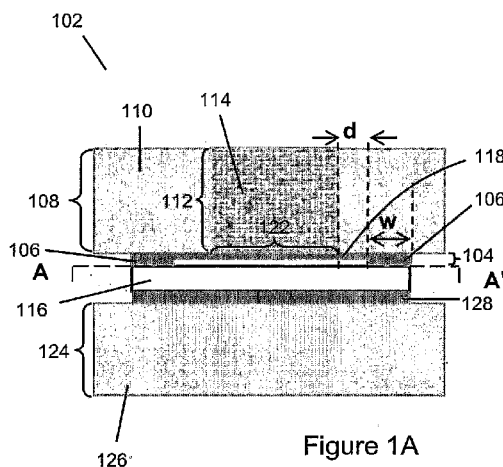


Figure 1A

(57) Abstract: In an embodiment, a stack arrangement is provided. The stack arrangement may include a semiconductor arrangement, the semiconductor arrangement including a substrate; a via formed through the substrate; and a conductive portion arranged in the via. The stack arrangement may further include an interconnect portion arranged over the via; a bond pad portion arranged between the semiconductor arrangement and the interconnect portion, the bond pad portion may include a bond pad circumferential portion arranged at least partially circumferential with respect to the via and at a first distance away from the conductive portion; and at least one bond pad electrical connection extending from within the bond pad circumferential portion to the conductive portion; wherein the interconnect portion may be arranged away from the conductive portion via the bond pad portion.