

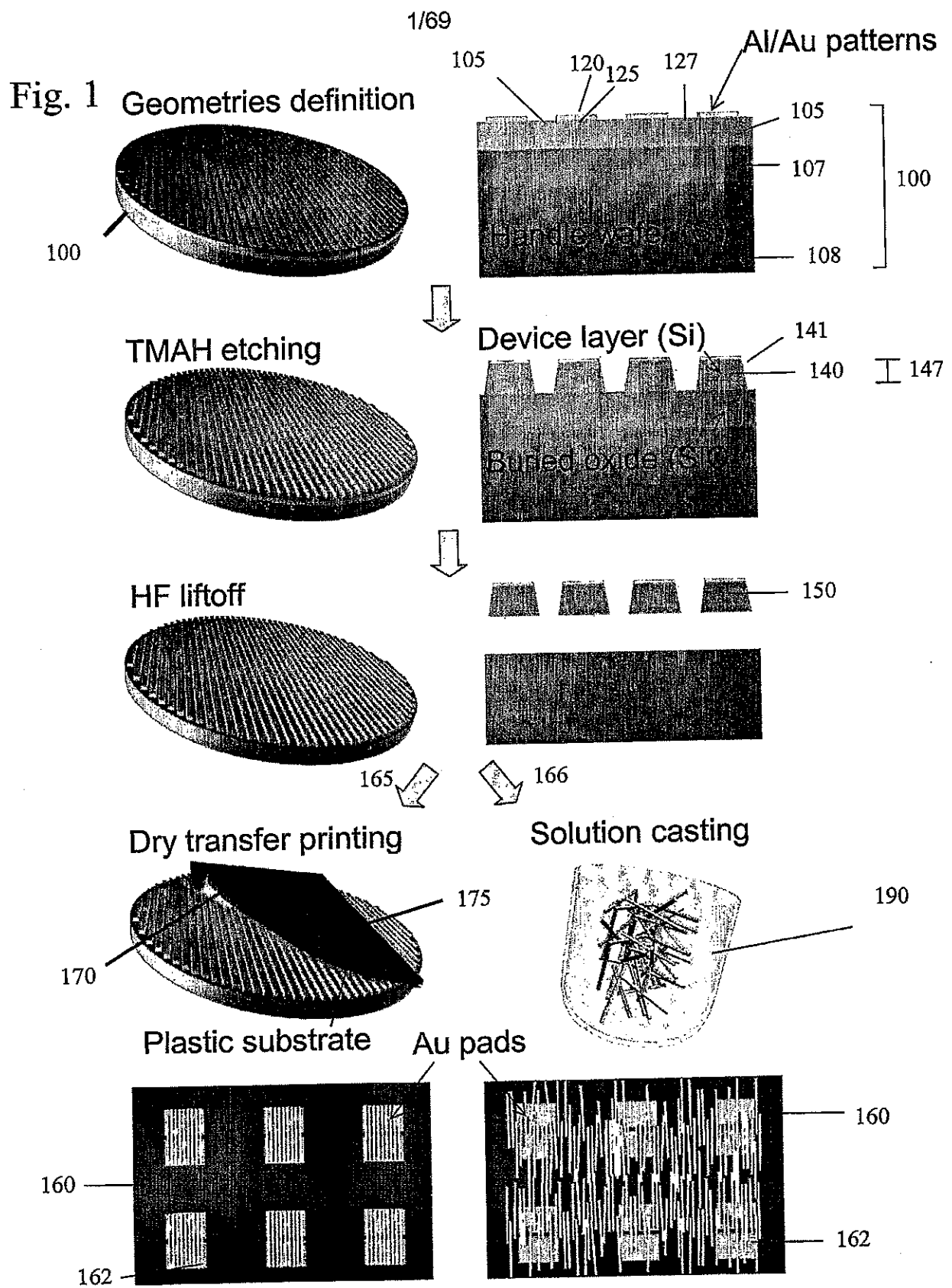
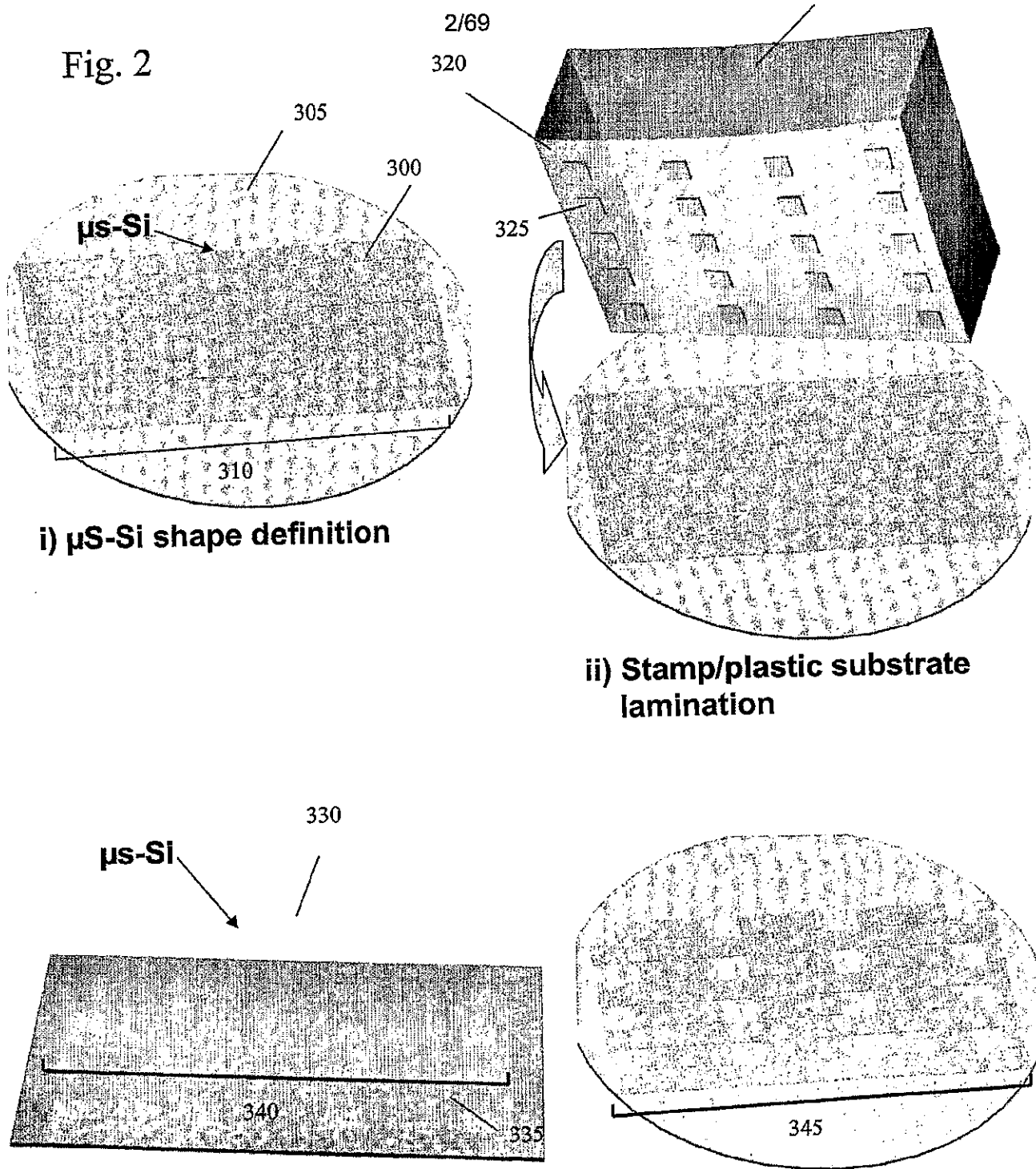
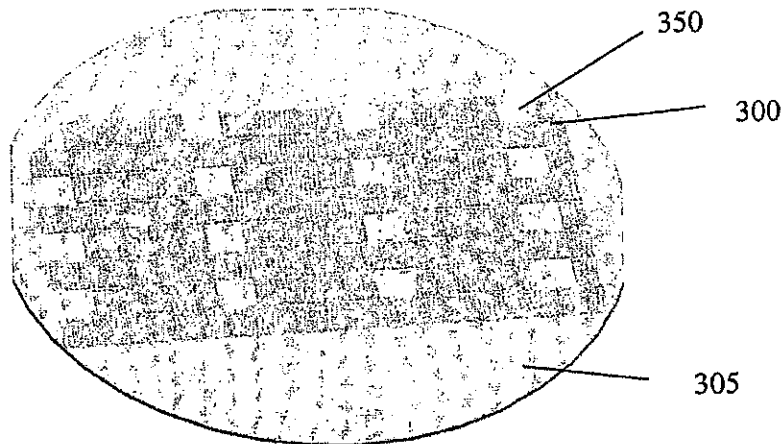


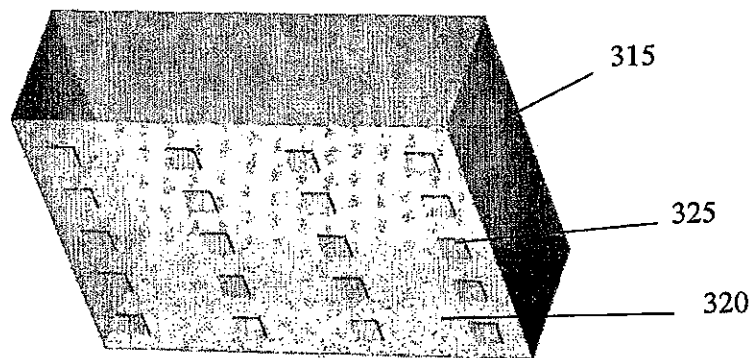
Fig. 2



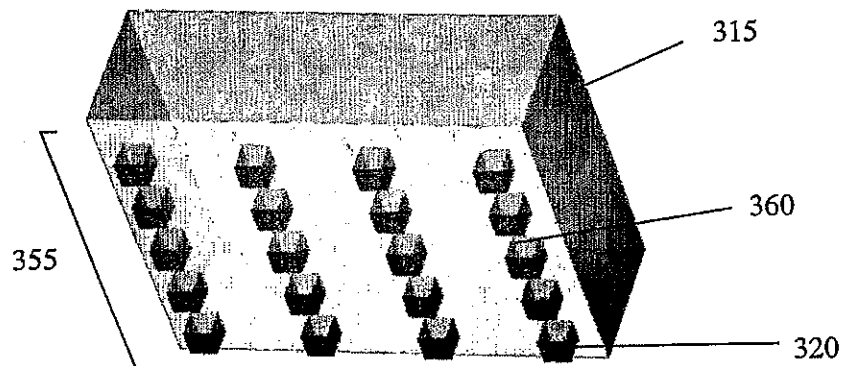
iii) Plastic and mother substrates after transfer

Fig. 3**Fig. 3A**

a) Selective coating of the mother substrate with an adhesive material

Fig. 3B

b) Flat stamp (or plastic substrate) selectively coated with an adhesive

Fig. 3C

c) Structured stamp inked with an adhesive

Fig. 3D

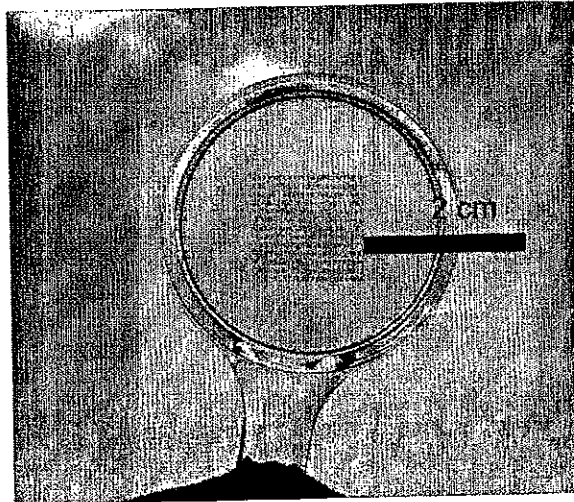


Fig. 3E

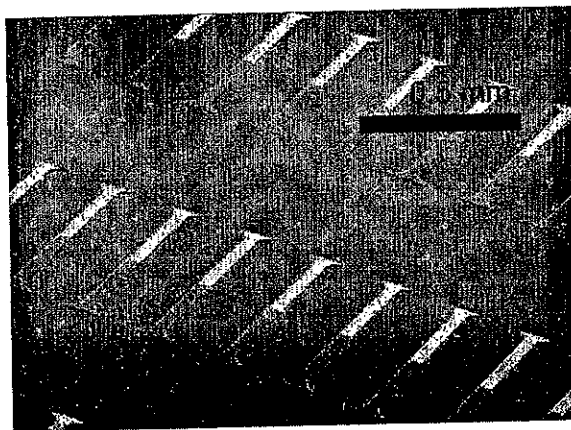


Fig. 3F

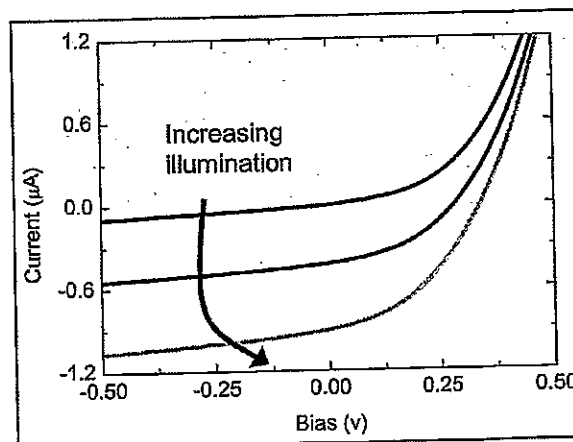


Fig. 4A1

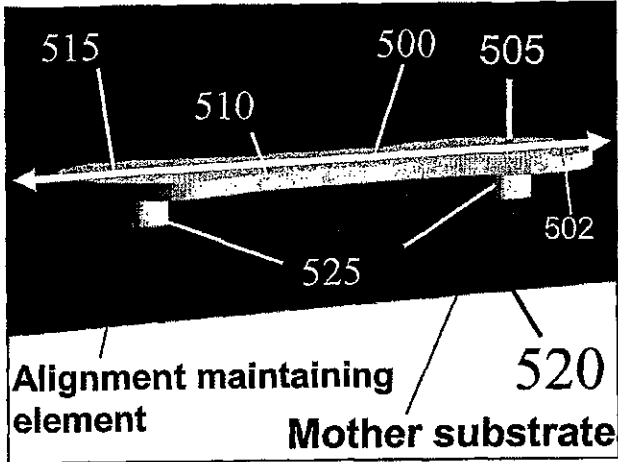


Fig. 4A2

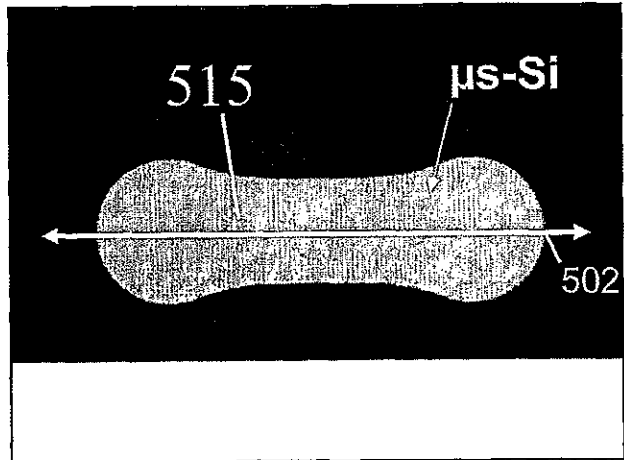


Fig. 4B1

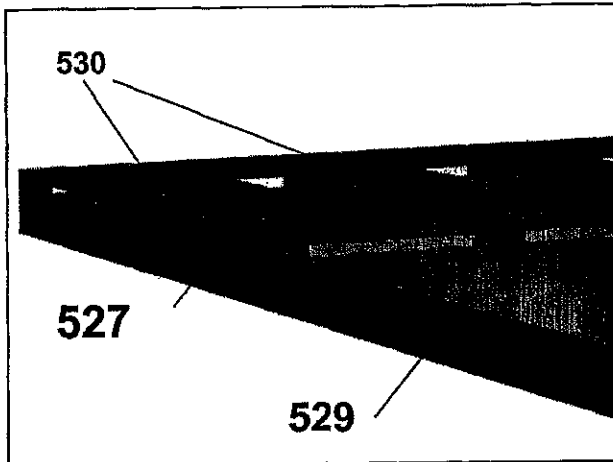


Fig. 4B2

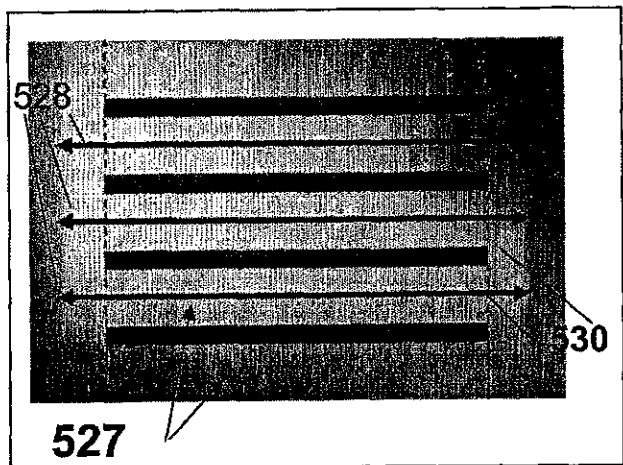


Fig. 5A

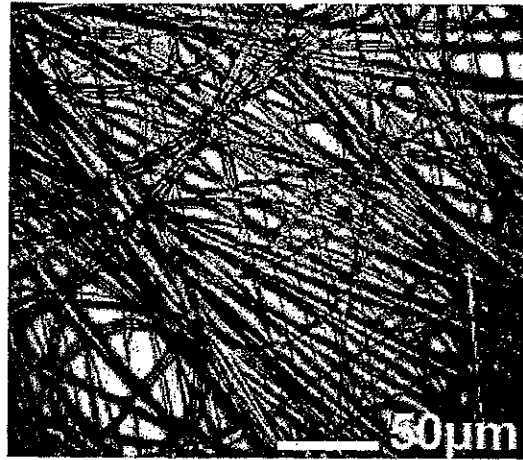


Fig. 5B

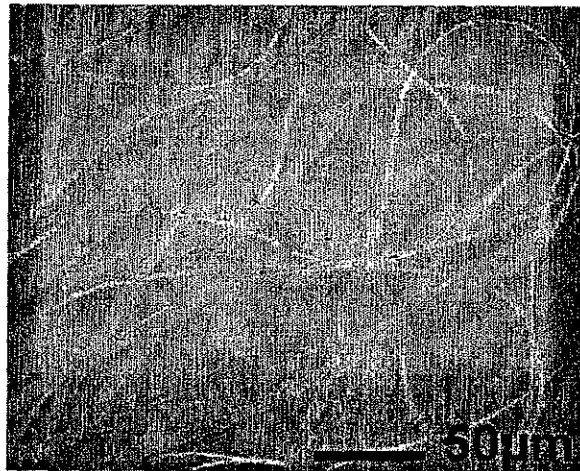


Fig. 5C

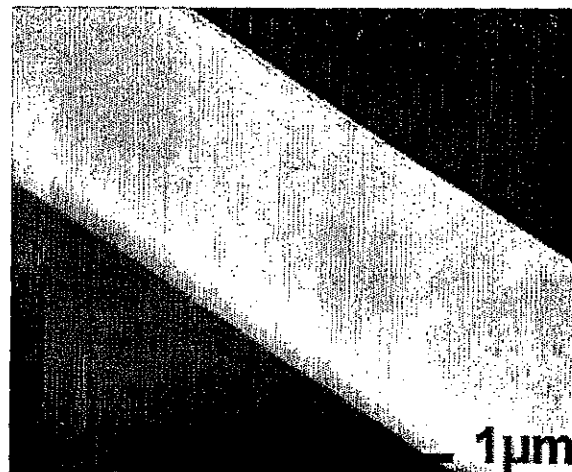
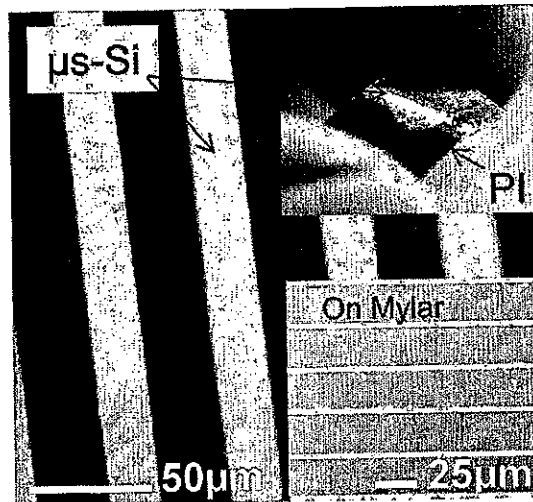


Fig. 6

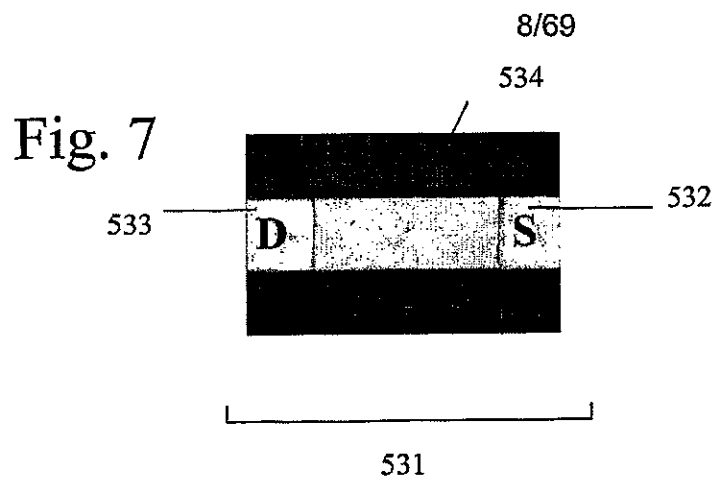


Fig. 8

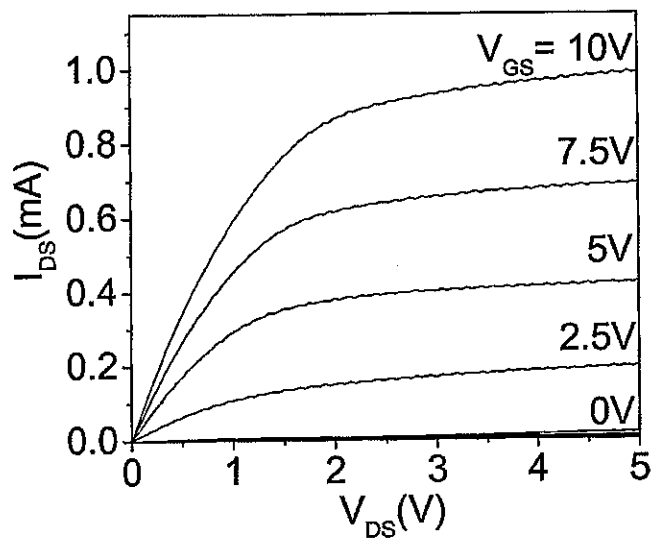


Fig. 9

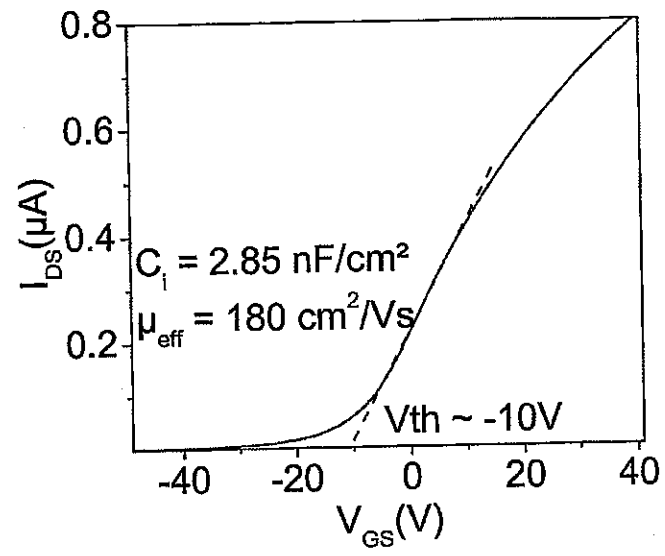


Fig. 10A: Definition of the gate electrodes on a thin sheet of polymer
 (Kapton, Mylar, PET...)
 (Soft lithography techniques can be used)

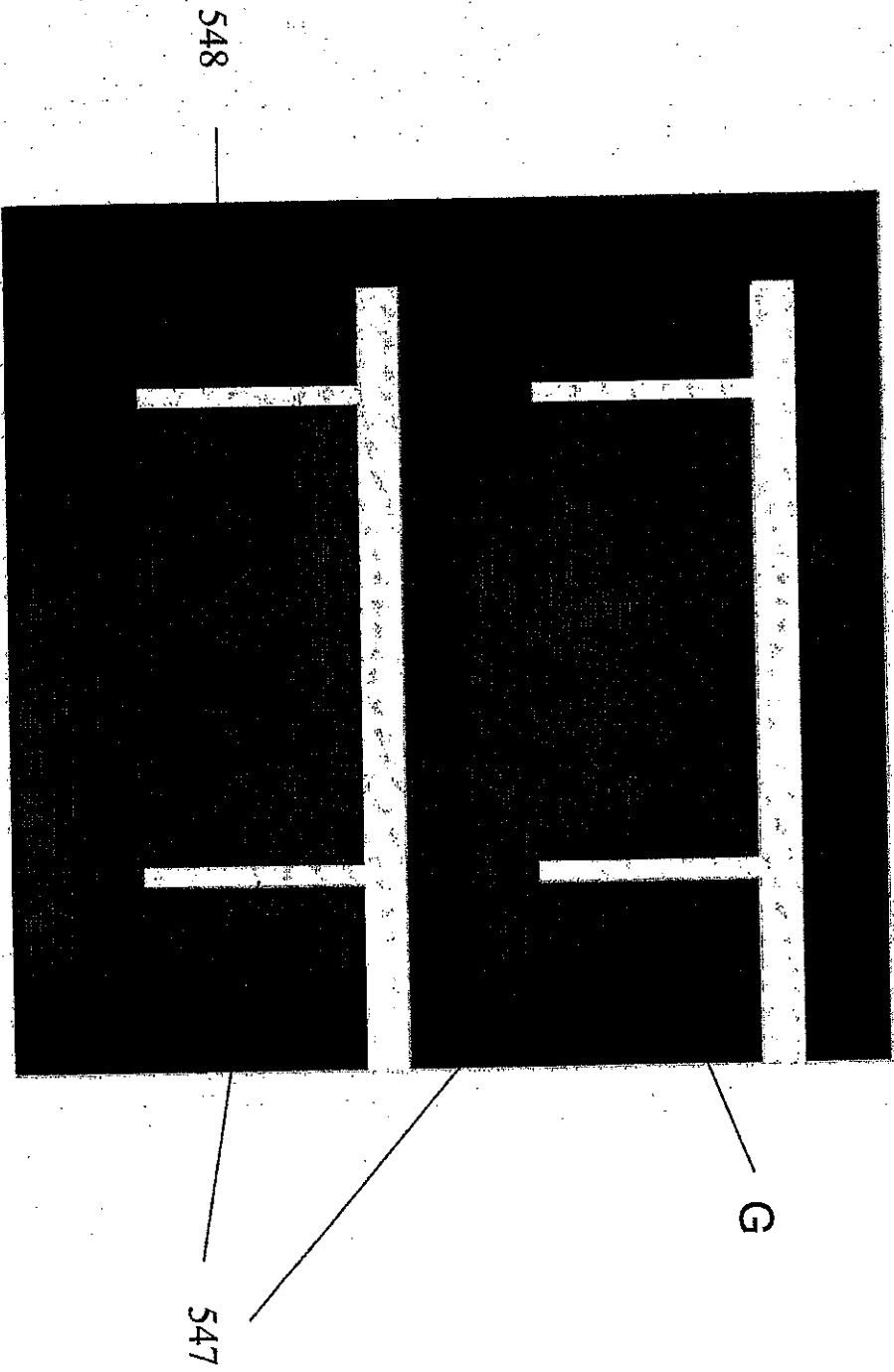


Fig. 10B. Fabrication of composite printable semiconductor elements having an integrated gate dielectric

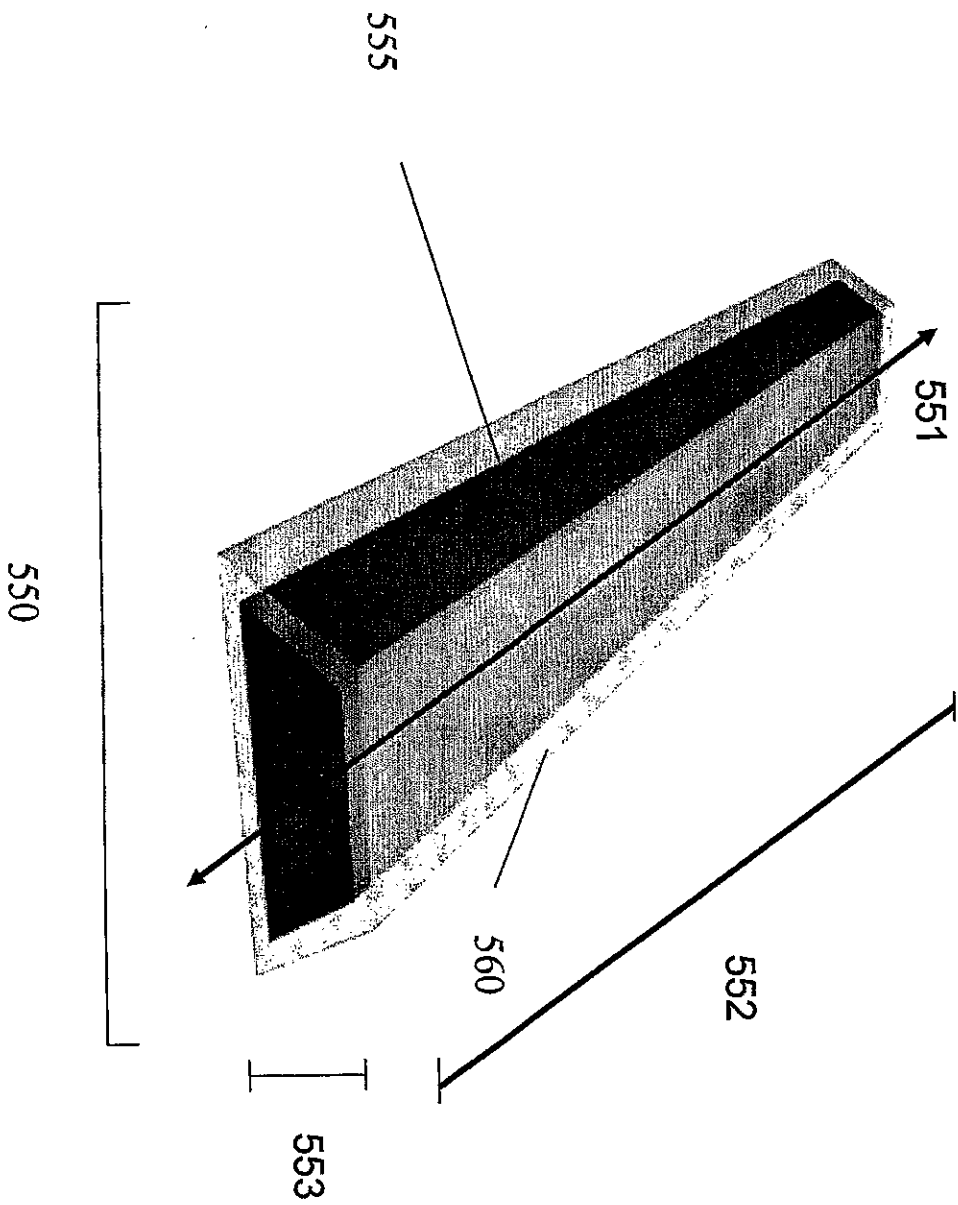
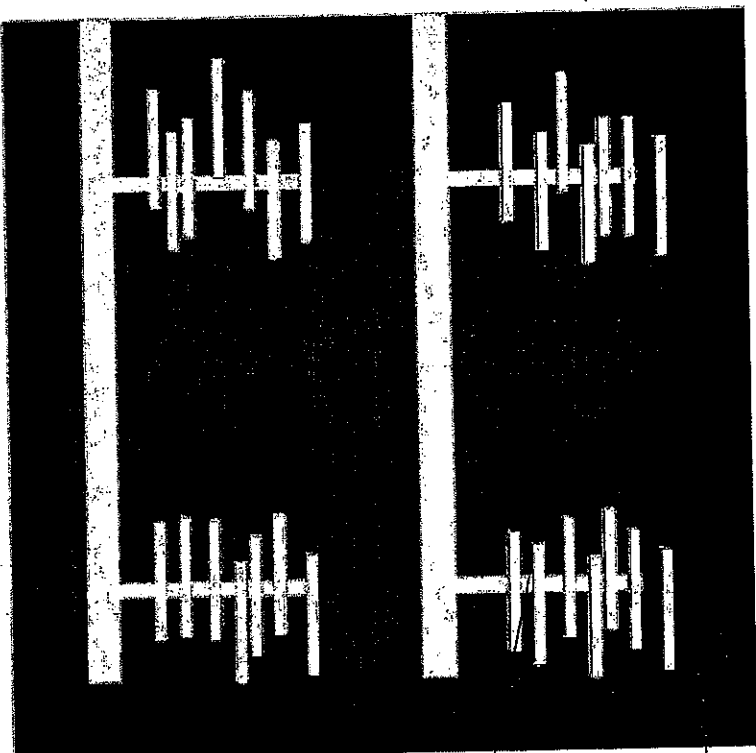


Fig. 10C: Printing of the composite printable semiconductor elements
on a plastic sheet

(Selective dry transfer printing or solution casting)



550

547

548

Fig. 10D: Spin coating of a positive resist

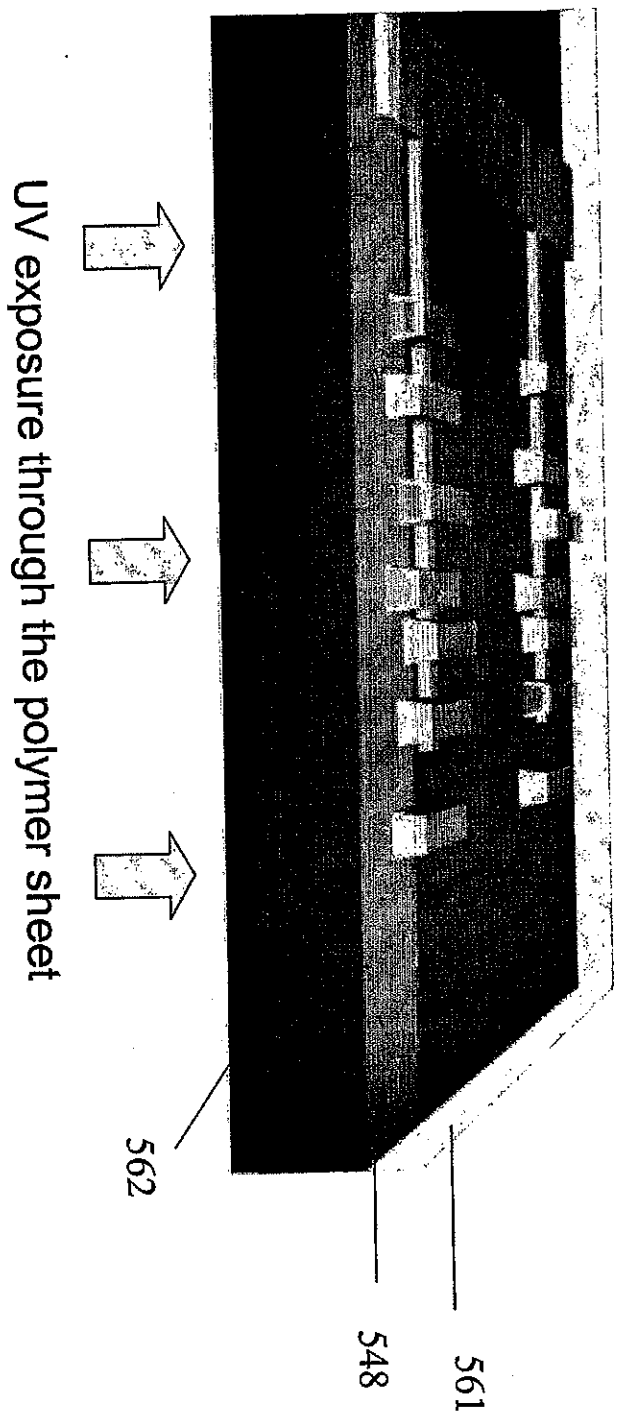


Fig. 10 E: Development of the resist:
the area shadow masked by the gate electrodes are undeveloped

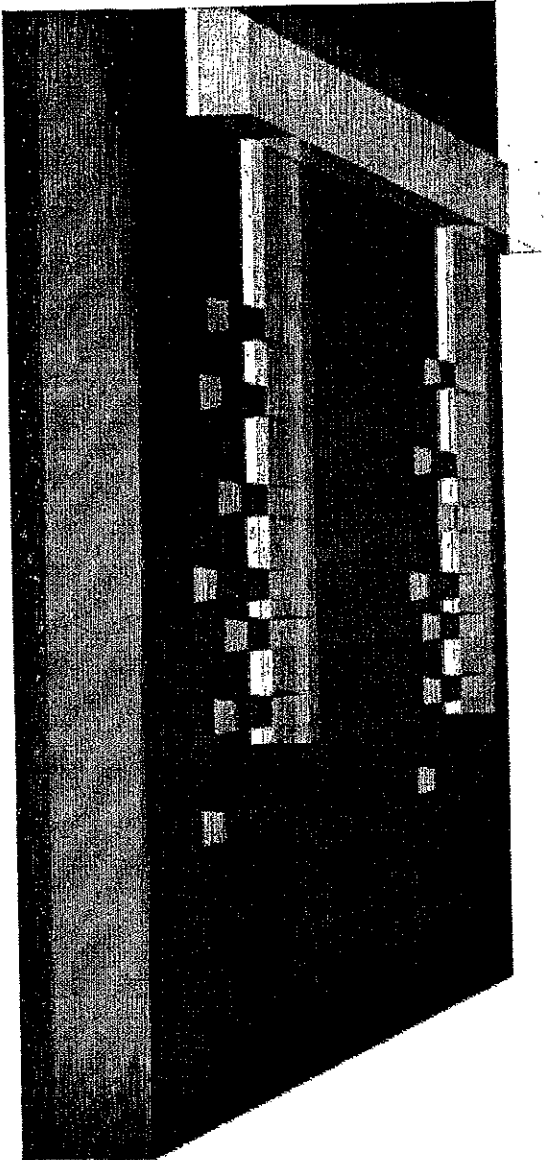


Fig. 10F: Source and drain contact opening
(Dry of wet etching of integrated SiO_2 dielectric)

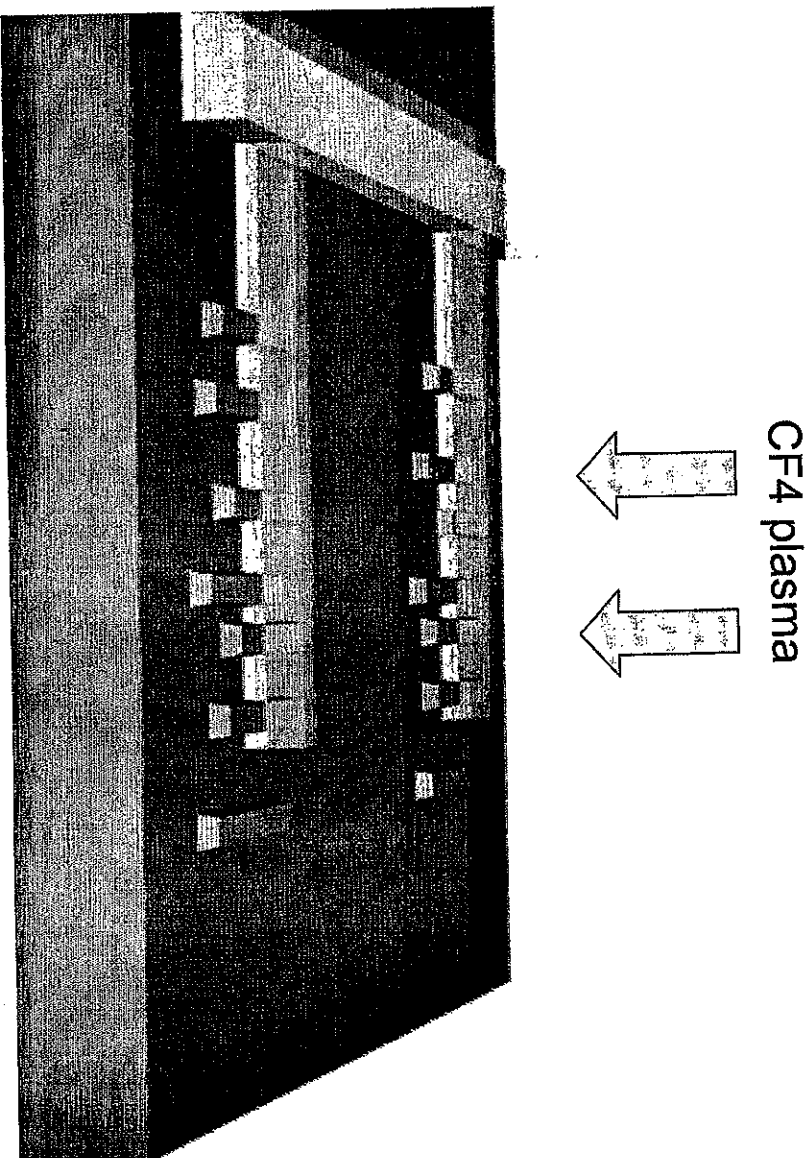
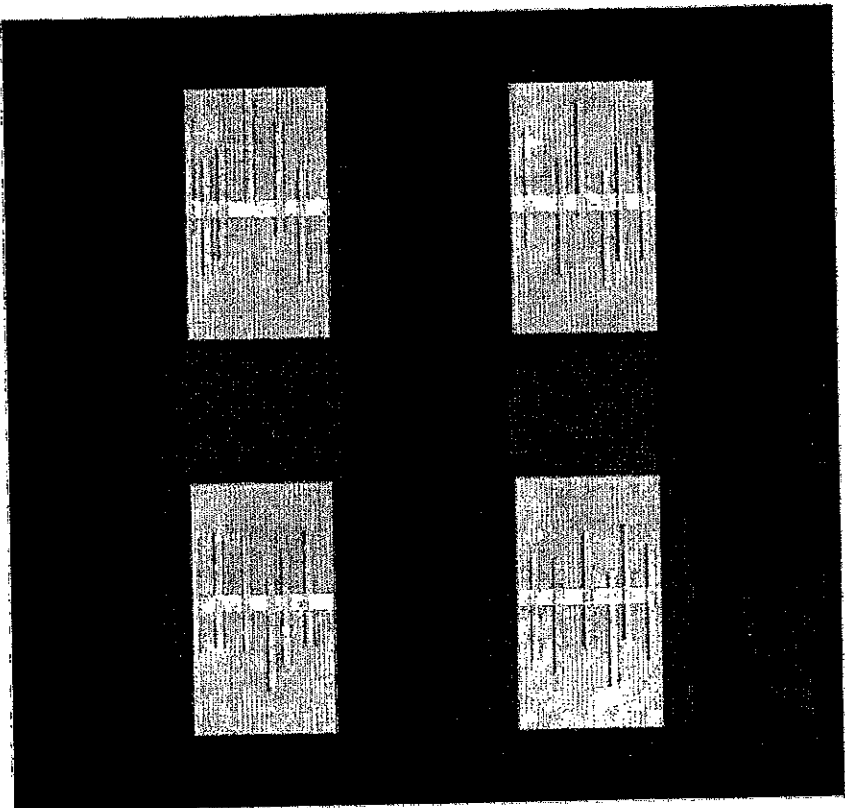


Fig. 10G: Definition of the source and drain electrodes
by shadow masking evaporation



REM: The alignment does not have to be very precise,
the channel will be defined in the next step

Figure 10H: Definition of the channel by lifting off the positive resist with acetone

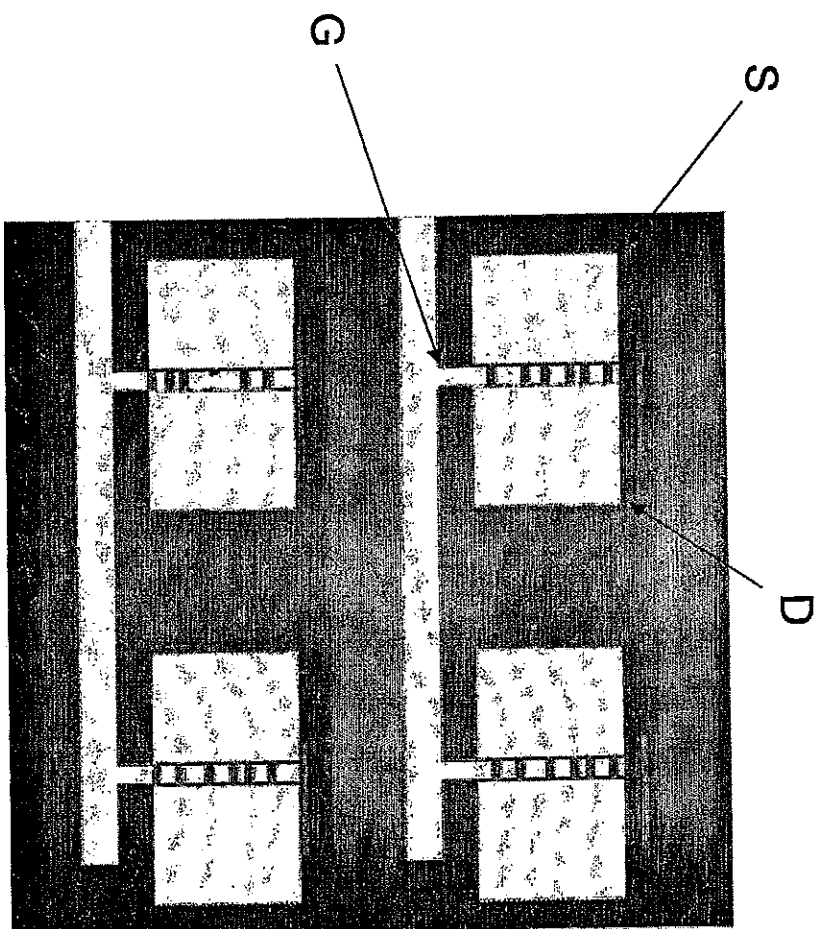
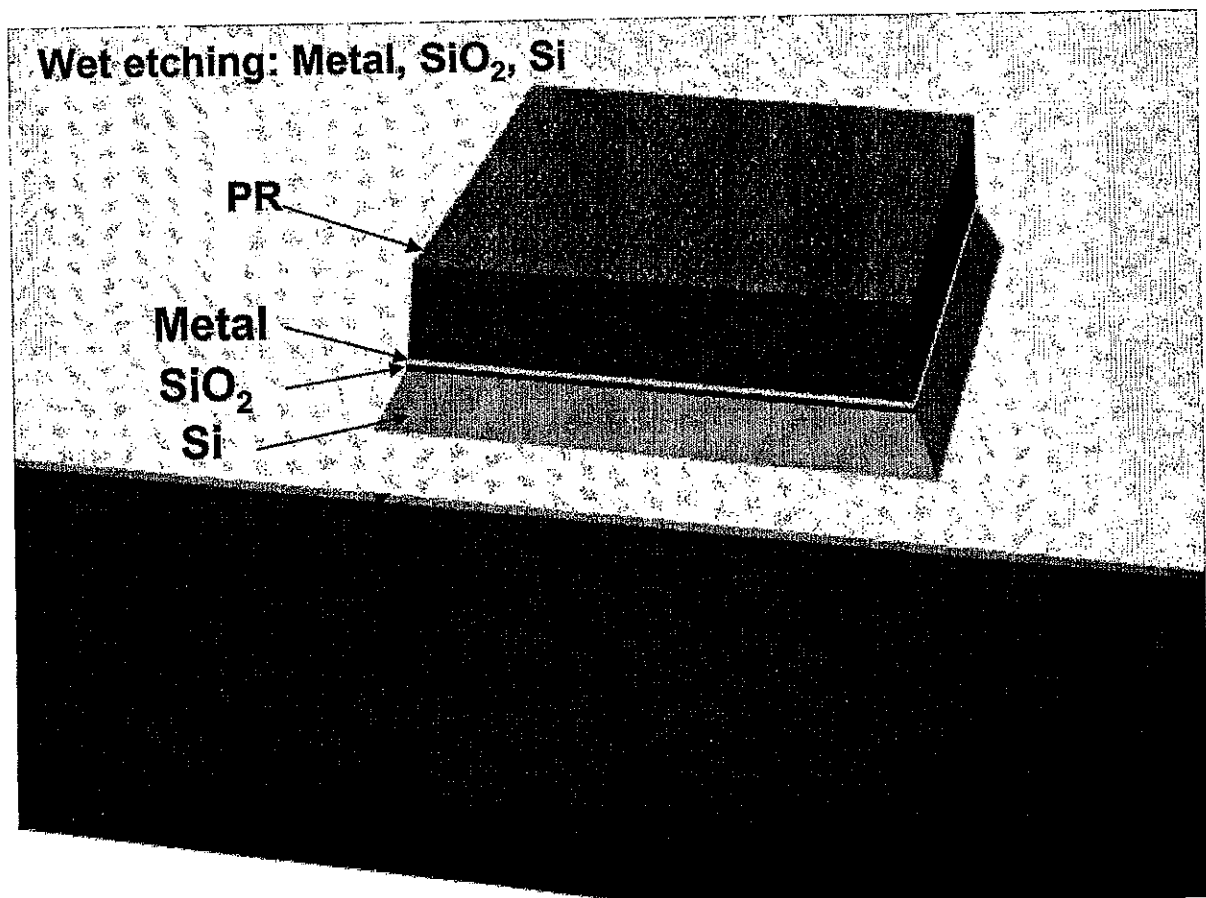


Fig. 11A



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Fig. 11B: Wet etching: Metal

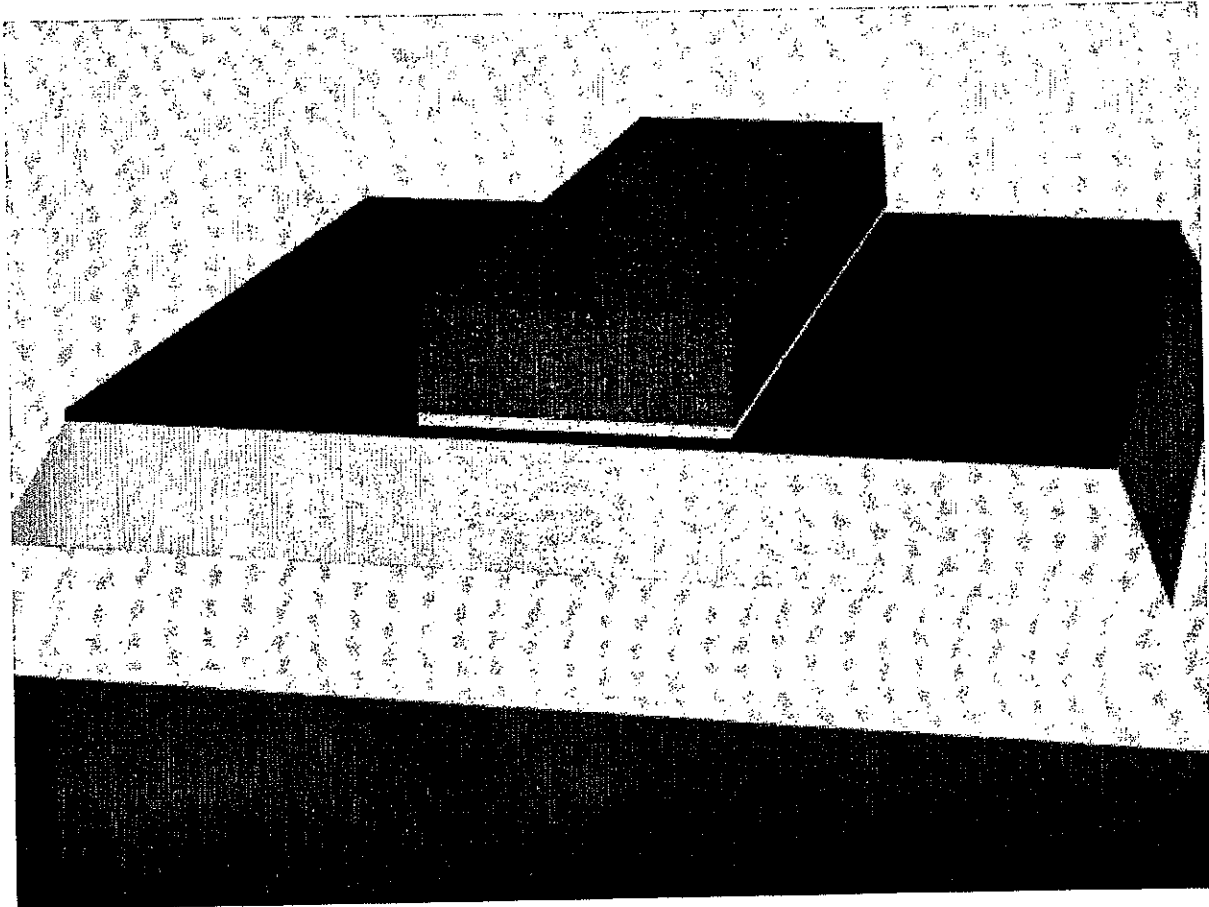
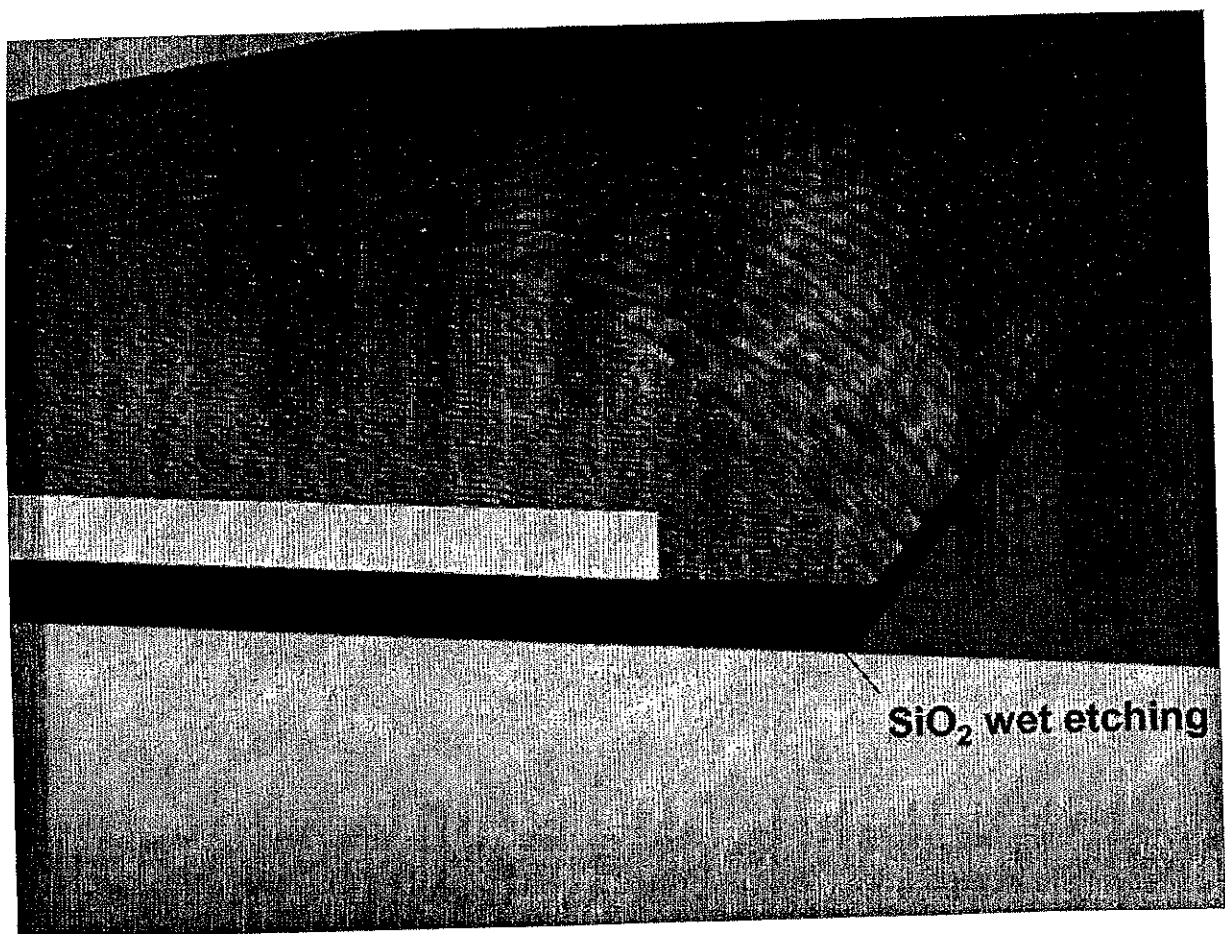
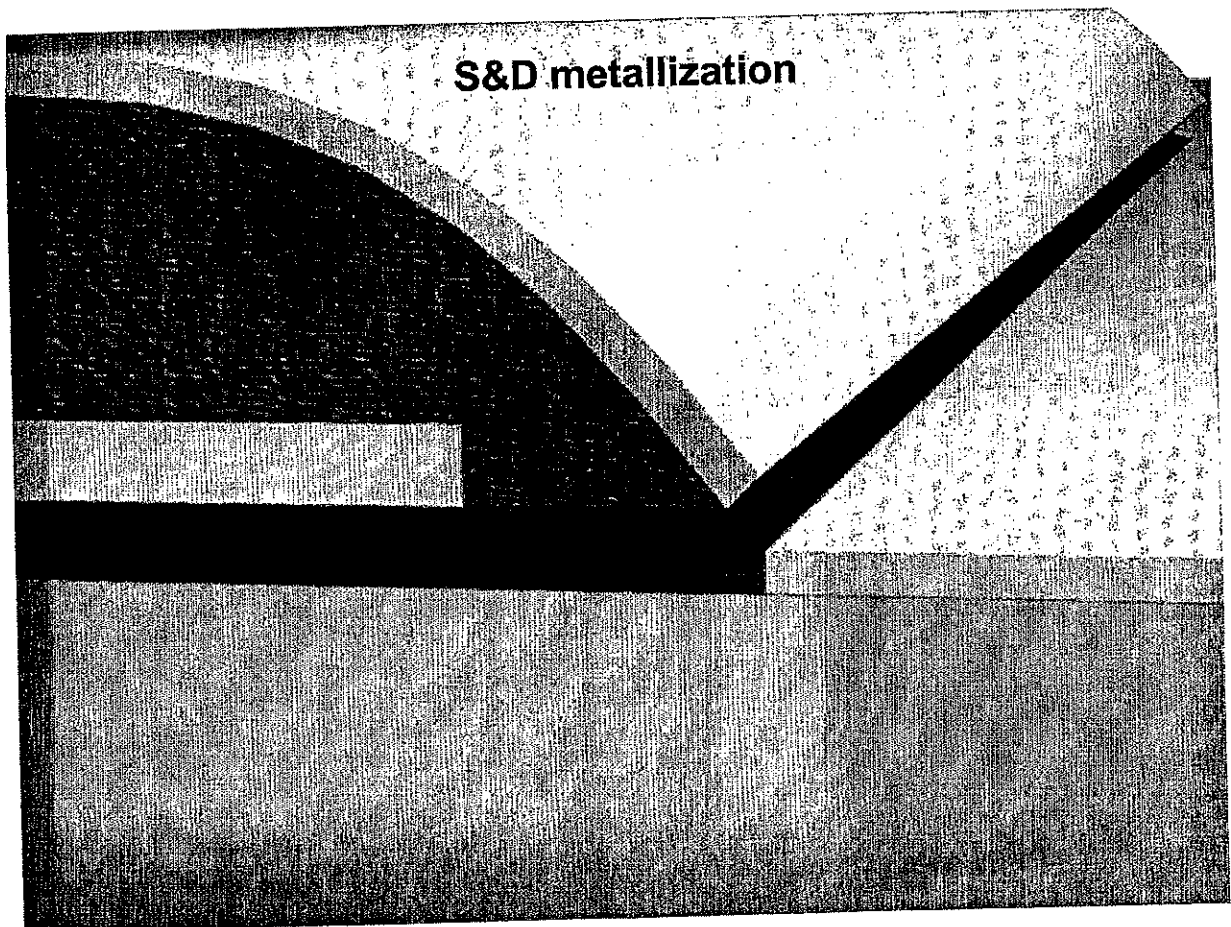


Fig. 11C

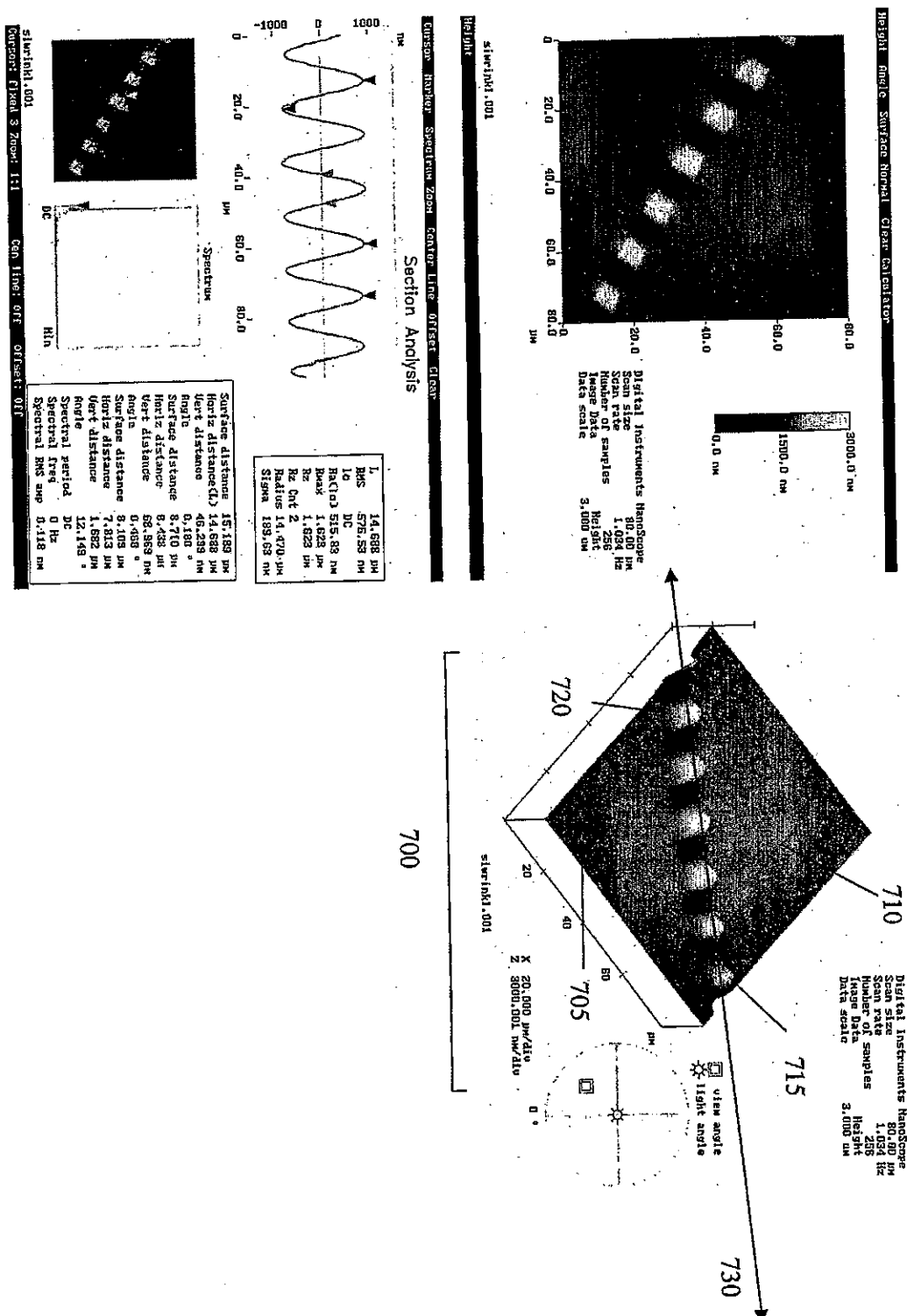


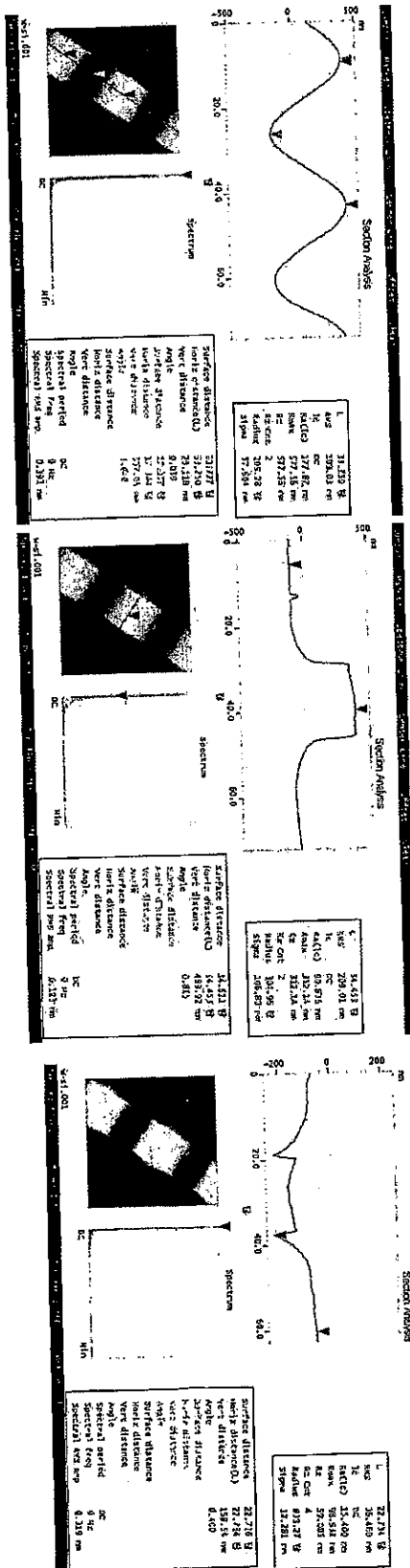
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Fig. 11D



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[illegible]

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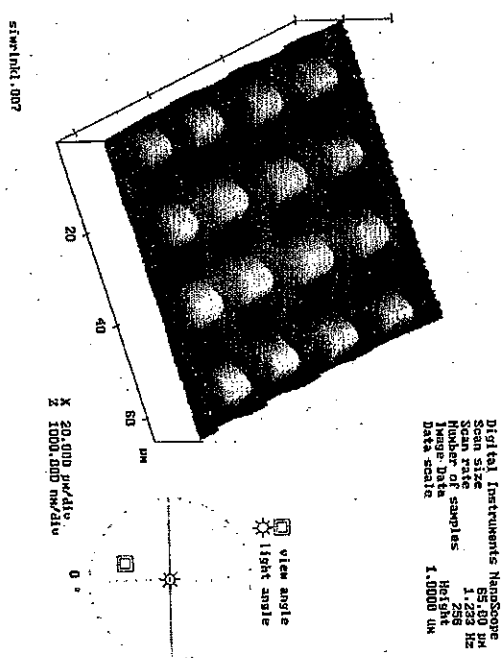


Fig. 15: Stretchable semiconductor element

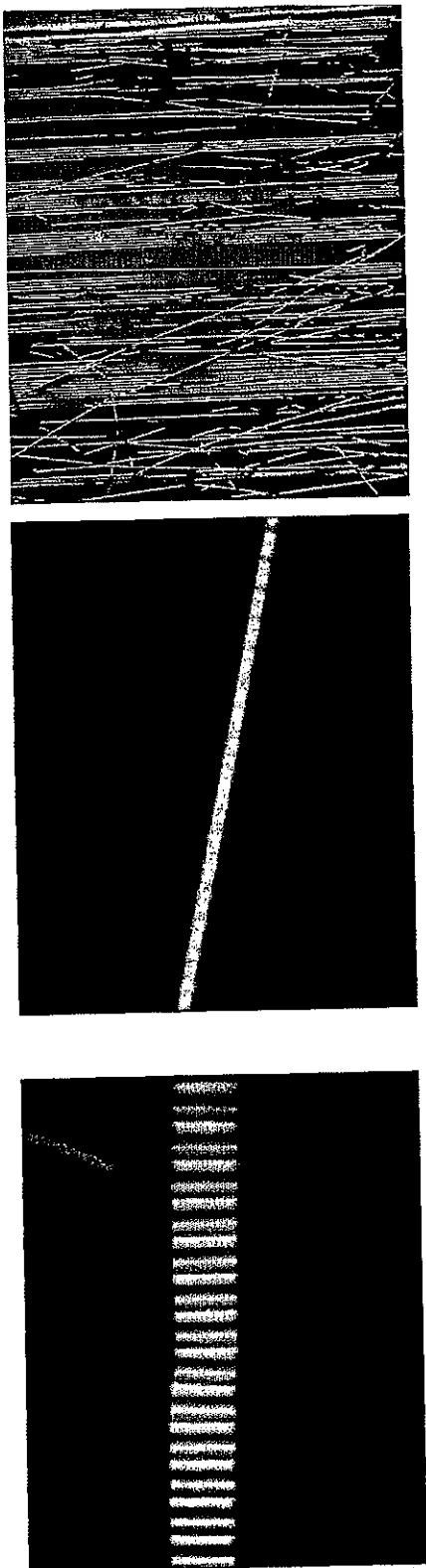


Fig. 16: Stretchable semiconductor element

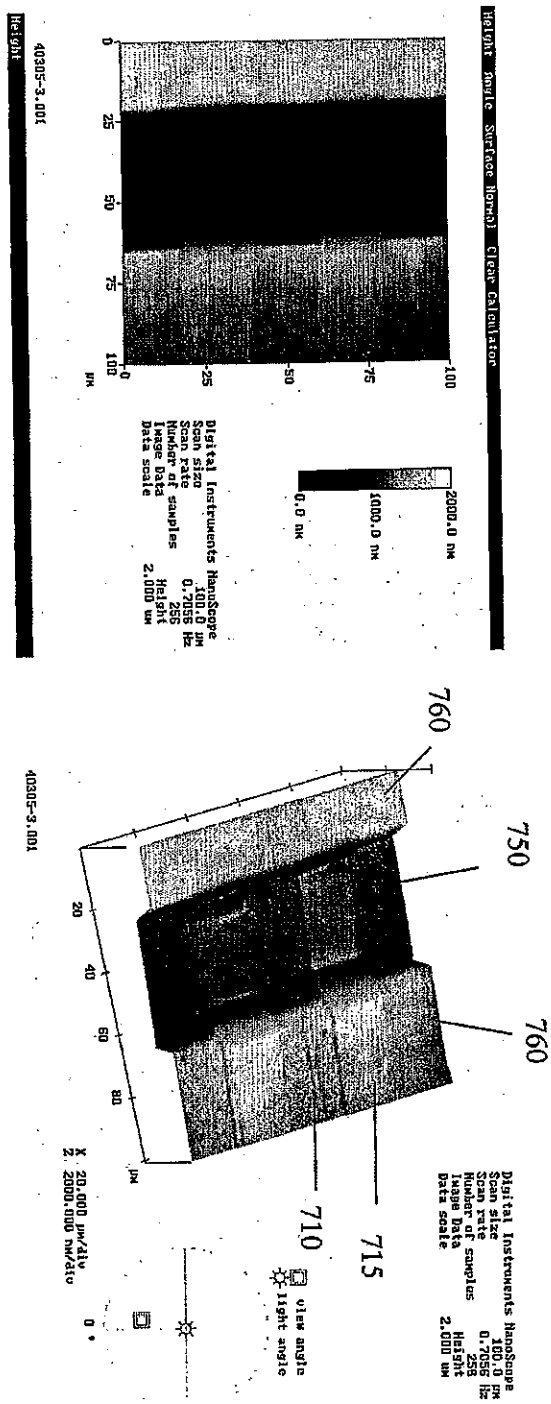


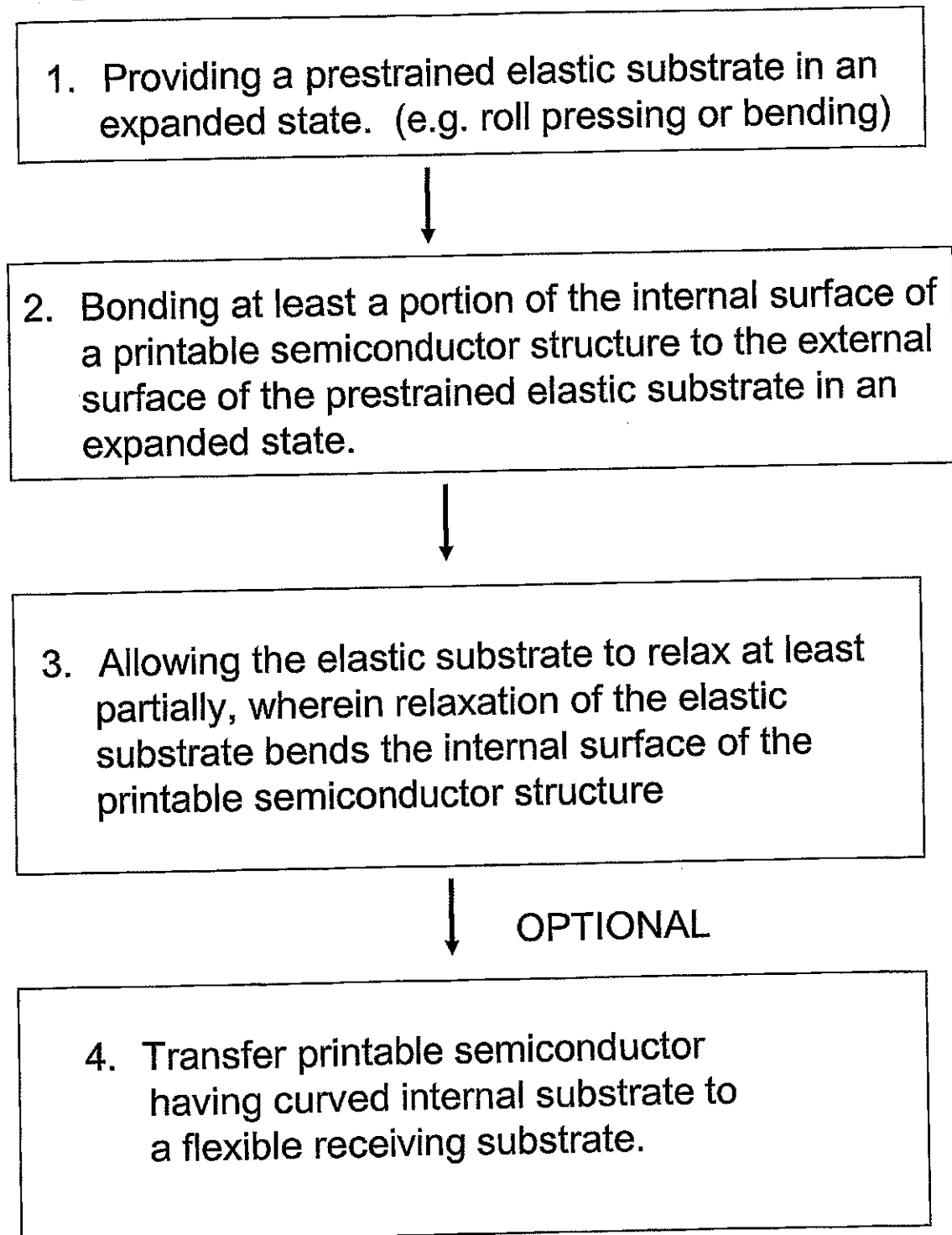
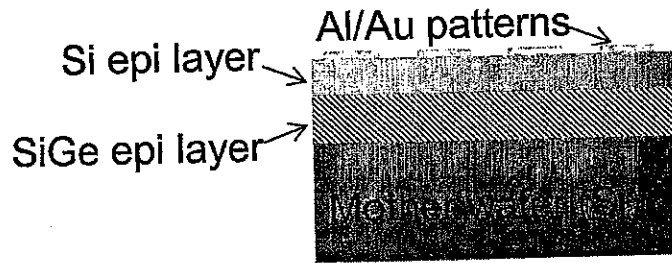
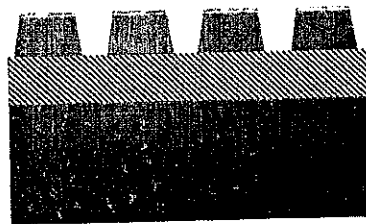
Fig. 17

Fig. 18A



i) μ s-Si shape definition



ii) μ s-Si wet etching



iii) Si-Ge selective wet etching

Fig. 18B

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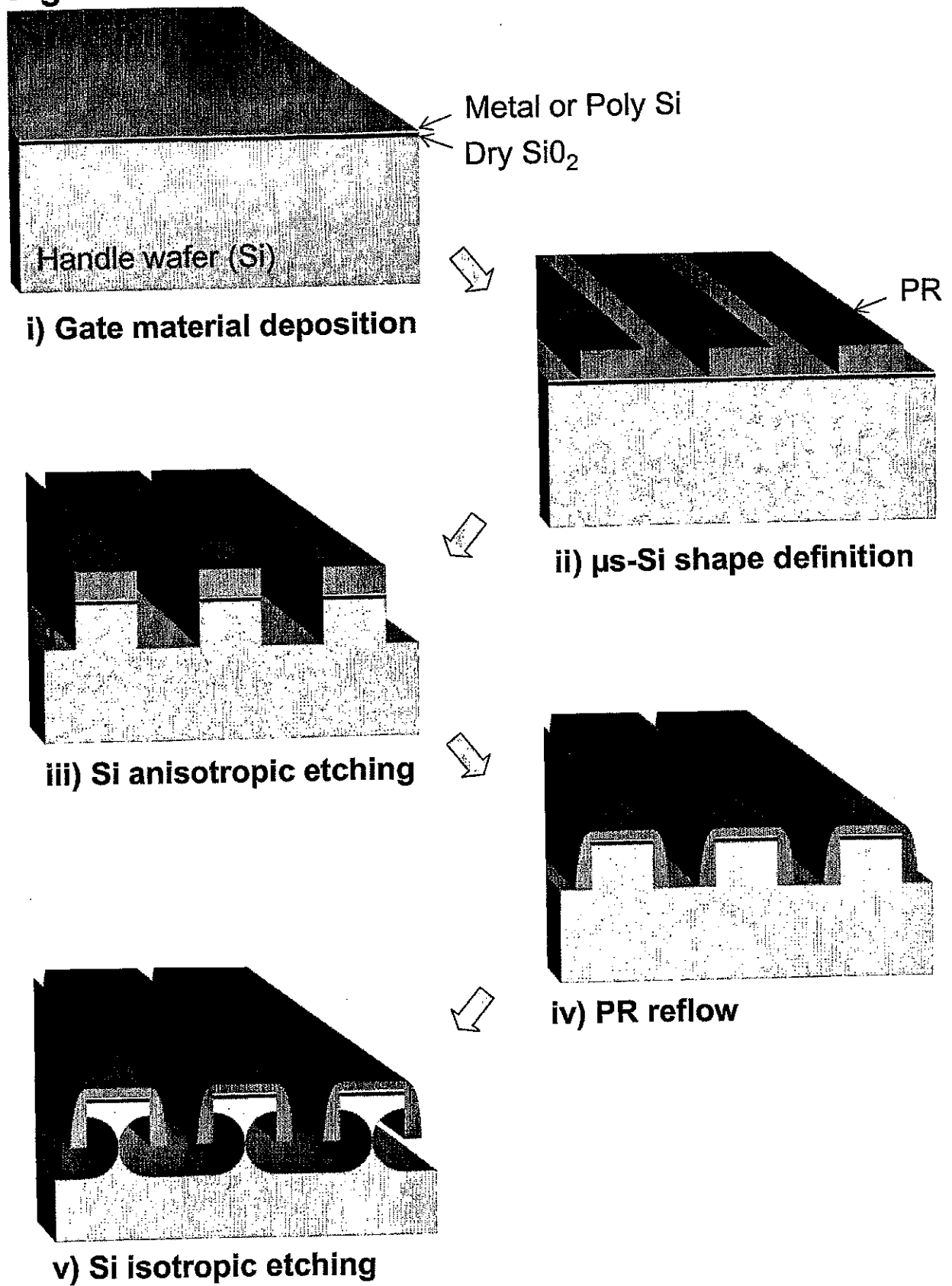


Fig. 18C

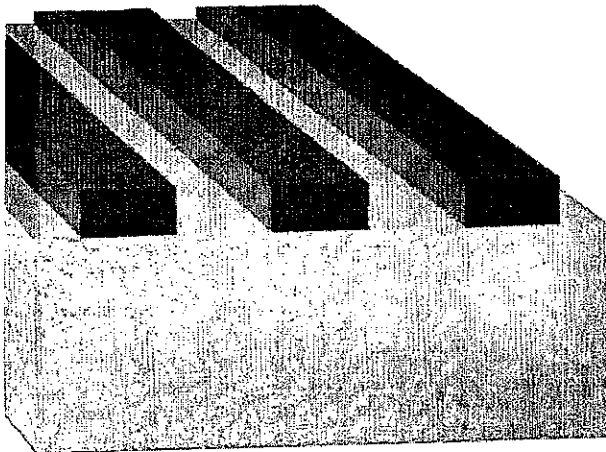
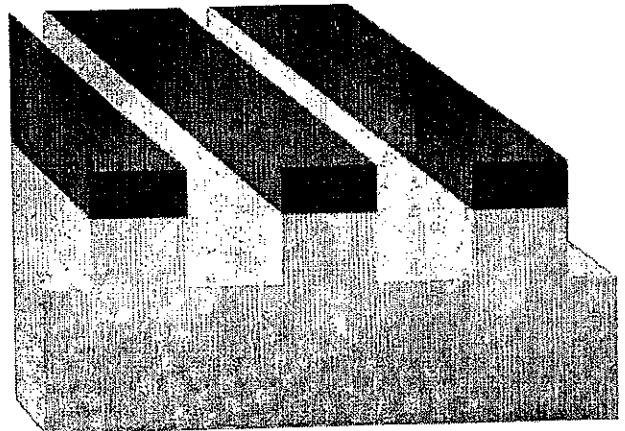
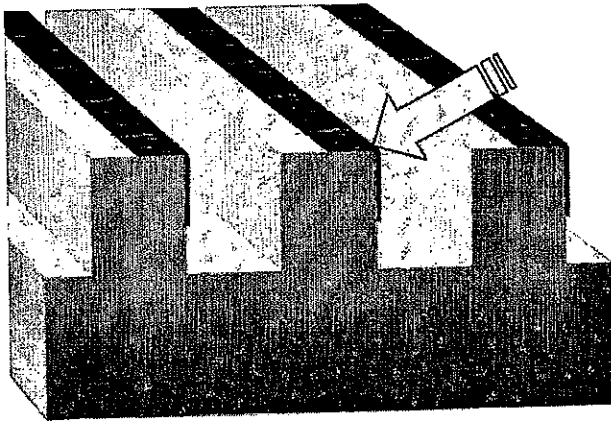
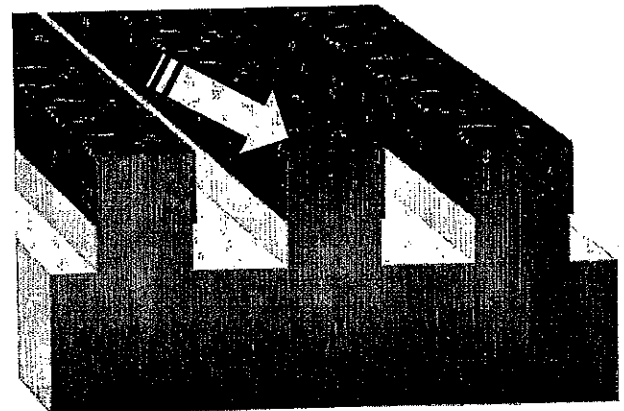
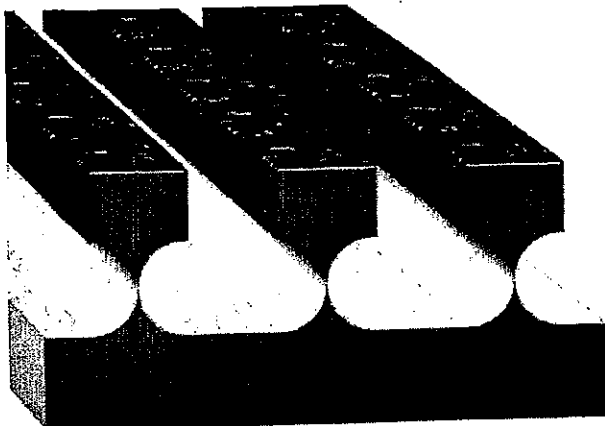
**i) μ s-Si shape definition****ii) anisotropic etching****iii) tilted evaporation****iv) tilted evaporation****v) isotropic etching**

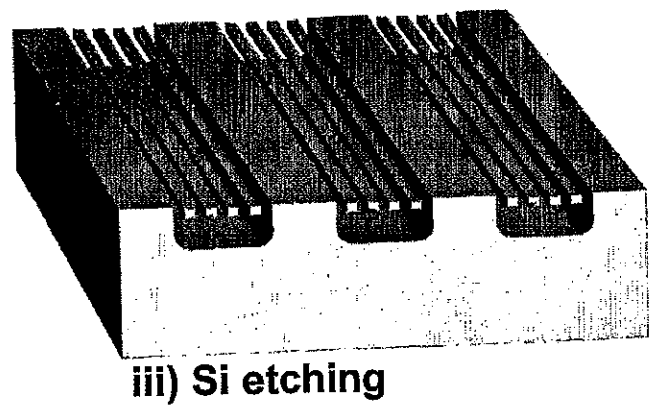
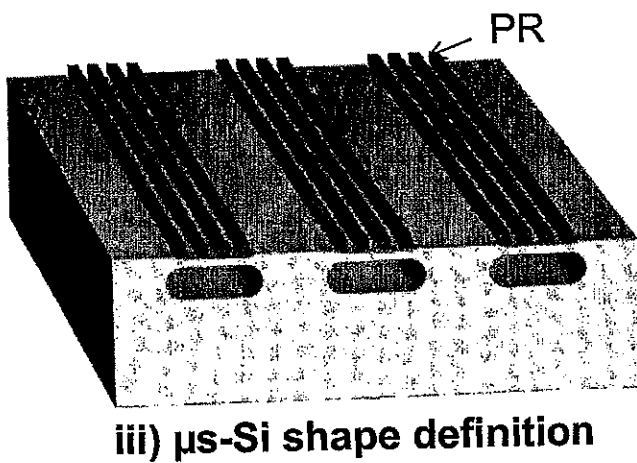
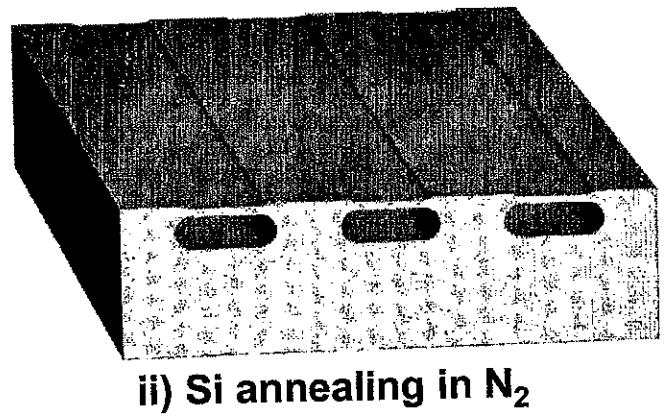
Fig. 18D

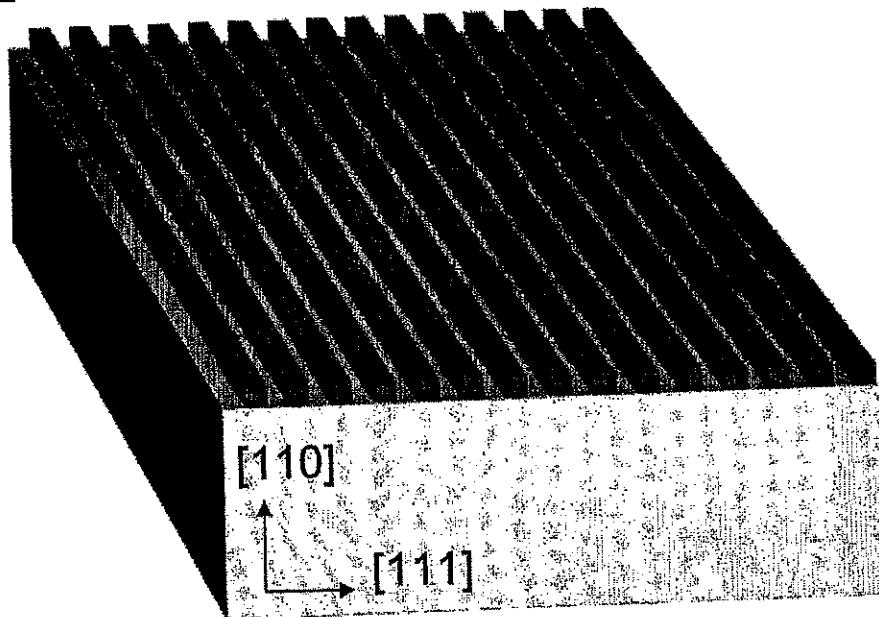
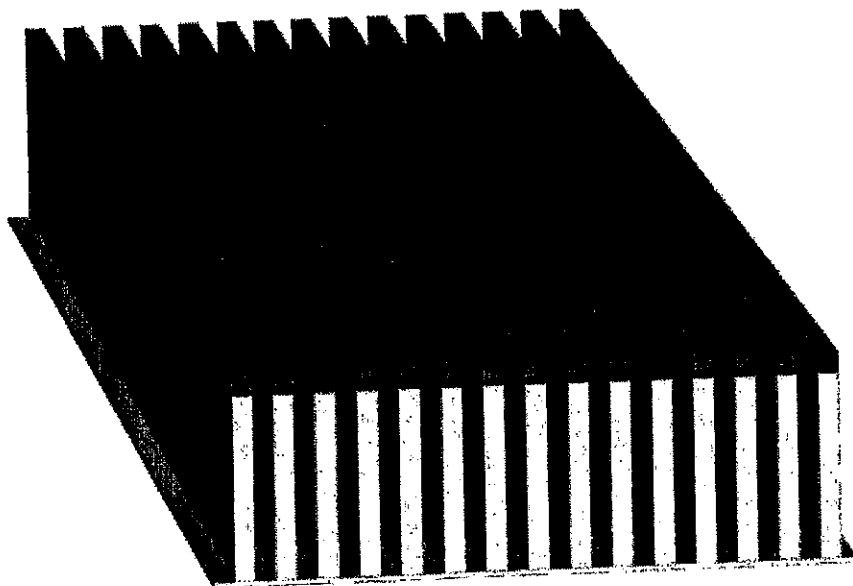
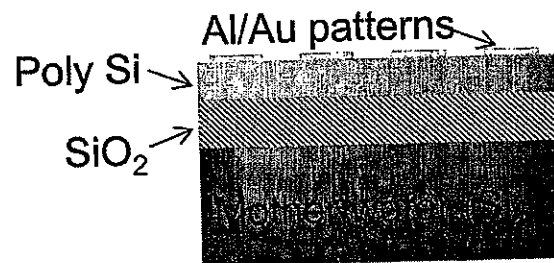
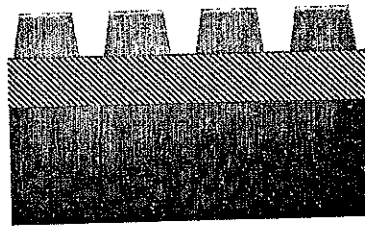
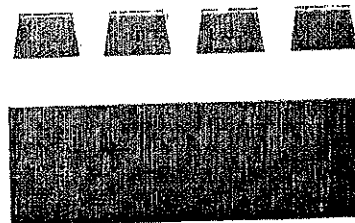
Fig. 18E**i) μ s-Si shape definition****ii) anisotropic wet chemical etching**

Fig. 18F

i) μ s-Si shape definition



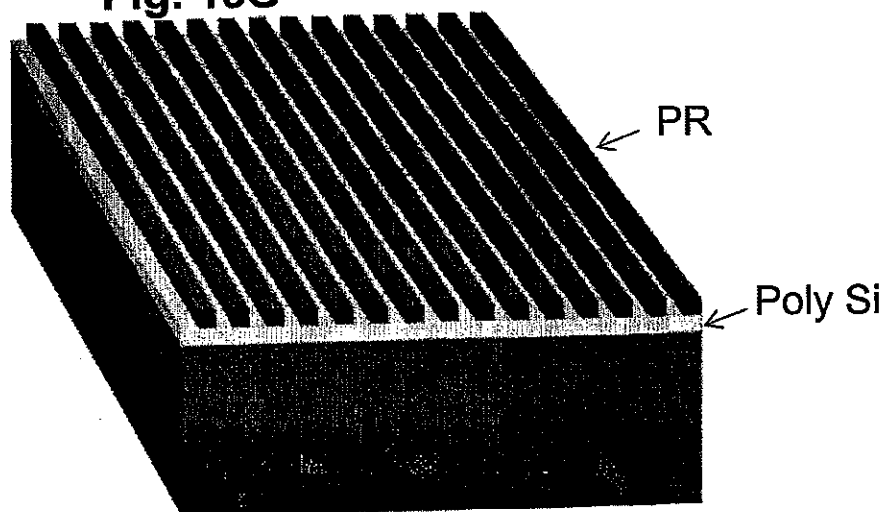
ii) μ s-Si wet etching



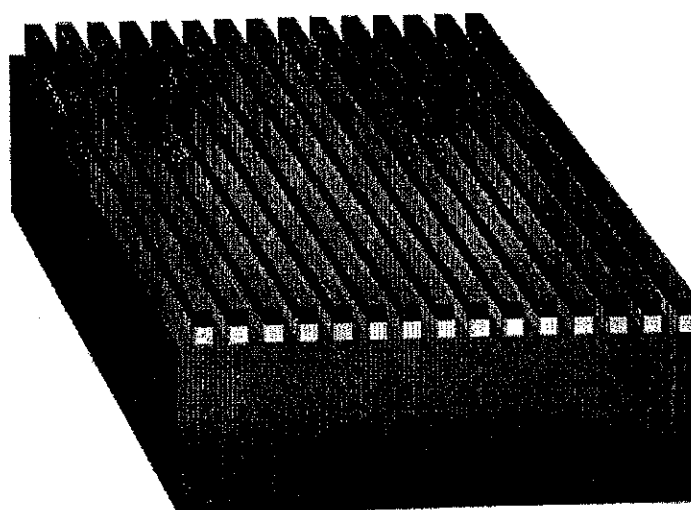
iii) Liftoff: SiO₂ selective wet etching

Fig. 18G

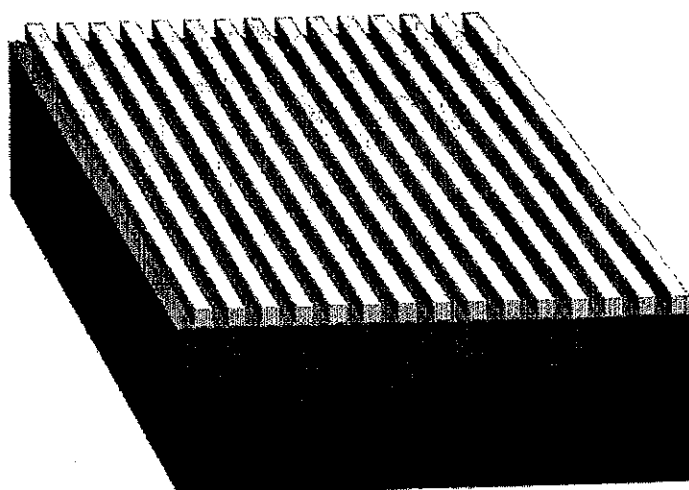
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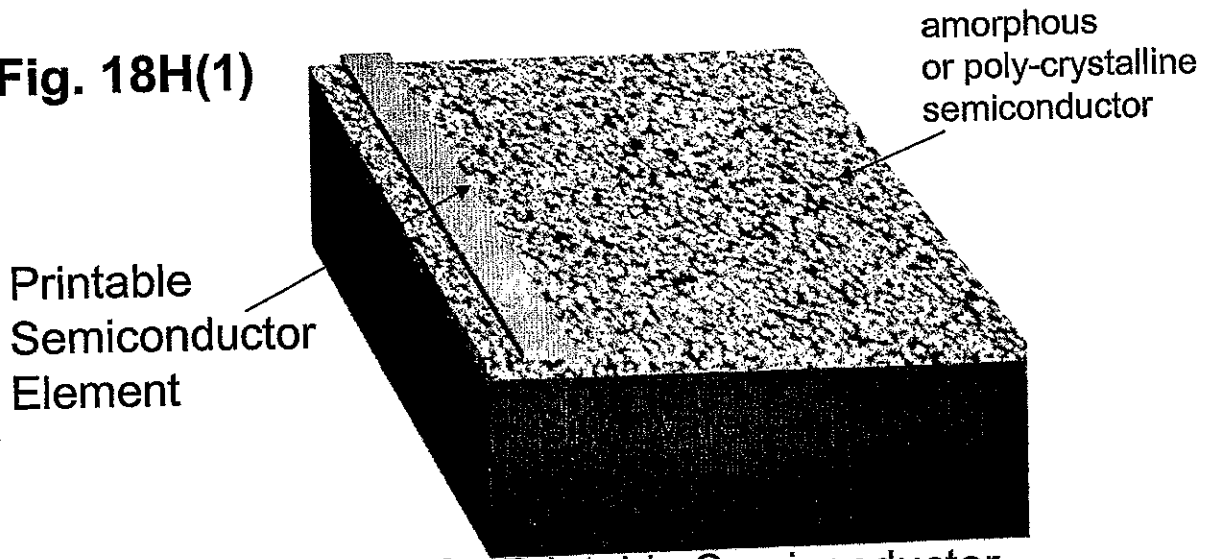
i) μ s-pSi shape definition



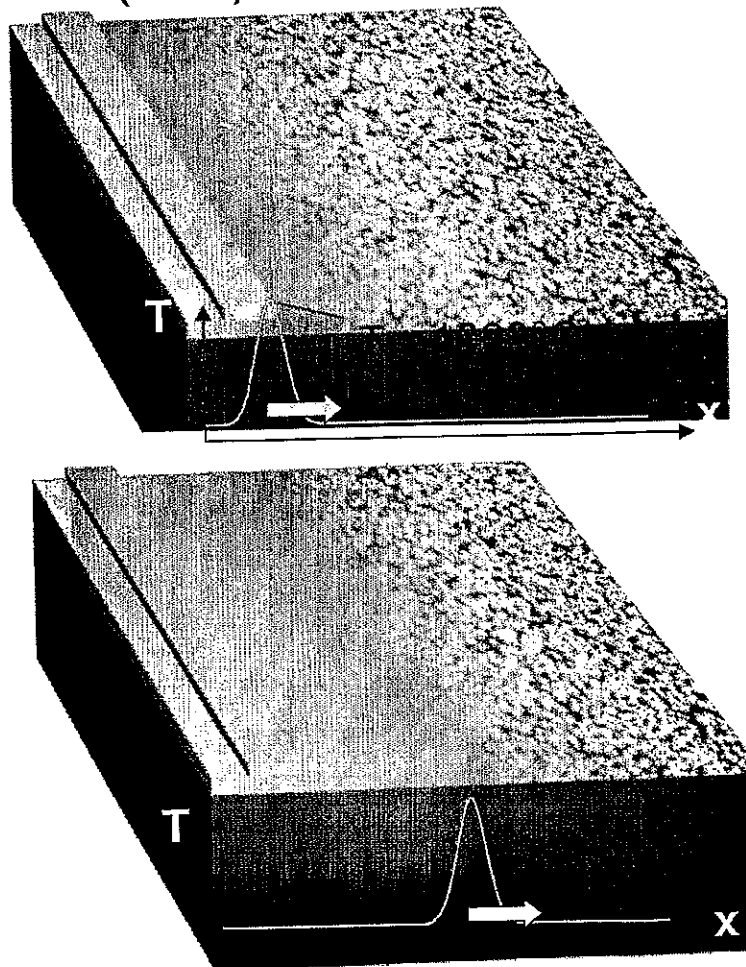
ii) μ s-pSi wet etching



iii) Liftoff: SiO_2 selective wet etching

Fig. 18H(1)

Transfer of a Printable Semiconductor Element(seed)

Fig. 18H(2)

Annealing of the thin film

Fig. 18I

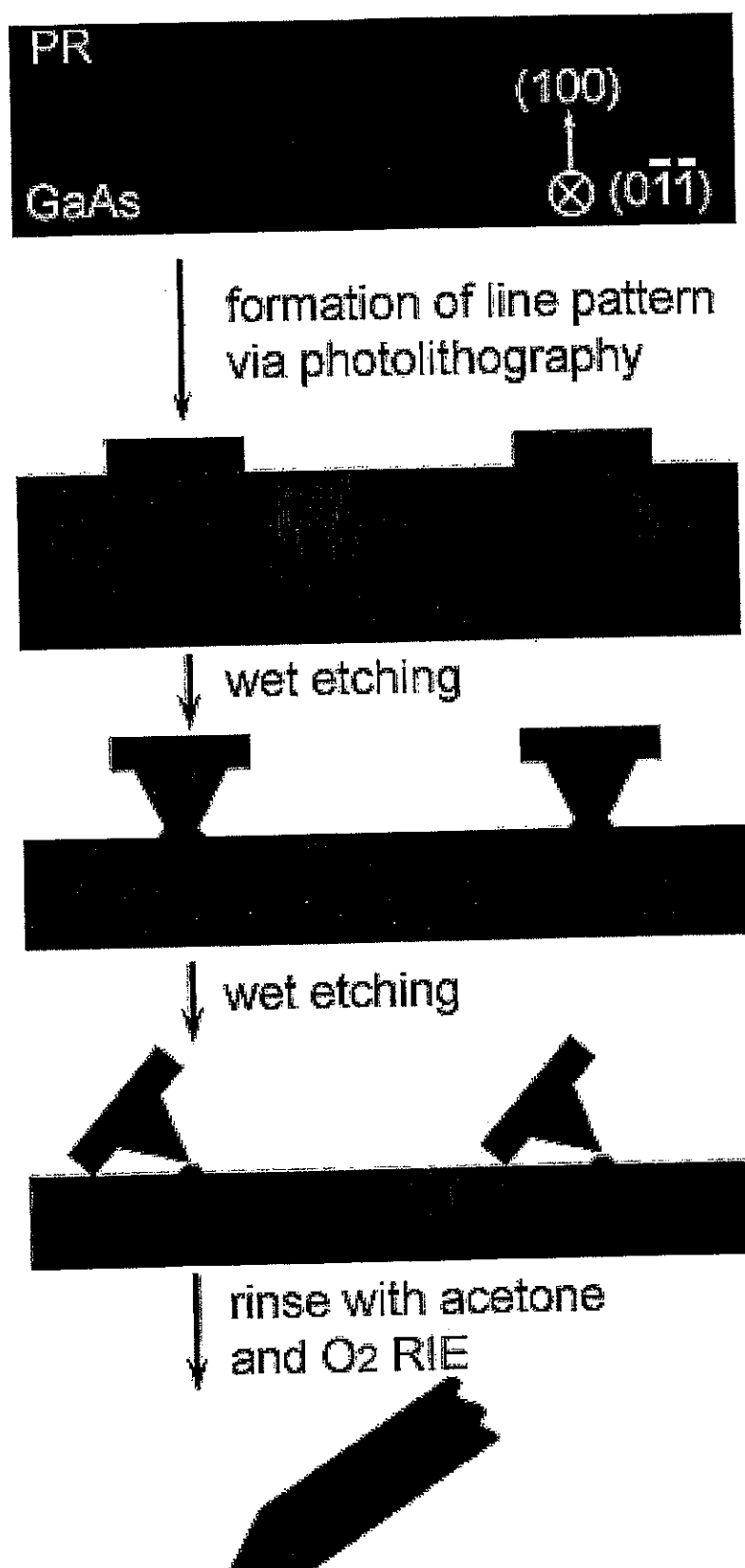


Fig. 18J: Bulk (110) Si to μ S-Si

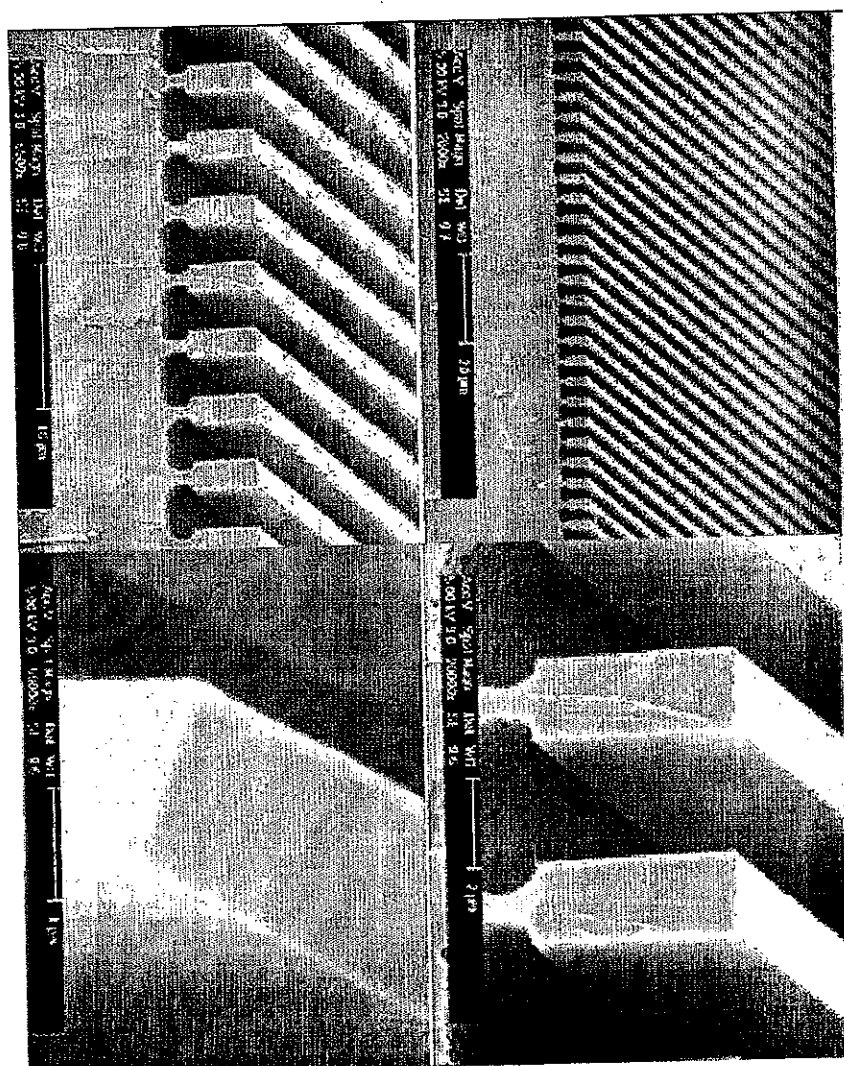
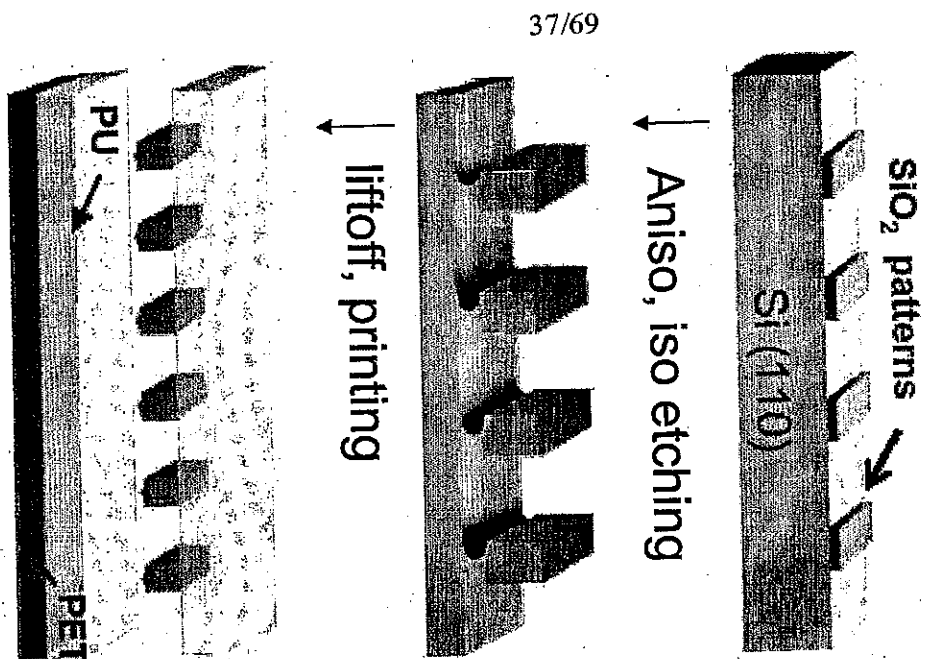
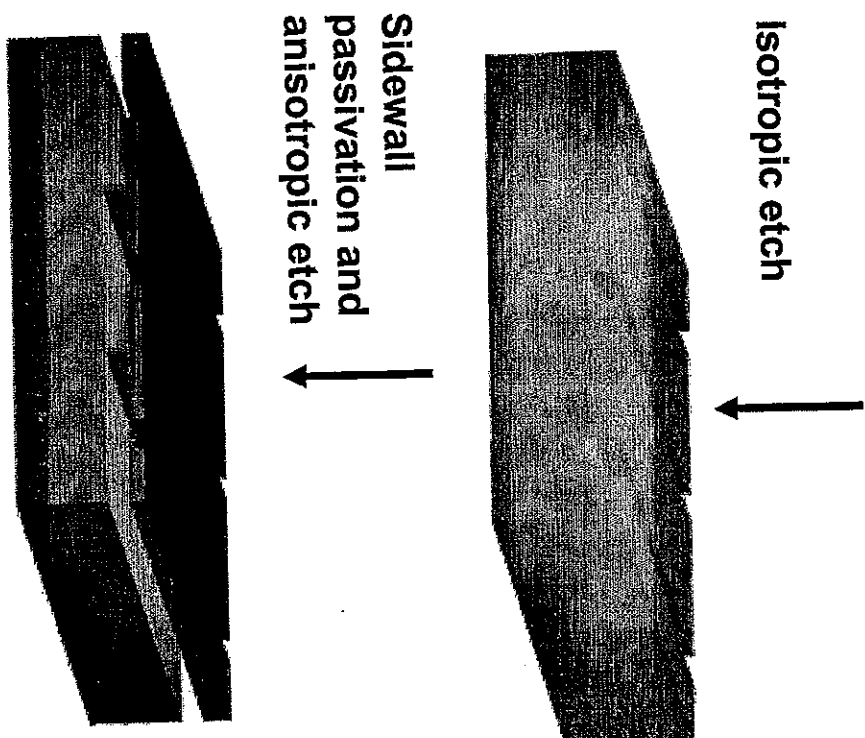


Fig. 18K: Bulk (111) Si to μ S-Si



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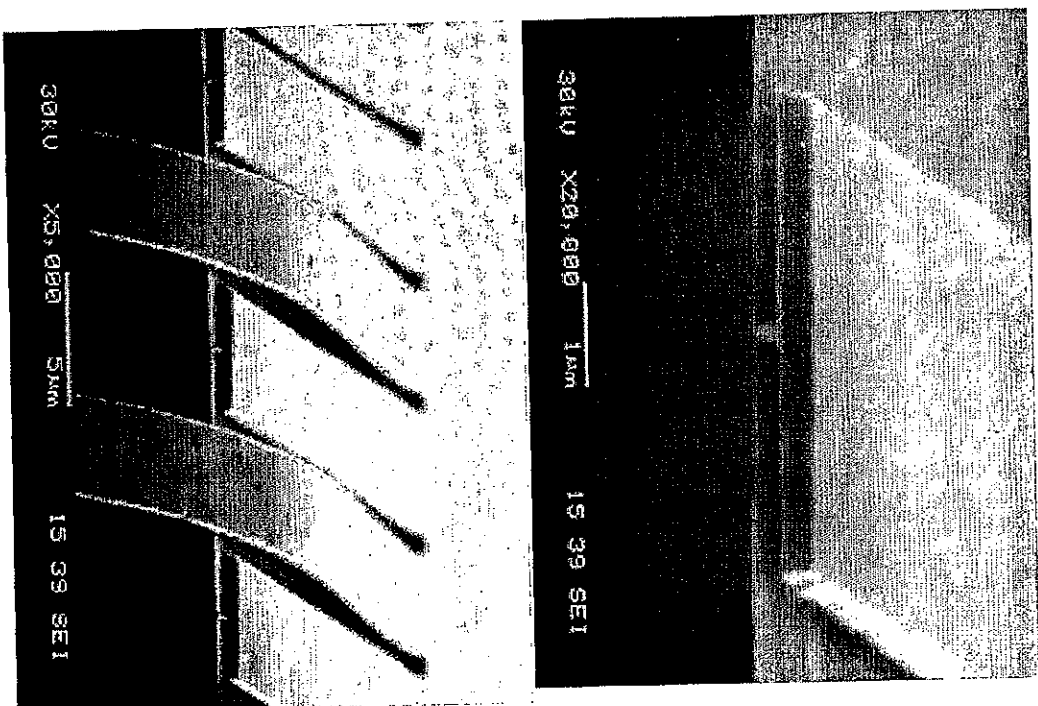
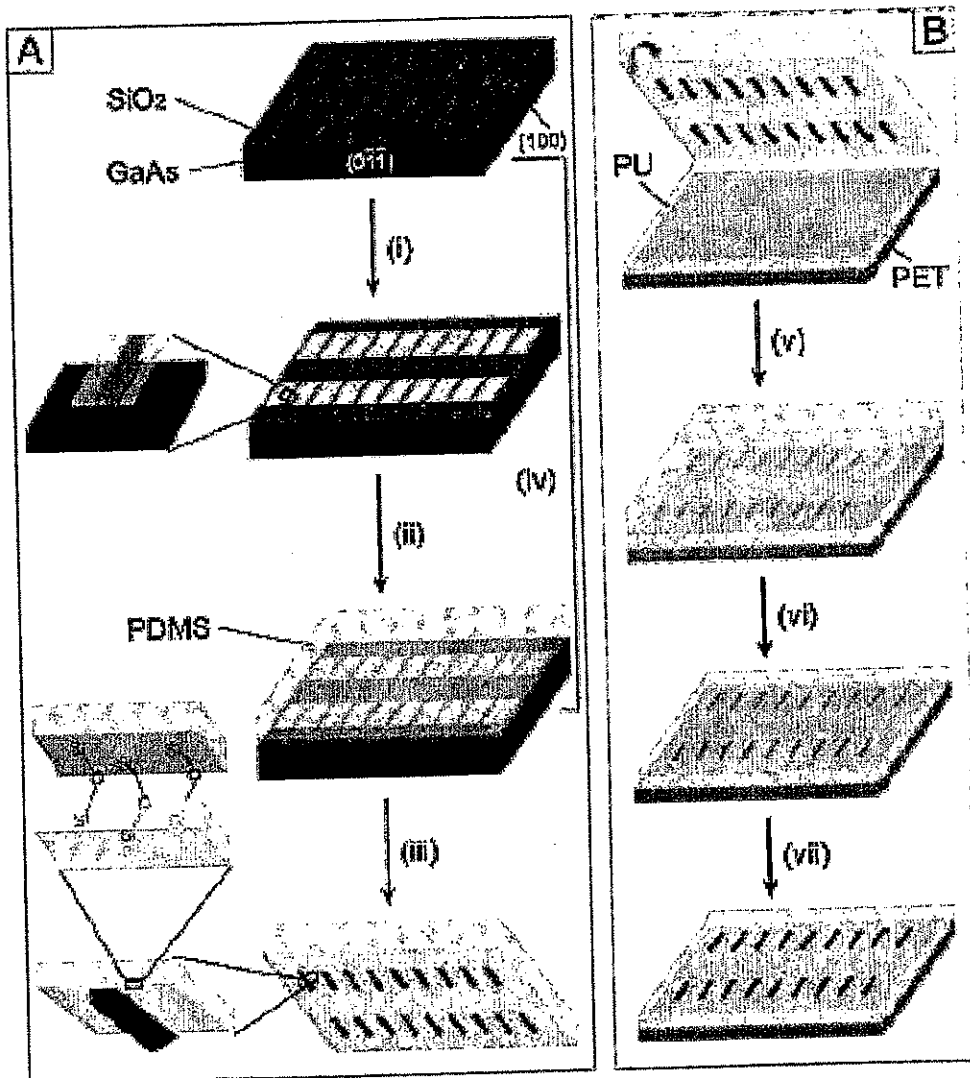
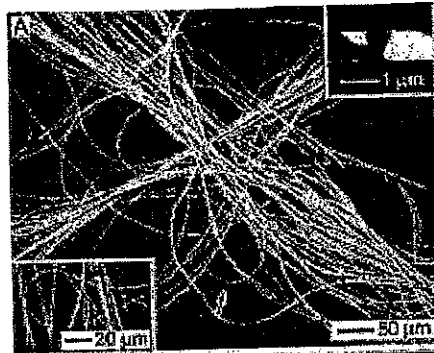


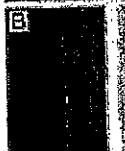
Fig. 19



20A



20B



20C



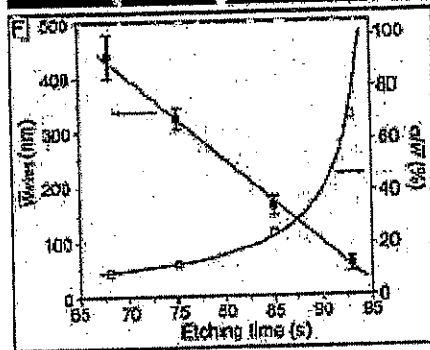
20D

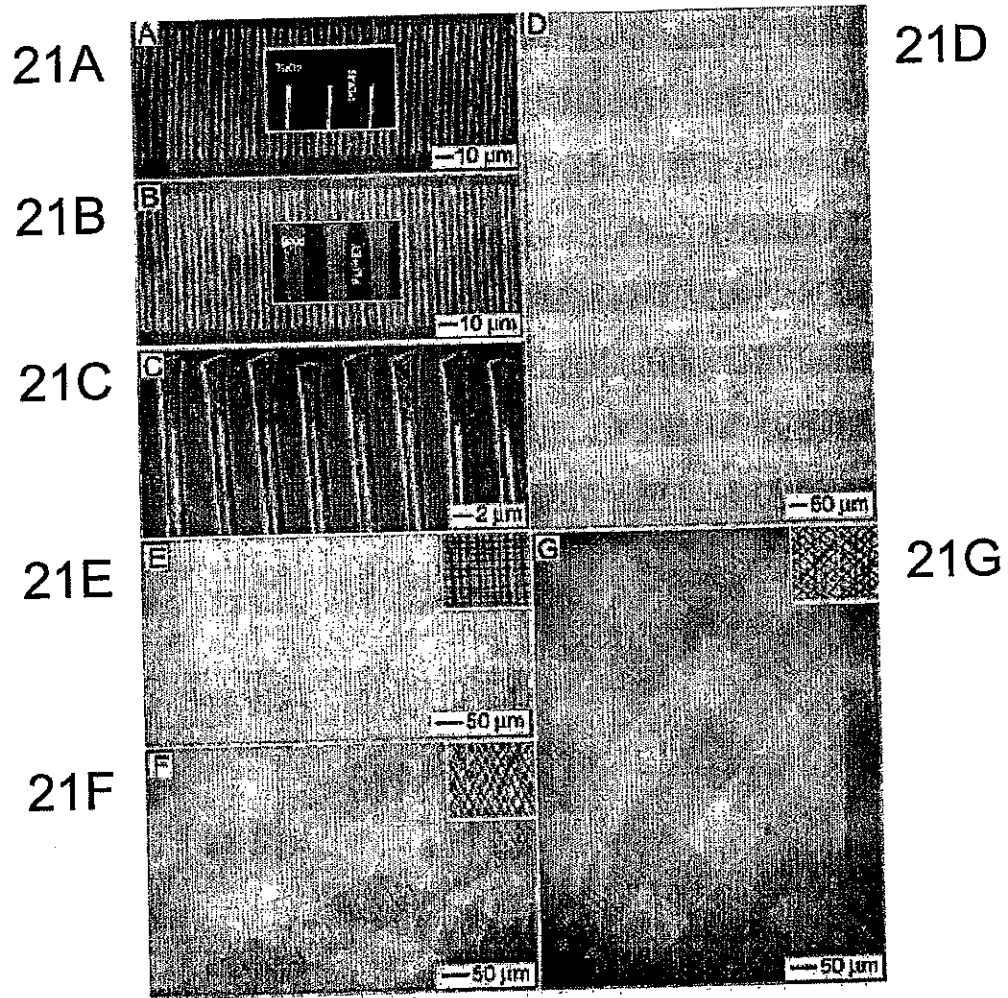


20E

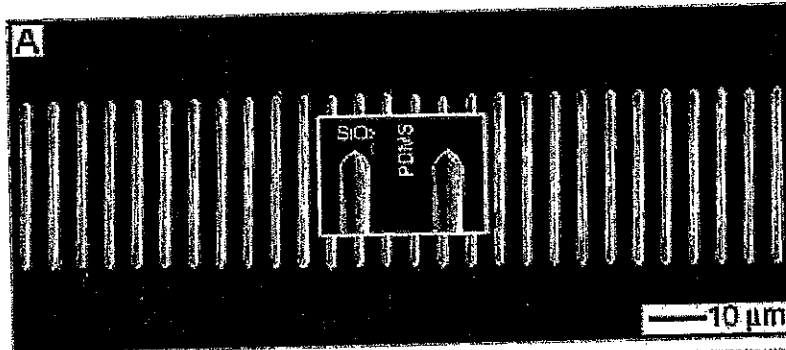


20F

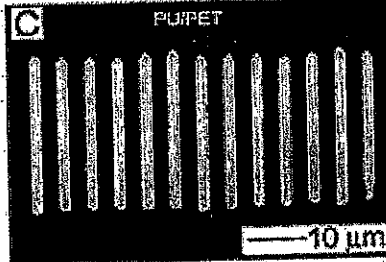
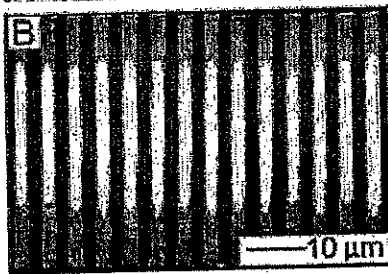




22A

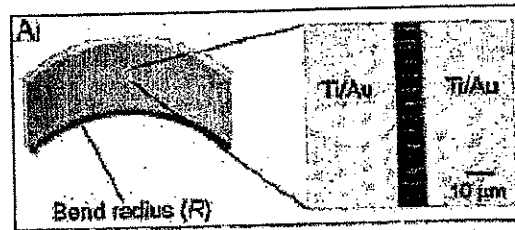


22B

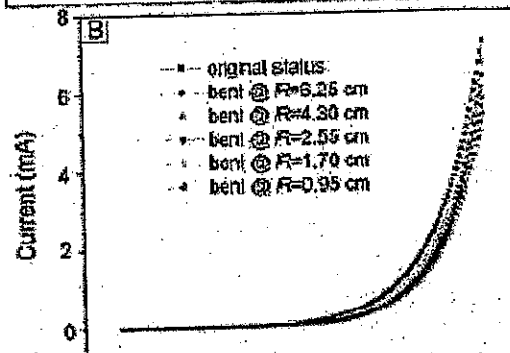


22C

23A



23B



23C

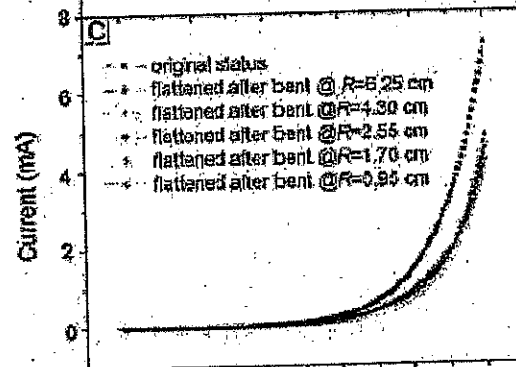
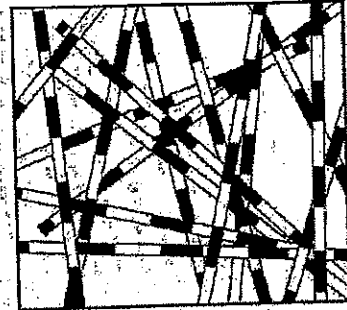


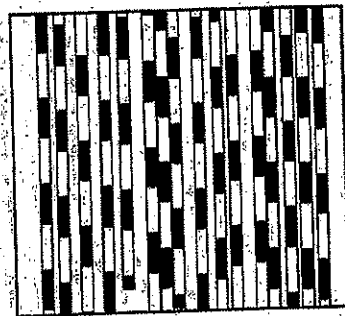
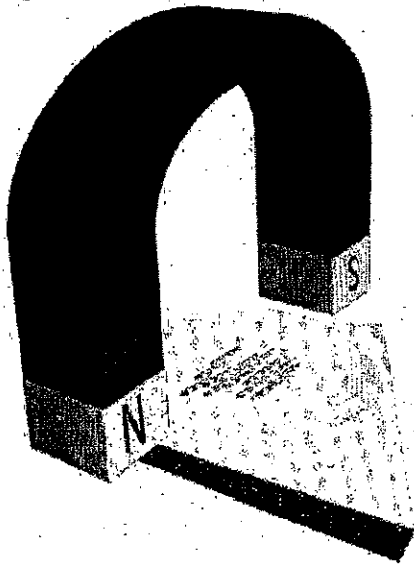
Fig. 24

I. Dispersal in Solution and Casting on Substrate



Magnetic Tags (light)
on Microstructured
Semiconductor (dark)

II. Organization in Magnetic Field



III. Metallization

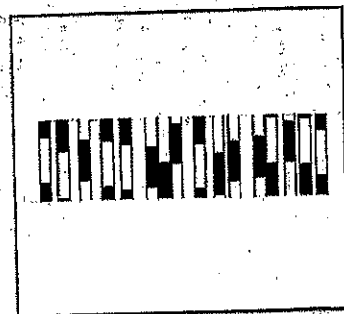
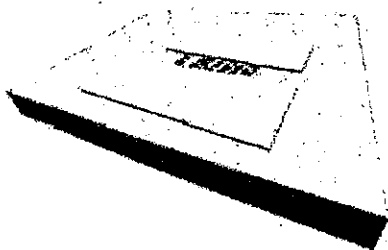
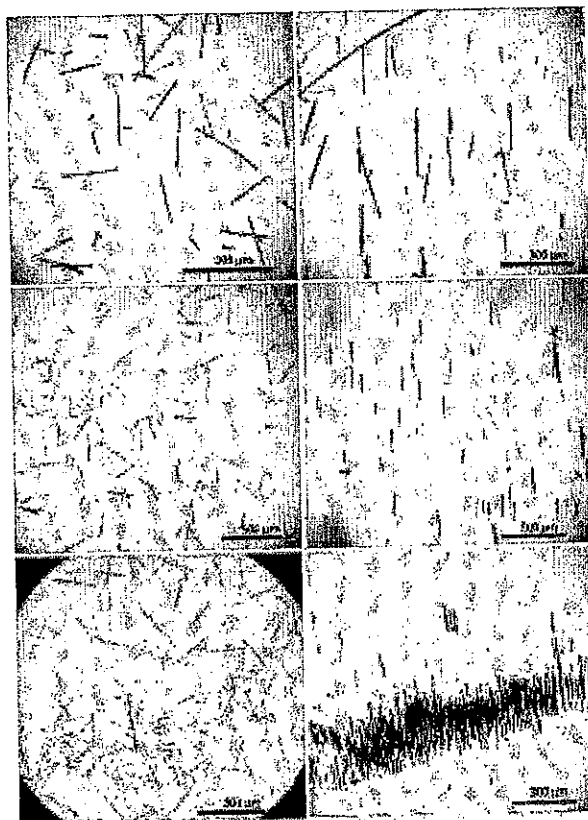
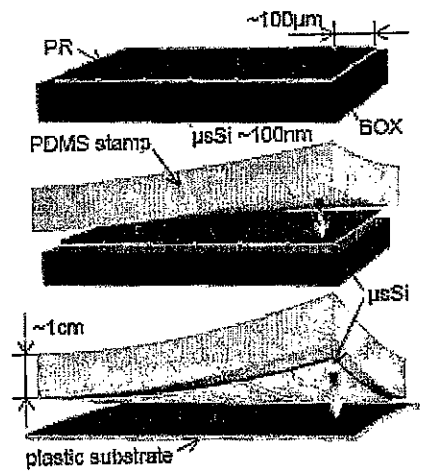


Fig 25

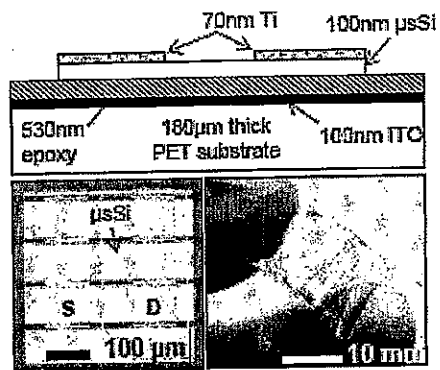


Magnetically tagged microstructures dispersed in solution and cast on a substrate (left). Influence of Magnetic field (right).

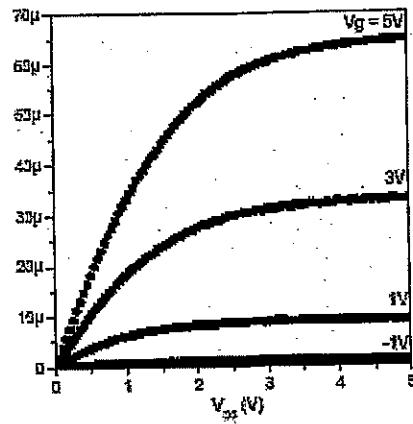
26A



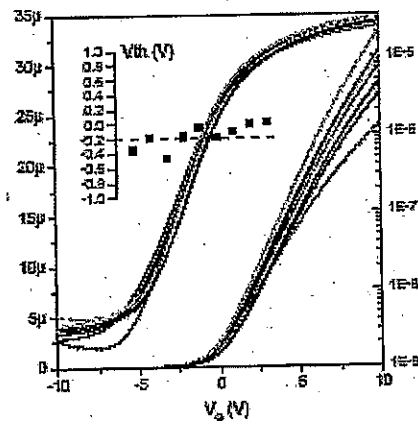
26B



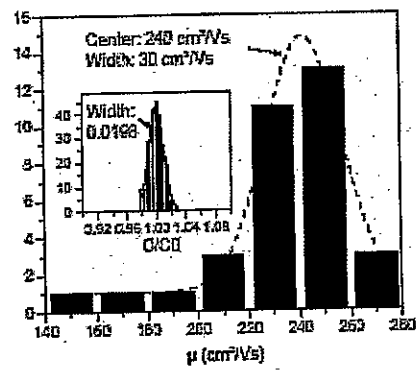
27A



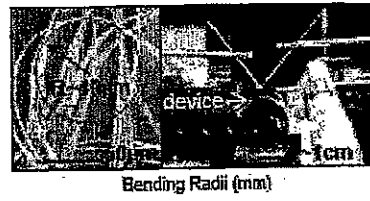
27B



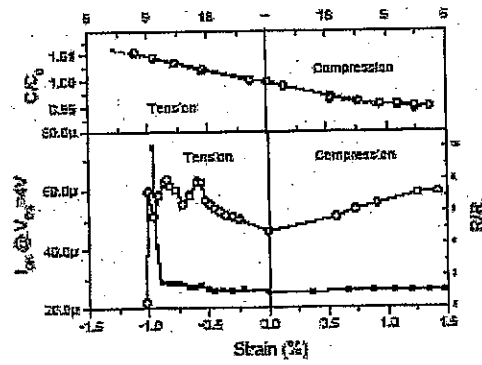
27C



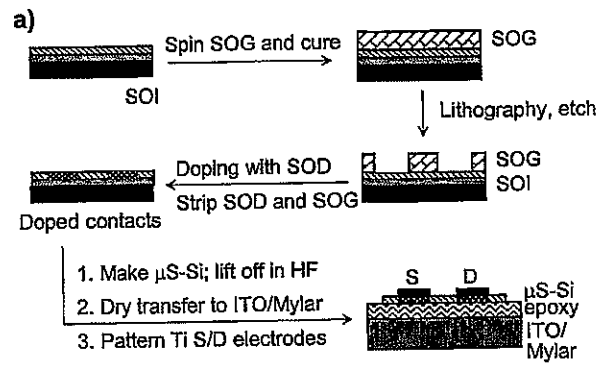
28A



28B



29A



29B



Fig. 30A

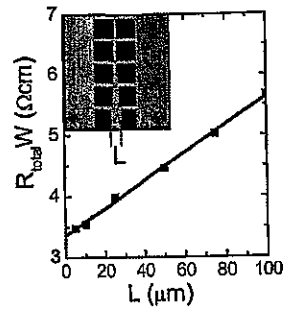


Fig. 30B

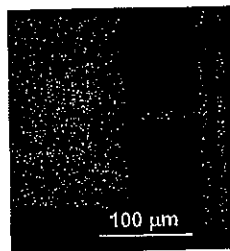


Fig. 31A

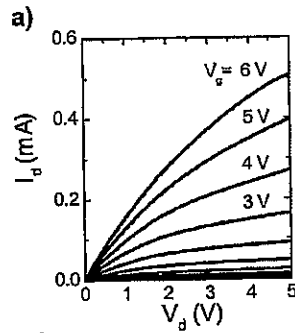


Fig. 31B

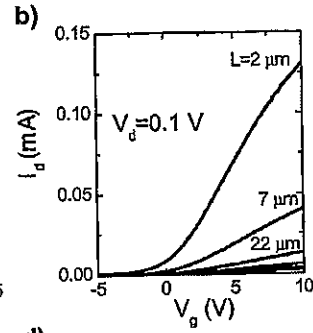


Fig. 31C

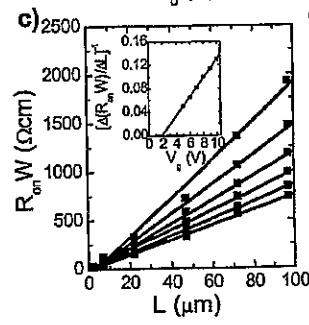


Fig. 31D

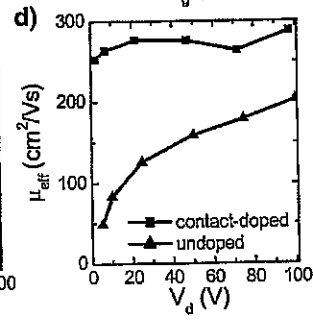


Fig. 32A

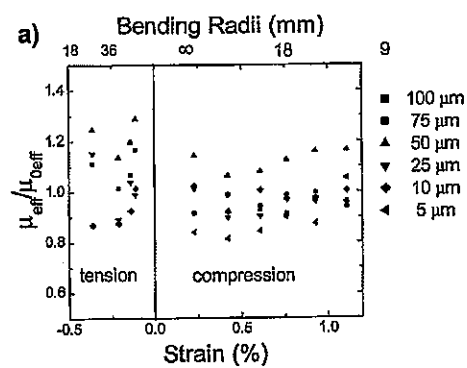


Fig. 32B

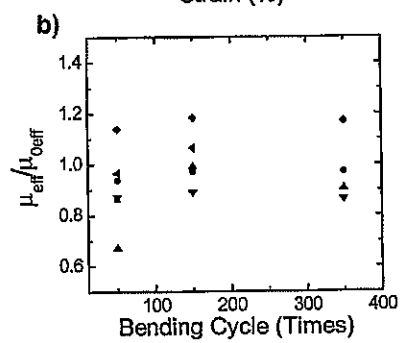
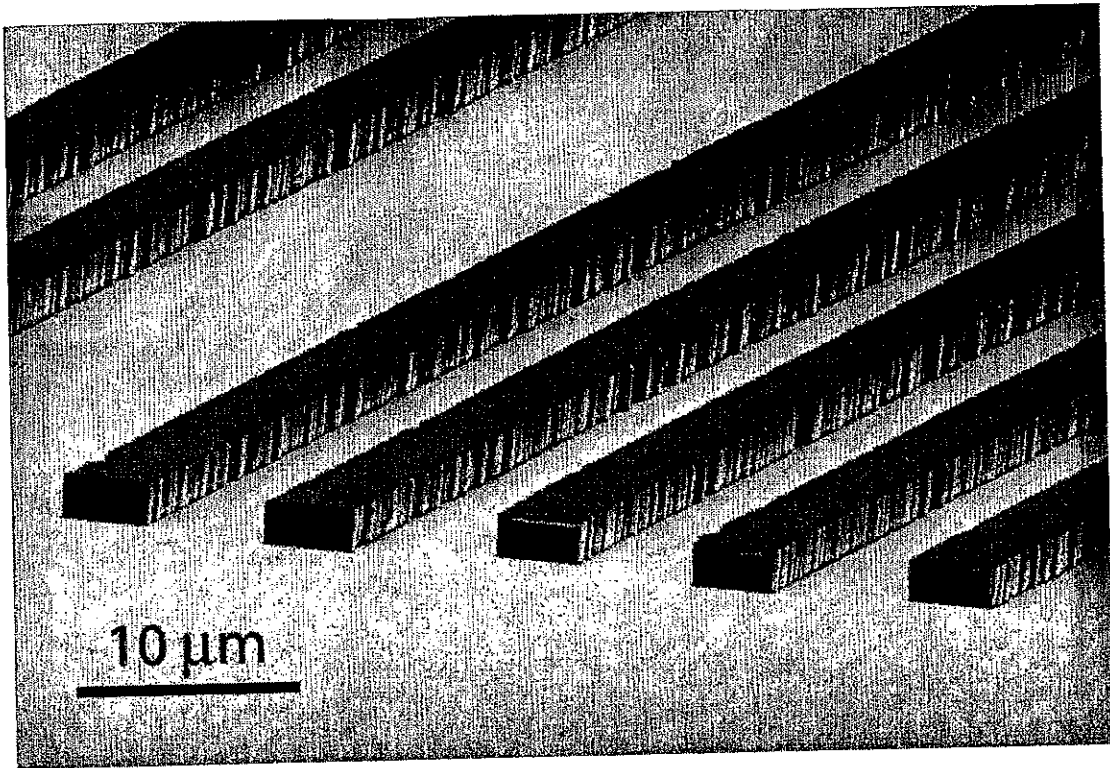


Fig. 33



34A

Provide high quality semiconductor material, such as a single crystal silicon wafer.



Process semiconductor material to generate adjacent N doped and P doped layers, for example using spin on dopants.



1. Pattern and etch processed semiconductor material to define physical dimensions of the printable P-N junction.
2. Lift-off processing to generate monolithic structure comprising the printable P-N junction.
3. Optionally, deposit contacts prior to lift-off, for example, via vapor deposition of metal(s).



Assemble printable P-N junction on substrate using (i) solution printing or (ii) dry transfer printing.



Optionally, deposit contacts onto P-N junction on substrate, for example, via vapor deposition of metal(s).

Fig. 34B

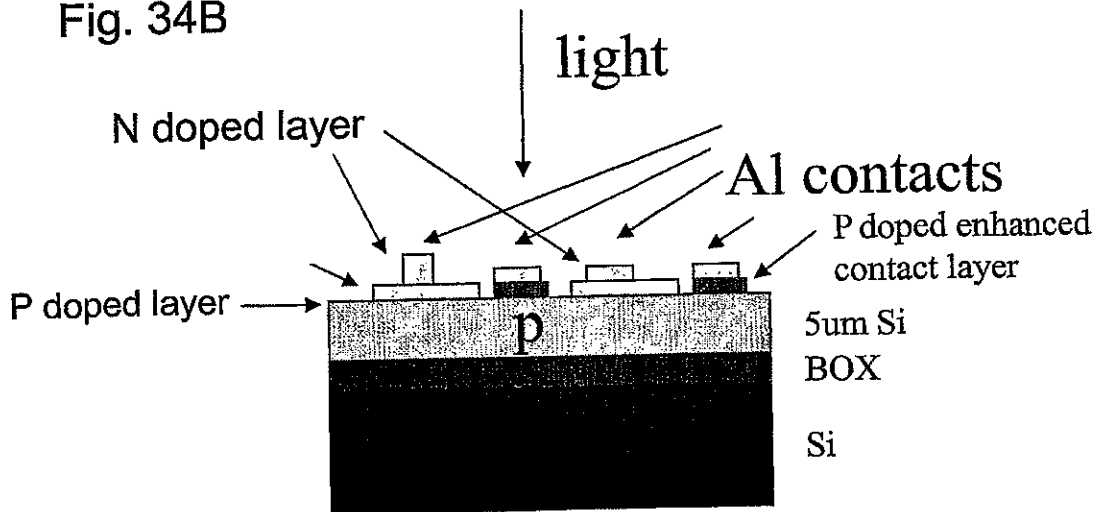
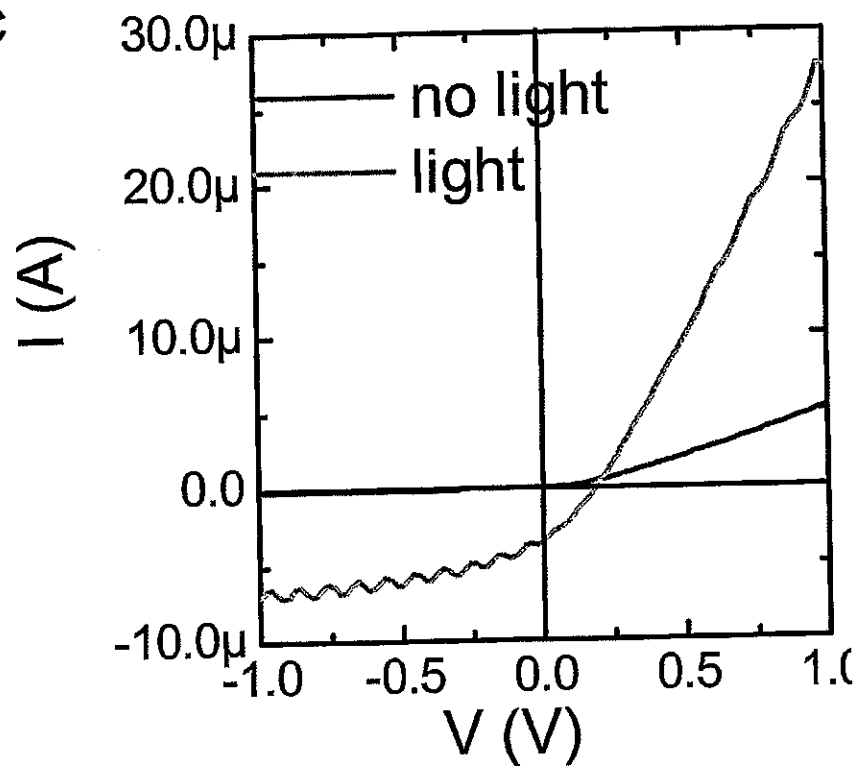


Fig. 34C



35A

Provide high quality semiconductor material, such as a single crystal silicon wafer.



Process semiconductor material to generate discrete N doped and P doped layers, for example using spin on dopants.



1. Pattern and etch processed semiconductor material to define physical dimensions of a separate P doped and N doped semiconductor region.
2. Lift-off processing to generate separate P doped and N doped printable semiconductor elements.
3. Optionally, deposit contacts prior to lift-off, for example, via vapor deposition of metal(s).
4. Optional strip any outer insulating layers (e.g. oxide layers) and remove water on surfaces to be joined.



Assemble P-N junction onto a substrate by printing a first and second doped semiconductor elements using (i) solution printing or (ii) dry transfer printing.



Optionally, anneal P-N junction to achieve high quality Interface between P and N doped semiconductor layers.



Optionally, deposit contacts onto P-N junction on substrate, for example, via vapor deposition of metal(s).

Fig. 35B

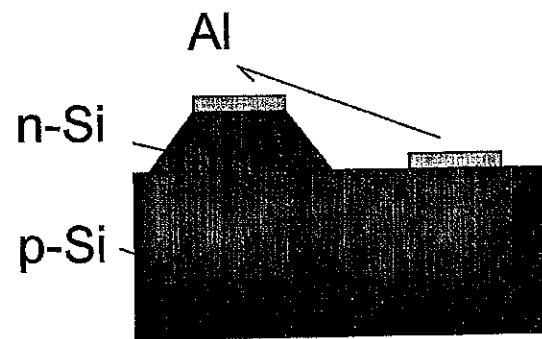


Fig. 35C

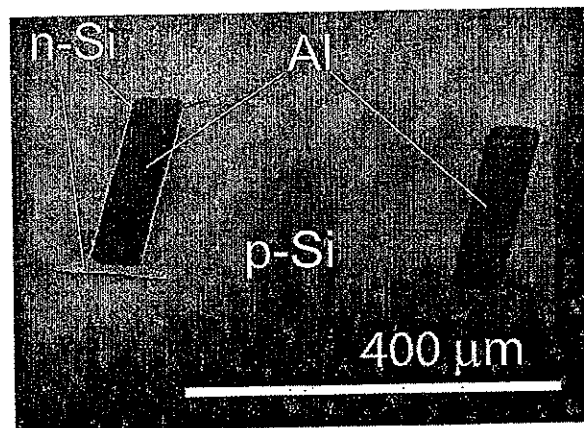


Fig. 35D

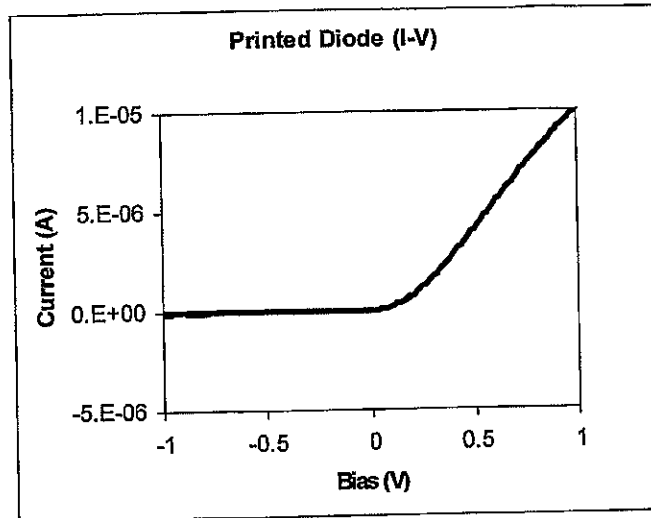


Fig. 35E

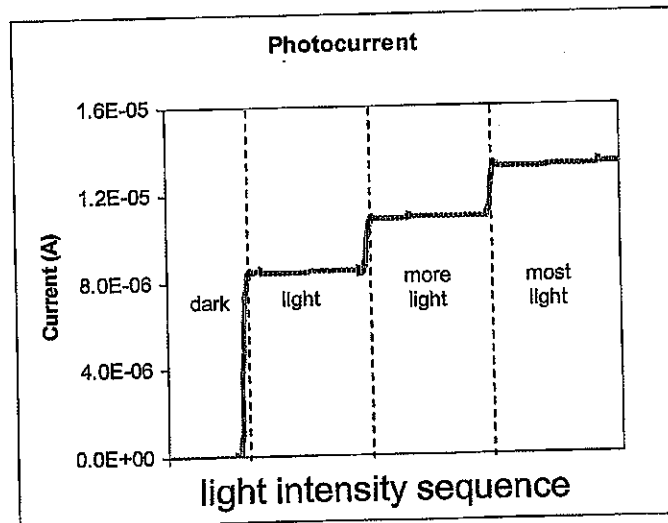


Fig. 36A

Stretchable μ -Si Transistors on Rubber Substrates

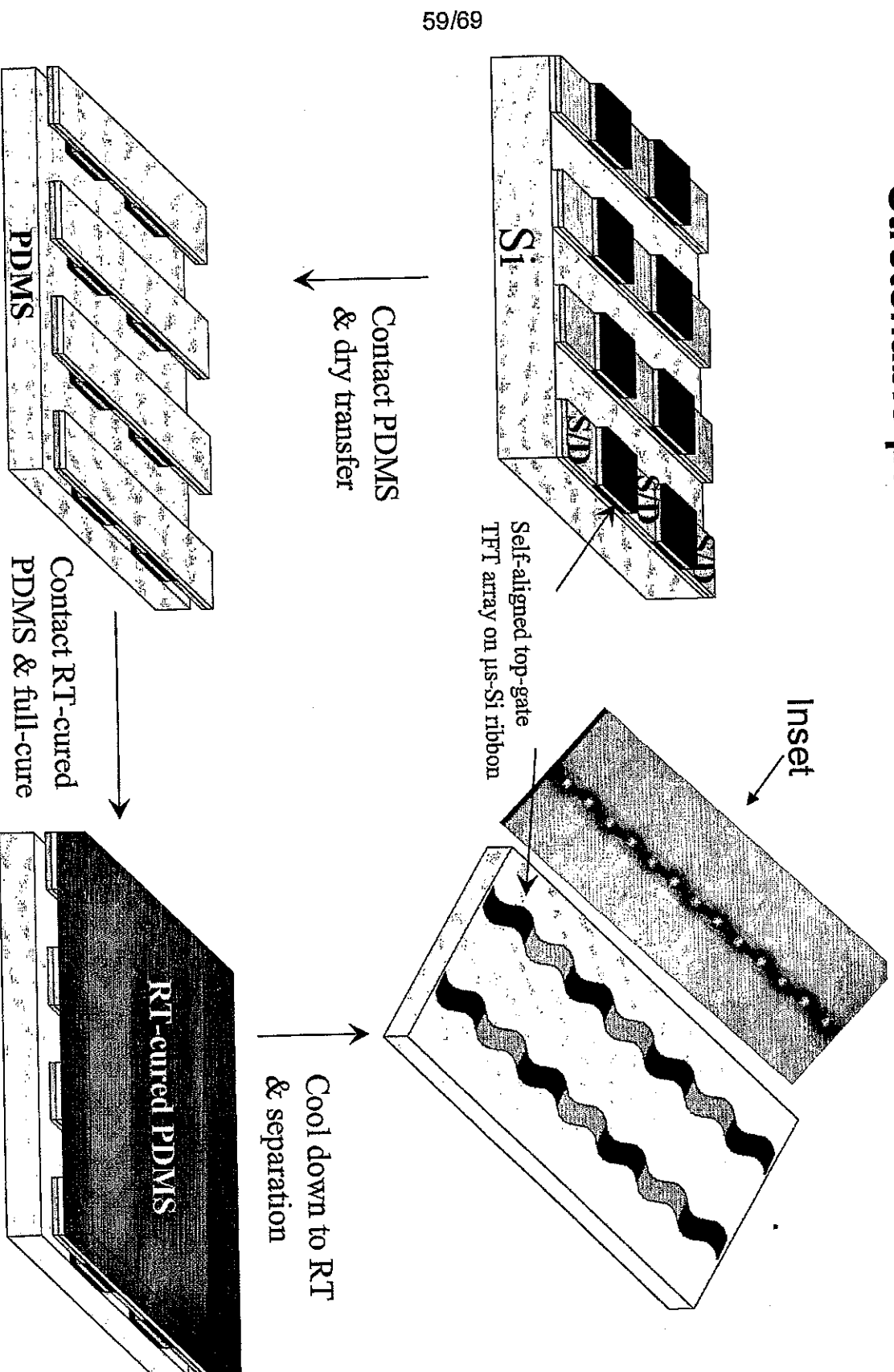


Fig. 36B Stretchable μ -Si Transistors on Rubber Substrates

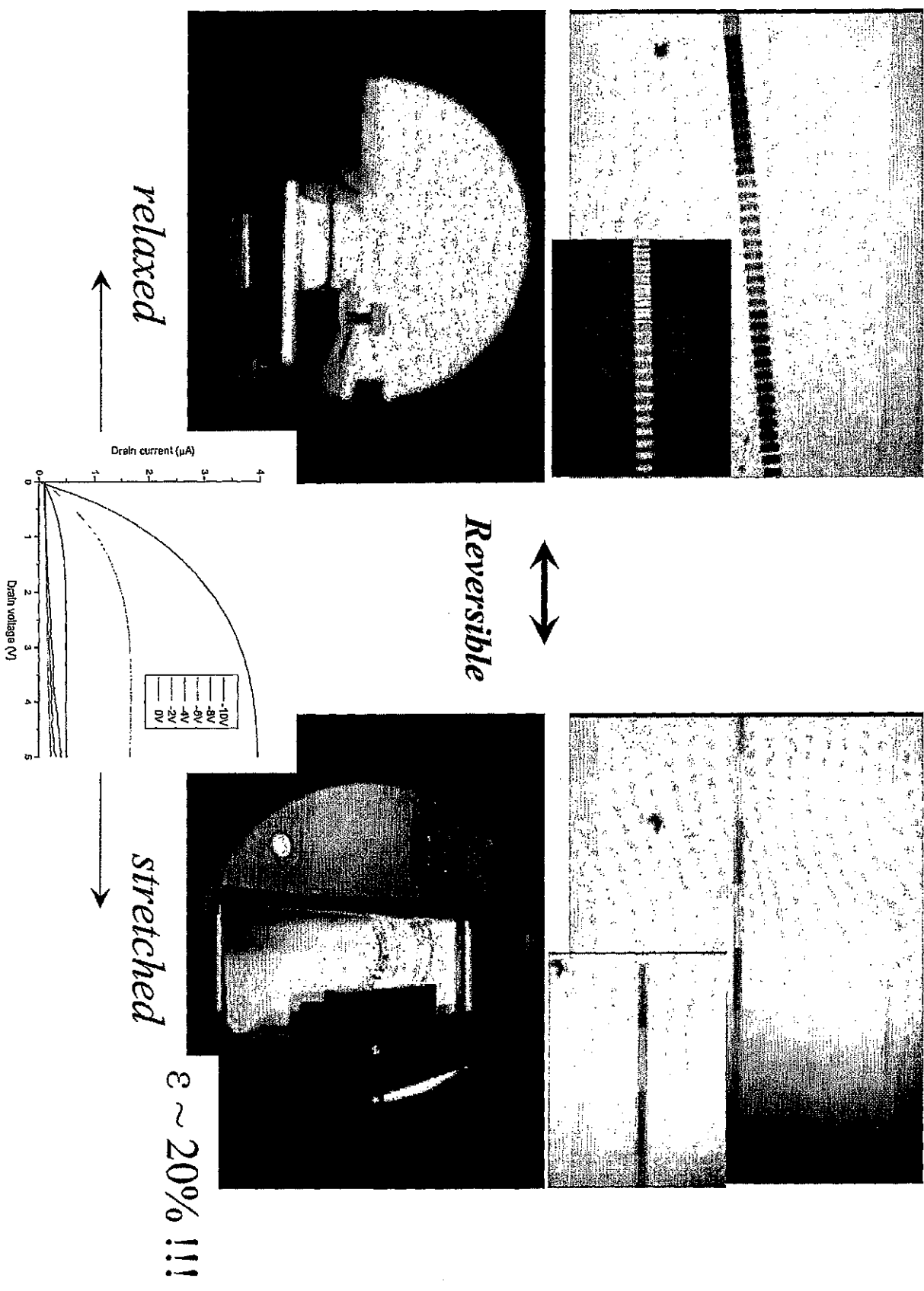


Fig. 37A

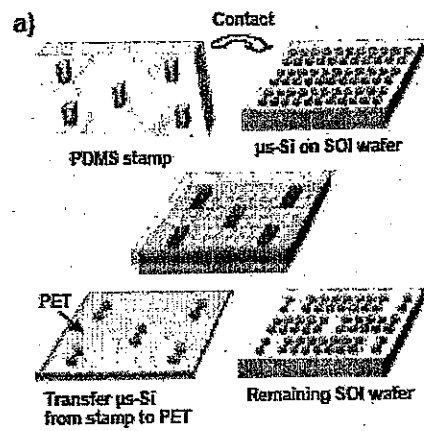


Fig. 37B

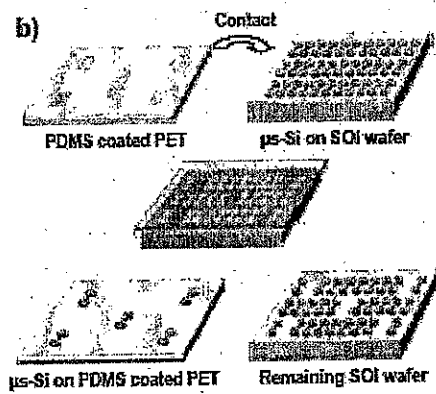


Fig. 38A

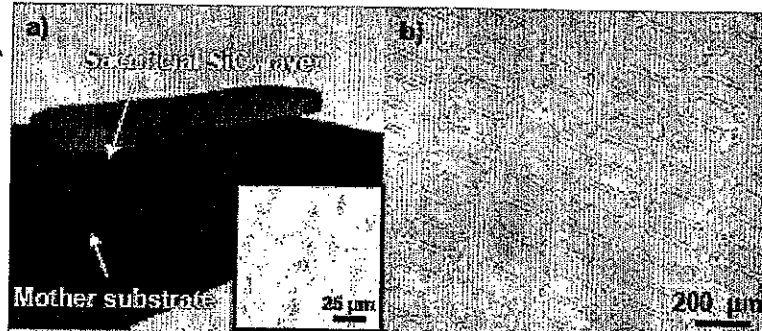


Fig. 38B

Fig. 38C

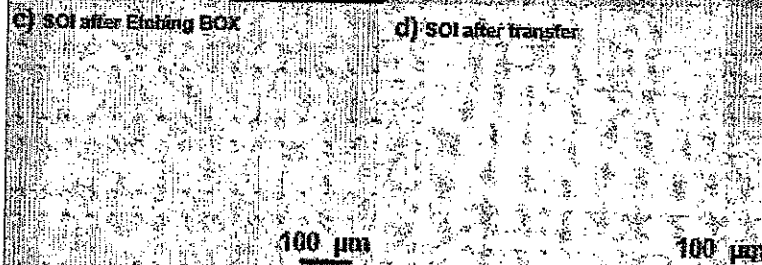


Fig. 38D

Fig. 38E

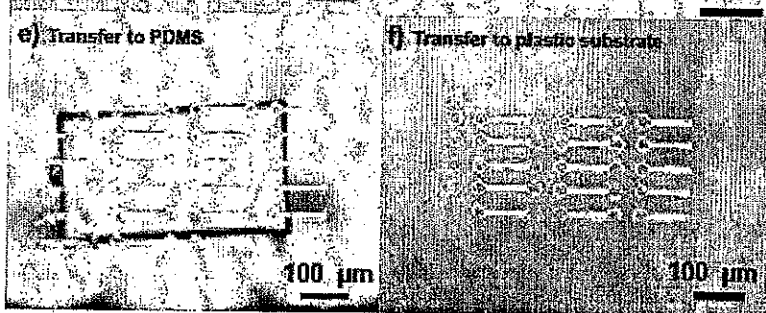


Fig. 38F

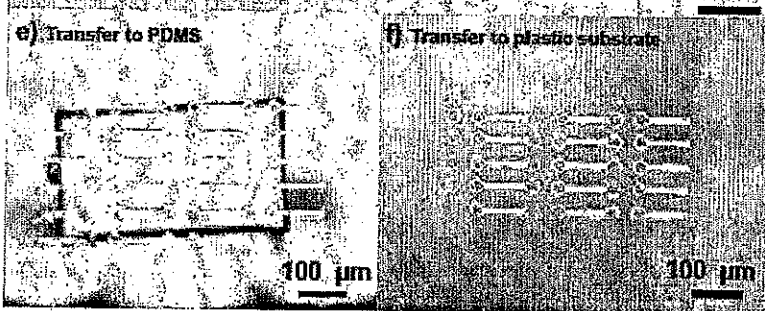


Fig. 39A

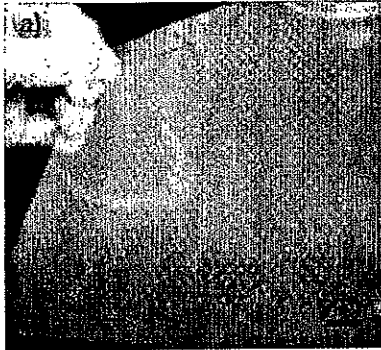


Fig. 39B

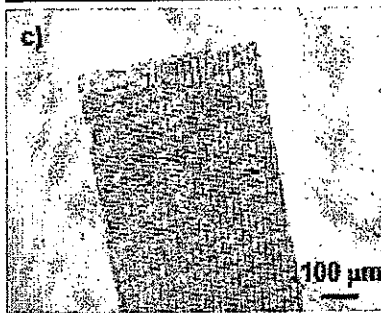
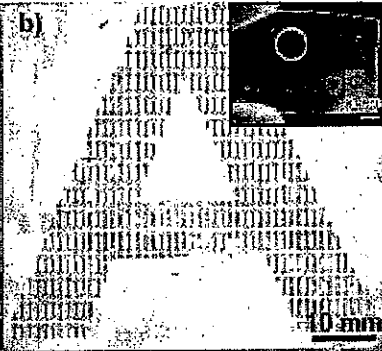


Fig. 39C

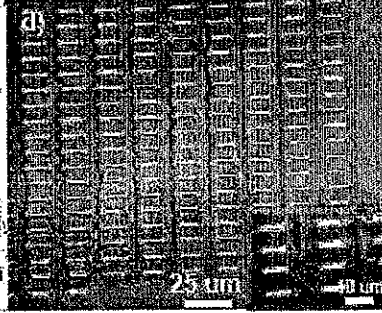


Fig. 39D

Fig. 40A

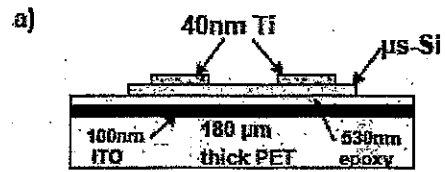


Fig. 40B

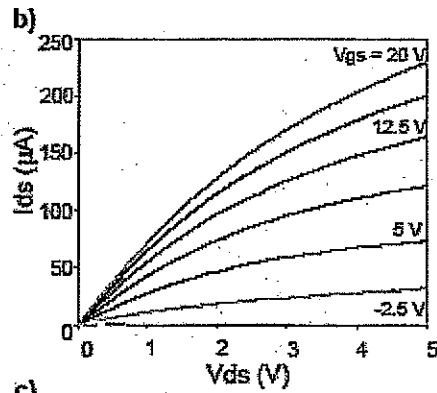


Fig. 40C

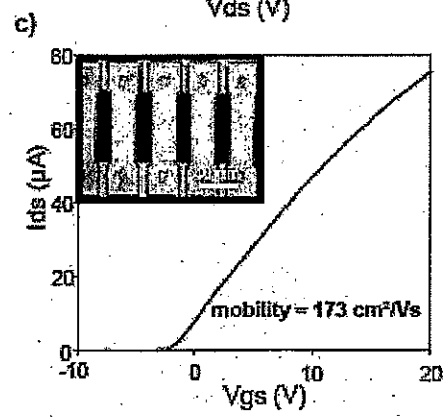


Fig. 41

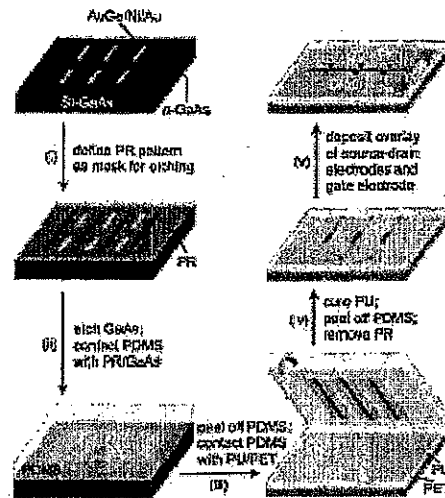


Fig. 42A

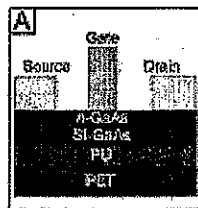


Fig. 42B

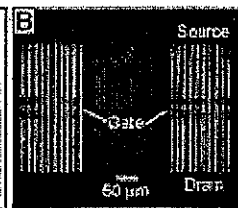


Fig. 42C

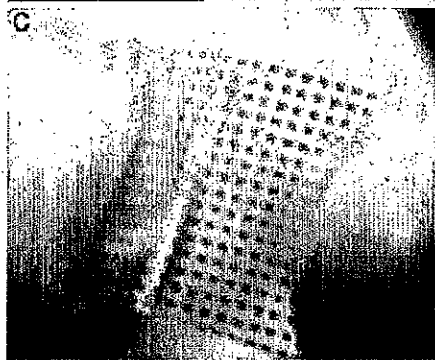


Fig. 43A

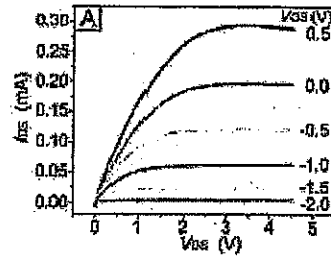


Fig. 43B

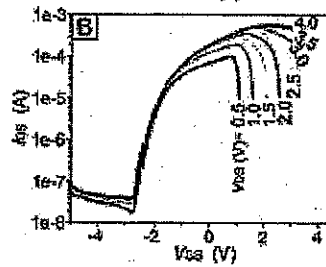


Fig. 43C

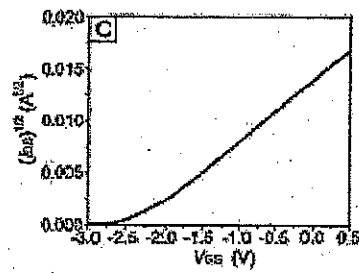


Fig. 44A

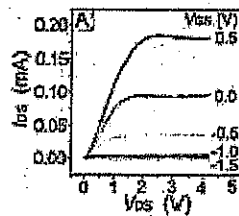


Fig. 44B

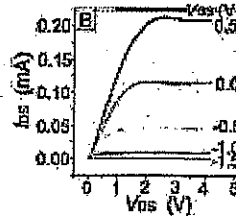


Fig. 44C

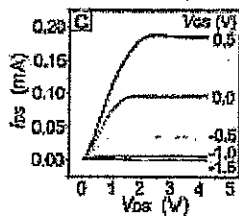


Fig. 44D

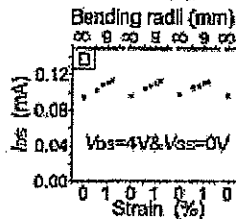


Fig. 45: P Type μ S-Si bottom gate TFTs

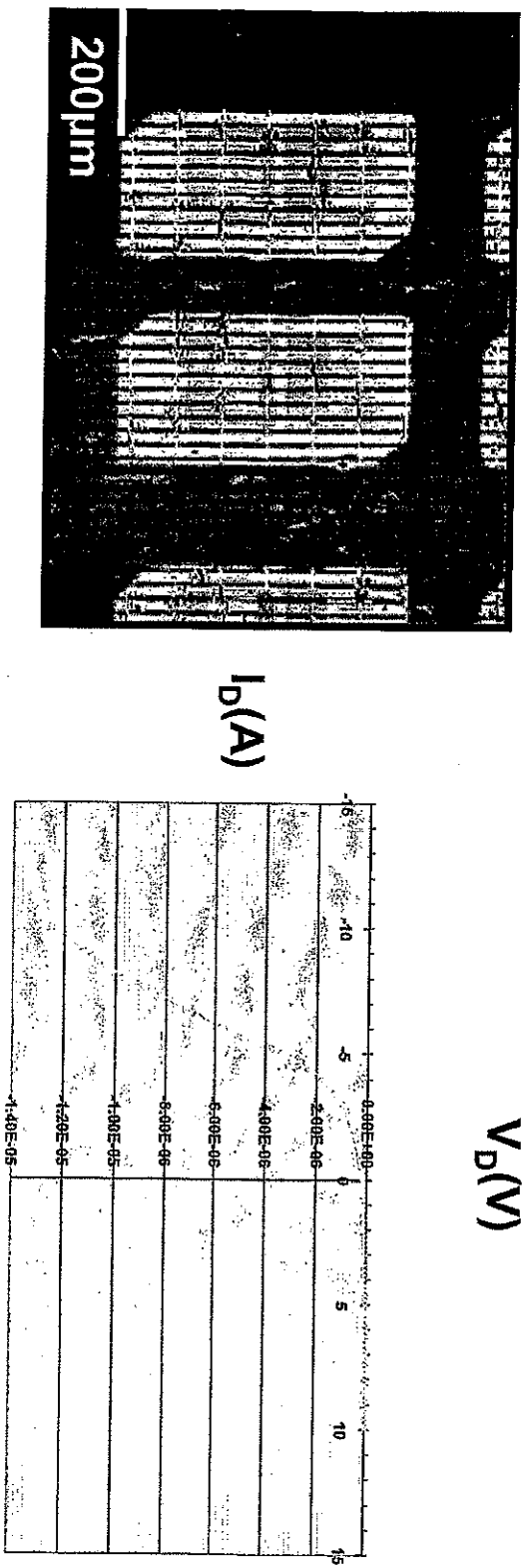
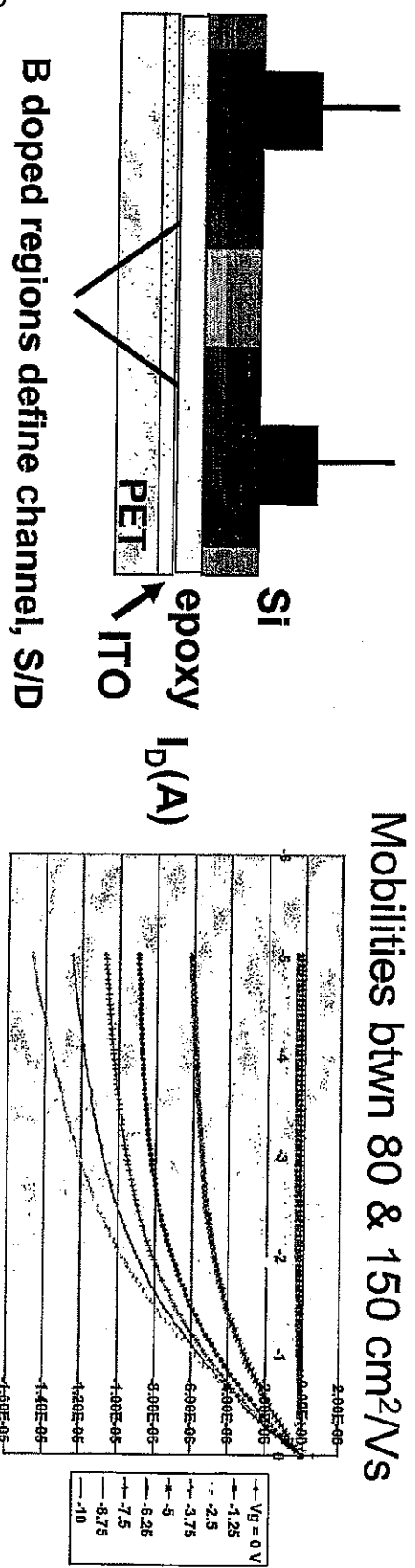
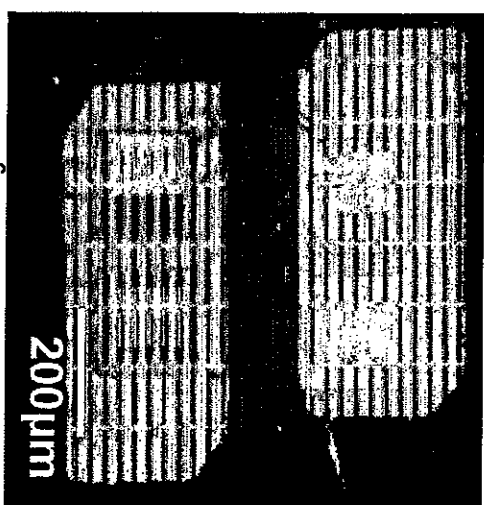
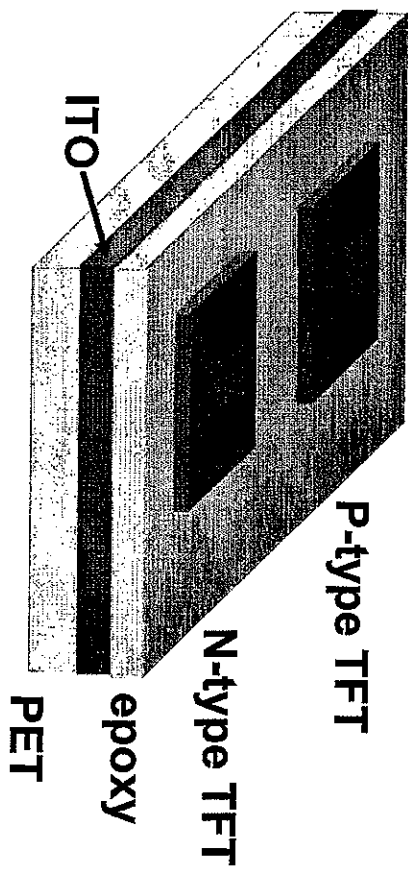


Fig. 46: Complementary Logic Gate (Inverter) on Plastic



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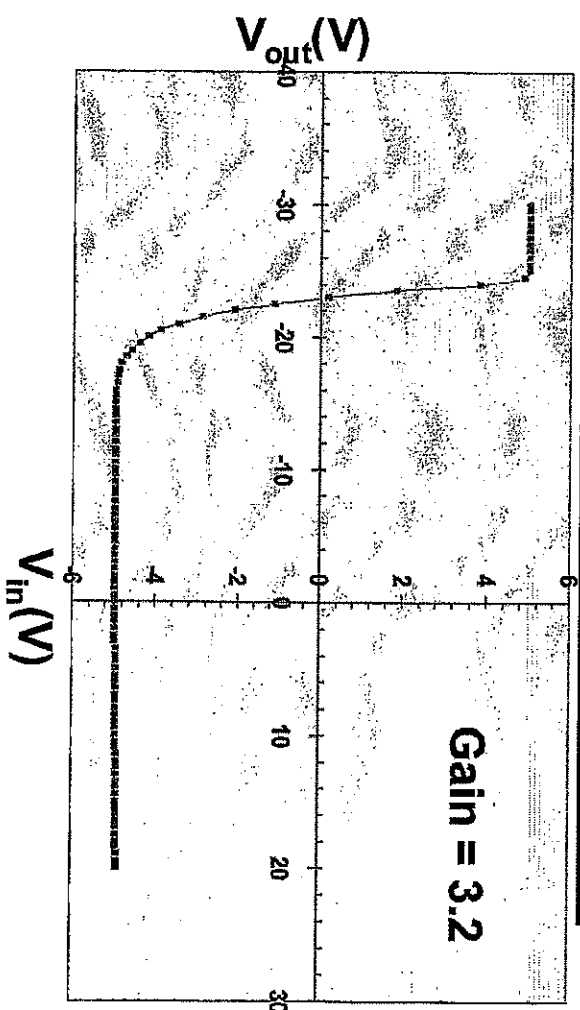
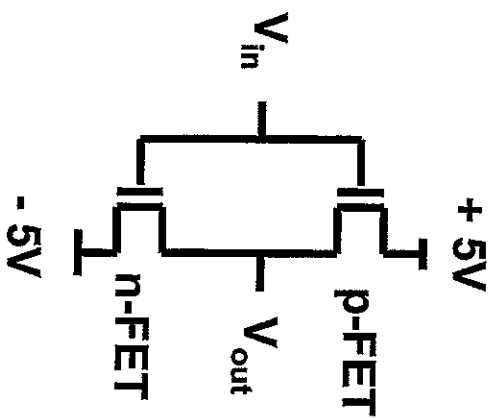


Fig. 47: Top Gate μ -Si Transistors on Plastic

