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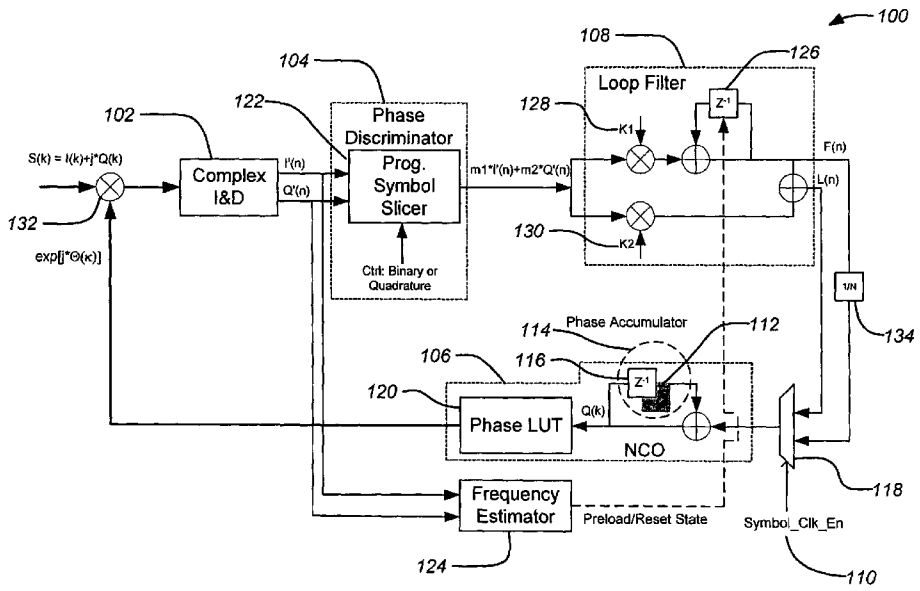
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(54) Title: DECISION DIRECTED SUPPRESSED CARRIER SYMBOL-RATE PLL WITH PROGRAMMABLE PHASE DISCRIMINATOR AND CHIP-RATE PHASE EXTRAPOLATION



(57) Abstract: A phase lock loop apparatus and method is disclosed. A typical apparatus includes a demodulator receiving a phase error signal from a comparator at a chip rate and providing a phase error update over a symbol period from the phase error signal wherein the chip rate is higher than the symbol rate. A phase discriminator produces a phase error output at the symbol rate from the phase error update based upon a signal modulation type. A loop filter produces one or more phase estimate parameters at a symbol rate from the phase error output and a numerically controlled oscillator (NCO) extrapolates a phase reference at a chip rate from the one or more phase estimate parameters at a symbol rate. The comparator produces the phase error signal to the demodulator based upon the phase reference and an incoming signal.

WO 2004/021660 A1