

SPECIFICATION

Electronic Timepiece

This invention relates to electronic timepieces.

- One known liquid crystal display device is such
- 5 that the contents to be displayed by the display device are quickly changed by means of an adjusting means. However the display itself does not necessarily respond to changing of the contents to be displayed so that the display
- 10 disappears or a meaningless display is produced. Thus if the contents in counters for counting time in such an electronic timepiece are changed at high frequency, one or more parts of the display produced by the display device do not respond
- 15 and so a desired display is not produced. This has been found to be particularly troublesome in conventional electronic timepieces.

- According to the present invention there is provided an electronic timepiece comprising: time
- 20 counting means for counting a standard time signal; selection means for selecting outputs from the said time counting means to produce the parts of a time indication; a liquid crystal display device for receiving the outputs from the said
- 25 selection means to display the time indication; time adjusting means for adjusting the contents of the said time counting means to adjust the time indication displayed by the display device; and control means for controlling the said
- 30 selection means during adjustment of the time indication so that the effective voltage applied to part of the display device when the display is being adjusted is greater than the voltage applied when the display is not being adjusted.

- 35 Preferably the display device is arranged to produce an analog display of the time indication.

- In a preferred embodiment the timepiece is arranged so that the effective voltage applied to the part of the time display when the display is
- 40 being adjusted is greater by a factor $\sqrt{2}$ than the voltage applied when the display is not being adjusted.

- The invention is illustrated, merely by way of example, in the accompanying drawings, in
- 45 which:—

- Figure 1, consisting of Figures 1A, 1B and 1C, is a block diagram of one embodiment of an electronic timepiece according to the present invention;

- 50 Figure 2 is a plan view of a segment electrode arrangement of a liquid crystal display device of the electronic timepiece of Figure 1;

- Figure 3 is a plan view of a common electrode arrangement of the display device of Figure 2;

- 55 Figure 4 is a diagram illustrating an output conversion circuit and a segment voltage supply circuit of the electronic timepiece of Figure 1;

- Figure 5 is a diagram illustrating a voltage selector of the electronic timepiece of Figure 1;

- 60 Figure 6 is a diagram illustrating a common voltage supply circuit of the electronic timepiece of Figure 1; and Figure 7 is a voltage table illustrating the operation of the electronic timepiece of Figure 1.

- 65 Referring first to Figure 1 an electronic timepiece according to the present invention comprises a crystal controlled time standard oscillator 1 the output of which is frequency divided by a multistage frequency divider 2, the
- 70 reduced frequency output from which is fed to a decimal counter 3 counting units of seconds. A carry output of the decimal counter 3 is fed to a divide-by-six counter 4. A decimal counter 5 and a divide-by-six counter 6 count units of minutes
- 75 and a decimal counter 7 and a divide-by-six counter 8 count units of hours. All the aforementioned counters produce binary decimal coded outputs.

- A duodecimal counter 9 counts carry output pulses of the counter 4 or time adjusting pulses described later herein. A timing pulse generator 10 receives output pulses such as pulses of 128
- 80 Hz from the frequency divider 2 and successively produces timing pulses at terminals P_1 to P_3 .

- 85 Periodic pulses produced at the terminal P_1 trigger a flip-flop circuit 11, pulses at an output terminal Q of which are fed to a voltage selector 12. The voltage selector 12 produces periodically relative voltages O , v_o , $2v_o$ and $3v_o$ at terminals S_o , S_1 , C_o and C_1 , respectively. The pulses at the terminal P_2 of the timing pulse generator 10 are fed to one input of an OR gate circuit 13 (Figure 1B) via a line L_4 and the pulses at the terminal P_1 are fed to one input of an AND gate circuit 14 and
- 95 one input of an AND gate circuit 15 via a line L_5 . An output appearing across a resistor 16 depends upon ON or OFF operation of a manual switch 17 connected to a positive potential E_o and is directly fed to the other input of the AND gate circuit 15
- 100 and is also fed via an inverter 18 to the other input of the AND gate circuit 14.

- AND gate circuits 19 to 21 control passage of input data responsive to pulses fed via lines M_2 , M_1 and L_3 respectively. AND gate circuits 22 to
- 105 24 control passage of input data responsive to the pulses fed via the lines M_2 , M_1 and L_3 respectively. An OR gate circuit 25 feeds output data from the gate circuits 19 to 21 to a decoder 26. An OR gate circuit 27 feeds output data from the gate circuits 22 to 24 to a decoder 28. The output of the decoder 26 is fed to an output conversion circuit 29 for changing the order of outputs produced from output terminals z_o to z_9 responsive to inputs fed directly and via an
- 115 inverter 30 from a 2^0 terminal of the gate circuit 27. The outputs of the output conversion circuit 29 are fed to a segment voltage supply circuit 31 for producing voltages to be applied to segment electrodes as explained later herein. The outputs of the decoder 28 are fed to a common voltage supply circuit 32 to be applied to common electrodes explained later as well as to the segment electrodes. A time adjusting pulse generator 33 produces time adjusting pulses
- 125 which are generated in accordance with rotation of a manually rotatable means. An example of such manually rotatable means is given in U.S. Patent Application No. 874 625 and West German Patent Application No. P 28 05 005.7

(Offenlegungsschrift No. 2 805 005). The time adjusting pulses are fed to the counter 9 via an AND gate circuit 34 and an OR gate circuit 35.

A liquid crystal display device includes a

segment electrode arrangement 36 consisting of 60 radial equi-angularly spaced apart segment electrodes 36a. The first ten of the segment electrodes 36a are respectively connected to the terminals e_1 to e_{10} of the segment voltage supply circuit 31. The remaining segment electrodes are connected as follows. The count order of the segment electrodes designated below is in the clockwise direction starting with the segment electrode 36a which is connected to the terminal e_1 as the first. The 10th segment electrode 36a is connected to the 11th: the 9th segment electrode is connected to the 12th and the 1st segment electrode is connected to the 20th which is connected to the 21st: the 19th segment electrode is connected to the 22nd and the 11th segment electrode is connected to the 30th.

The display device also includes a common electrode arrangement generally designated 37 in Figure 3. The common electrode arrangement consists of six similar inner common electrodes 37a and six similar outer common electrodes 37b. Spaces 37c which separate the individual common electrodes 37a and 37b from one another radially are located between the 10th segment electrode and the 11th: between the 20th segment electrode and the 21st: between the 30th segment electrode and the 31st: between the 40th segment electrode and the 41st: between the 50th segment electrode and the 51st: and between the 60th segment electrode and the 1st, counting in the clockwise direction.

The segment electrode arrangement is positioned over the common electrode arrangement and a layer of liquid crystal material (not shown) is interposed between the two electrode arrangements in a sealed housing (not shown) through which the display produced can be observed.

Figure 4 shows, in some detail, the output conversion circuit 29 and the segment voltage supply circuit 31 of Figure 1. Reference numerals 38 to 47 denote AND gate circuits, reference numerals 48 to 52 denote OR gate circuits, reference numerals 53 to 62 denote switching circuits and reference numerals 63 to 67 denote inverters.

Figure 5 shows, in some detail, the voltage selector 12 of Figure 1A. Reference numerals 68 to 75 denote switching circuits and reference numeral 76 denotes an inverter.

Figure 6 shows, in some detail, the common voltage supply circuit 32 of Figure 1C. Reference numerals 77 to 82 denote AND gate circuits, reference numerals 83 to 92 denote switching circuits and reference numerals 93 to 97 denote inverters.

The relative voltages to be applied to the segment electrodes and the common electrodes will now be described.

Let it be assumed that values of relative voltages are predetermined and the liquid crystal display device used in this embodiment will not produce a display if the periodic voltage

difference between one of the segment electrodes and one of the common electrodes beneath it is smaller than $|v_0|$ but a display will be produced if the voltage difference is $3|v_0|$ or more. On this assumption a voltage of 0 is applied to terminals I_1 and I_4 , a voltage v_0 is applied to terminals I_2 and I_7 , a voltage $2v_0$ is applied to terminals I_3 and I_6 and a voltage $3v_0$ is applied to terminals I_5 and I_8 .

In Figure 1 when periodic pulses are produced at the terminal P_1 of the timing pulse generator 10, they trigger the flip-flop circuit 11 thereby producing periodic pulses at the output terminal Q thereof. Consequently in Figure 5, voltages 0 and $3v_0$ are alternately produced at the terminal S_0 , voltages v_0 and $2v_0$ are alternately produced at the terminal S_1 , voltages 0 and $3v_0$ are alternately produced at the terminal C_0 , and voltages $2v_0$ and v_0 are alternately produced at the terminal C_1 . The relationship between these voltages is illustrated in Figure 7. In Figure 7 the voltages v_s are those which may be assumed by the terminals S_0 , S_1 and the voltages v_c are those which may be assumed by the terminals C_0 , C_1 . Among these two groups of voltages, those on the left are voltages that will be produced at the terminals S_0 , S_1 , C_0 , C_1 every time a pulse is produced at the terminal P_1 . In the remainder of Figure 7 the voltage difference between the respective voltages produced at the terminals S_0 , S_1 and the respective voltages produced at the terminals C_0 , C_1 , namely the voltages v_{s-c} are illustrated. As will be seen from Figure 7 when a voltage is applied between the terminals S_0 and C_0 a display element corresponding to electrodes connected thereto is displayed.

Given the aforementioned assumption, there will now be described the operation of the electronic timepiece. When any time adjusting operation is not effected the manual switch 17 of Figure 1C is kept open. Therefore a logic level on the line L_6 is logic 0, which is inverted to logic 1 by the inverter 18 to open the AND gate circuit 14. Therefore periodic pulses at the terminal P_1 of the timing pulse generator 10 appear at the output terminal of the AND gate circuit 14. Meanwhile periodic pulses at the terminal P_2 of the timing pulse generator 10 appear at the output terminal of the OR gate circuit 13 via the line L_4 .

For ease of explanation, let us consider the production of a display of 10 hrs: 5 mins: 0 secs. In this example, the counter 3 counts 0, the counter 4 counts 0, the counter 5 counts 5, the counter 6 counts 0, the counter 7 counts 0, the counter 8 counts 5 and the counter 9 counts 5. In this state, when the periodic pulses appear at the terminal P_1 of the timing pulse generator 10, the gate circuits 19, 22 are opened to feed seconds output data from the counter 3 to the gate circuit 25 and to feed seconds output data from the counter 4 to the gate circuit 27. Therefore logic 0

is produced at the terminals 2^0 to 2^3 of the gate circuit 25 and also at the terminals 2^0 to 2^2 of the gate circuit 27. Consequently logic 1 is produced at the terminal $\bar{h}$, logic 0 is produced at the

- 5 terminal h and logic 1 is produced at the terminal x_0 of the decoder 26. Meanwhile referring to the circuit of Figure 4 logic 1 is produced at both output terminals of the AND gate circuit 38 and the OR gate circuit 48 so that voltages being fed to the terminal S_0 appear at the terminal e_1 .
 10 Furthermore the switching circuits 54 to 56, 58 to 60, 62 are turned ON to produce voltages being fed to the terminal S_1 at the terminals e_2 to e_{10} . In addition the decoder 28 produces logic 1 at the terminal y_0 to produce voltages being fed to terminal C_0 at the terminal k_1 of Figure 6.
 15 Meanwhile the AND gate circuits 77 to 82 are opened in consequence of logic 1 produced at the terminal $\bar{P}_3$. The above logic level of the terminal $\bar{P}_3$ is for the reason that while a pulse is being produced at the terminal P_1 there is no pulse produced at the terminal P_3 , as a result, if logic 0 is produced at the terminal P_3 logic 1 results from the terminal $\bar{P}_3$ which is an inverted output from
 20 the terminal P_1 .

- Now since the gate circuits 77 to 82 are opened the switching circuit 83 is turned ON to produce voltages fed to the terminal C_0 at the terminal g_1 . Meanwhile voltages fed to the
 30 terminal C_1 appear at the terminals k_2 to k_6 and g_2 to g_6 . Since the voltages described hereinbefore are fed to the above referred to terminals, as will be seen from Figure 7, the display element for units of seconds corresponding to the segment electrode S of Figure 2 is caused to produce a display.
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- When the periodic pulses are produced at the terminal P_2 of the timing pulse generator 10 in Figure 1A, the AND gate circuits 20, 23 are
 40 opened to permit the counted data 5 and 0 of the counters 5, 6, respectively to pass therethrough. Therefore logic 1 is produced at the terminal x_6 of the decoder 26, at the terminal y_0 of the decoder 28 and at the terminal $\bar{h}$, and further logic 0 is produced at the terminal h . Consequently logic 1 is produced at the output terminal of the gate circuit 50 of Figure 4 and the switching circuit 57 is turned ON so that voltages fed to the terminal S_0 appear at the terminal e_6 . Voltages fed to the
 50 terminal S_1 appear at the terminals e_1 to e_6 and e_7 to e_{10} . In Figure 6 voltages fed to the terminal C_0 appear at the terminals g_1 , k_1 and voltages fed to the terminal C_1 appear at the terminals g_2 to g_6 and k_2 to k_6 . As will be seen from Figure 7 the display element for minutes consists of the segment electrode M (Figure 2) connected to the terminal e_6 and the common electrodes connected to the terminals g_1 , k_1 .
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- When periodic pulses are produced at the
 60 terminal P_3 of the timing pulse generator 10, the AND gate circuits 21, 24 are opened to permit the counted data from the counters 7, 8 to pass therethrough. Consequently voltages being fed to the terminal S_0 appear at the terminal e_{10} of the segment voltage supply circuit 31, voltages being
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fed to the terminal C_0 appear at the terminal k_6 and voltages being fed to the terminal C_1 appear at the terminals k_1 to k_6 . While one pulse appears at the terminal P_3 a logic level of which becomes logic 1 and thus that on the terminal $\bar{P}_3$ is kept at logic 0, the outputs of the AND gate circuits 77 to 82 becomes logic 0. Consequently voltages being fed to the terminal C_1 appear at the terminals g_1 to g_6 . Therefore a display element for hours which comprises a segment electrode H (Figure 2) connected with the terminal e_{10} and the common electrode connected to the terminal k_6 is displayed.

- As will be apparent, the display elements
 80 corresponding to the segment electrodes H, M and S display 10 hours 5 minutes 0 seconds.

- Below is explained a time adjusting operation. When the manual switch 17 of Figure 1 is closed, the frequency divider 2 and the contents of units of seconds are reset so that the contents in the counters 3, 4 become 0. Furthermore the AND gate circuit 34 is opened to enable time adjusting pulses to pass therethrough. A logic 1 produced on the line L_6 opens the AND gate circuit 15 so that pulses produced at the terminal P_1 and the terminal P_2 of the timing pulse generator 10 appear at the terminal M_2 . Consequently the gate circuits 19, 22 are held in the closed condition, and the gate circuits 20, 23 are opened and the
 90 AND gate circuits 21, 24 are opened responsive to pulses produced at the terminal P_3 . As pulses are generated from the time adjusting pulse generator 33 by manual operation, the contents in the counters 5 to 8 are changed. Thus the hours and minutes indications are adjusted together, the seconds indication being suppressed. The effective voltage applied to the minutes indication during adjustment is greater than when it is not being adjusted.
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- Here, in the case of adjusting a time indication the gate circuits 20, 23 are opened for twice the time they are opened during normal or usual time display (i.e. when the time indication is not adjusted), so that in a time adjusting state an effective value of the voltage to be applied to the liquid crystal display device is larger by a factor of $\sqrt{2}$ to increase the speed of response of the liquid crystal display device. Therefore even if the frequency of the adjusting pulses become
 110 relatively high, the display elements for minutes will be energised or turned on.

- The control time of the AND gate circuits 20, 23 is not limited to that described hereinbefore. For example, in the case of adjusting a time indication it may be advantageous to make the effective value larger than during the usual time display by time-division controlling gate circuits for minutes and hours and keeping the gate circuits 19, 22 for seconds in a closed state.
 120 When a time indication is adjusted the contrast between display and non-display portions of the display device is noticeable and as a result it is easy to recognise the display portion being adjusted.
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Claims

1. An electronic timepiece comprising: time counting means for counting a standard time signal; selection means for selecting outputs from the said time counting means to produce the parts of a time indication; a liquid crystal display device for receiving the outputs from the said selection means to display the time indication;
- 5 time adjusting means for adjusting the contents of the said time counting means to adjust the time indication displayed by the display device; and control means for controlling the said selection means during adjustment of the time indication so that the effective voltage applied to part of the
- 10 display device when the display is being adjusted
- 15

is greater than the voltage applied when the display is not being adjusted.

2. A timepiece as claimed in claim 1 in which the display device is arranged to produce an analog display of the time indication.
- 20 3. A timepiece as claimed in claim 1 or 2 arranged so that the effective voltage applied to the part of the time display when the display is being adjusted is greater by a factor of $\sqrt{2}$ than the voltage applied when the display is not being adjusted.
- 25 4. An electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.

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