WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a substrate;

a buried oxide layer disposed on the substrate;

a silicon layer disposed on the buried oxide layer, the silicon layer including etched vertical channels extending through the silicon layer to the buried oxide layer, the silicon layer further including etched lateral channels extending only partially into the silicon layer;

an oxide material disposed on the silicon layer, the oxide material extending into the vertical channels in the silicon layer, the oxide material extending into the lateral channels in the silicon layer; and

a III-V semiconductor layer disposed on the oxide material, wherein water molecules present between the III-V semiconductor layer and the oxide material are forced during manufacturing through the vertical channels into the buried oxide layer thereby to enhance bonding between the III-V semiconductor layer and the oxide material, the lateral channels extending laterally from an interior of a periphery of the III-V semiconductor layer to an exterior of the periphery of the III-V semiconductor layer.

2. The integrated circuit of claim 1, wherein the vertical channels are positioned in a first repeating pattern across an area of the III-V semiconductor layer.

3. The integrated circuit of claim 2, wherein the lateral channels are positioned in a second repeating pattern around the periphery of the III-V semiconductor layer.

4. The integrated circuit of claim 2, wherein at least some of the vertical channels intersect at least some of the lateral channels.

5. The integrated circuit of claim 1, wherein the oxide material is applied during manufacturing, then polished during manufacturing, to form a planarized oxide layer disposed on the silicon layer.

6. The integrated circuit of claim 5, wherein:

the III-V semiconductor layer is included on a III-V semiconductor chip; and

during manufacturing, the III-V semiconductor chip is forced against the planarized oxide layer to force the water molecules through the vertical channels into the buried oxide layer.

7. The integrated circuit of claim 1, wherein, during manufacturing:

the silicon layer is etched to a first depth to form the lateral channels; and

the silicon layer is etched to a second depth, different from the first depth, to form waveguides in the silicon layer.

8. The integrated circuit of claim 1, wherein, during manufacturing:

the silicon layer is etched to a first depth to form the lateral channels and to form waveguides in the silicon layer.

9. The integrated circuit of claim 1, wherein:

the substrate is formed from silicon (Si);

the buried oxide layer is formed from silicon dioxide (SiO_2);

the oxide material is silicon dioxide; and

the III-V semiconductor layer is formed from indium phosphide (InP).

10. A method of manufacturing an integrated circuit, the method comprising:

providing a silicon-on-insulator wafer including a substrate, a buried oxide layer disposed on the substrate, and a silicon layer disposed on the buried oxide layer;

etching portions of the silicon layer to create vertical channels extending through the silicon layer to the buried oxide layer and partially etching portions of the silicon layer to create lateral channels in the silicon layer

applying an oxide material onto the silicon layer, the applied oxide material extending into the vertical channels in the silicon layer;

placing a III-V semiconductor layer in contact with the oxide material, the lateral

channels positioned such that when the III-V semiconductor layer is placed in contact with the oxide material, the lateral channels extend laterally from an interior of a periphery of the III-V semiconductor layer to an exterior of the periphery of the III-V semiconductor layer; and

forcing the III-V semiconductor layer against the oxide material to force water molecules present at an interface between the III-V semiconductor layer and the oxide material through the vertical channels into the buried oxide layer thereby to enhance bonding between the III-V semiconductor layer and the oxide material.

11. The method of claim 10, further comprising, prior to applying the oxide material:

wherein when the III-V semiconductor layer is forced against the oxide material, at least some of the water molecules present at the interface between the III-V semiconductor layer and the oxide material are forced into the lateral channels, past the periphery of the III-V semiconductor layer, and, through diffusion, out of the oxide material into an atmosphere surrounding the periphery of the III-V semiconductor layer and adjacent the oxide material.

12. The method of claim 11, wherein, when the III-V semiconductor layer is placed in contact with the oxide material:

the vertical channels are positioned in a first repeating pattern across an area of the III-V semiconductor layer; and

the lateral channels are positioned in a second repeating pattern around the periphery of the III-V semiconductor layer.

13. The method of claim 11, wherein at least some of the vertical channels intersect at least some of the lateral channels.

14. The method of claim 11, further comprising, prior to applying the oxide material:

partially etching portions of the silicon layer to create waveguides in the silicon layer.

15. The method of claim 14, wherein:

the silicon layer is etched to a first depth to form the lateral channels; and

the silicon layer is etched to a second depth, different from the first depth, to form waveguides in the silicon layer.

16. The method of claim 15, wherein the silicon layer is etched to a first depth to form the lateral channels and the waveguides in the silicon layer.

17. The method of claim 10, further comprising, after applying the oxide material and prior to placing the III-V semiconductor layer in contact with the oxide material:

polishing the oxide material to form a planarized oxide layer disposed on the silicon layer, wherein the III-V semiconductor layer is placed in contact with the planarized oxide layer.

18. The method of claim 10, wherein:

the III-V semiconductor layer is placed in contact with the oxide material layer at room temperature; and

the III-V semiconductor layer is forced against the oxide material at ambient pressure and at a temperature greater than room temperature.

19. The method of claim 10, wherein:

the III-V semiconductor layer is placed in contact with the oxide material layer at room temperature; and

the III-V semiconductor layer is forced against the oxide material in a vacuum and at a temperature greater than room temperature.

20. An integrated circuit, comprising:

a substrate;

a buried oxide layer disposed on the substrate;

a silicon layer disposed on the buried oxide layer, the silicon layer including etched vertical channels extending through the silicon layer to the buried oxide layer, the silicon layer including etched lateral channels extending only partially into the silicon layer;

a planarized oxide layer disposed on the silicon layer, the planarized oxide layer formed

from an oxide material that extends into the vertical channels and the lateral channels in the silicon layer; and

a III-V semiconductor layer disposed on the oxide material, the lateral channels extending laterally from an interior of a periphery of the III-V semiconductor layer to an exterior of the periphery of the III-V semiconductor layer, the vertical channels being positioned in a first repeating pattern across an area of the III-V semiconductor layer, the lateral channels being positioned in a second repeating pattern around the periphery of the III-V semiconductor layer,

wherein at least some water molecules present between the III-V semiconductor layer and the oxide material are forced during manufacturing through the vertical channels into the buried oxide layer thereby to enhance bonding between the III-V semiconductor layer and the oxide material, and

wherein at least some water molecules present between the III-V semiconductor layer and the oxide material are forced during manufacturing into the lateral channels, past the periphery of the III-V semiconductor layer, and, through diffusion, out of the oxide material into an atmosphere surrounding the periphery of the III-V semiconductor layer and adjacent the oxide material.