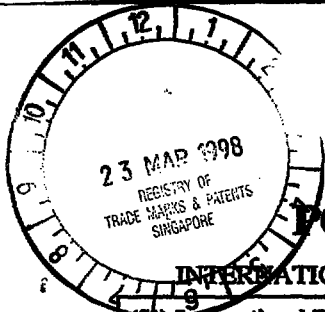


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08/235,591**29 April 1994 (29.04.94)****US**(71) Applicant (for **AT BE CH DE DK ES FR GB GR IE IT JP KR LU MC NL PT SE** only): **TEXAS INSTRUMENTS INCORPORATED [US/US]; 13500 North Central Expressway, Dallas, TX 75265 (US).**(71) Applicant (for **SG** only): **TEXAS INSTRUMENTS LIMITED [GB/GB]; Manton Lane, Bedford MK41 7PA (GB).**(72) Inventors: **DORNEY, Timothy, Dominic; Apartment 1006, 8330 El Mundo Street, Houston, TX 77054 (US). BALISTRERI, Anthony, Michael; 4203 Canterbury Court, Sugar Land, TX 77479 (US).**(74) Agents: **BLANCO WHITE, Henry, Nicholas et al.; Abel & Inmray, Northumberland House, 303-306 High Holborn, London WC1V 7LH (GB).**(81) Designated States: **JP, KR, SG, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).****Published***With international search report.**Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.*

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②. IPR + Annexes

(54) Title: **A METHOD AND APPARATUS FOR TESTING A MEMORY CIRCUIT WITH PARALLEL BLOCK WRITE OPERATION**

(57) Abstract

An integrated circuit memory device (21) includes plural input/output pins (30, 127 and others) and plural arrays of addressable storage cells (31-46). A set of circuits (51, 68, 70, 71-86, 90) provides access to a unique storage location in each array (31-46) through a given row and column address. A writing circuit (47, 68, 70, 71-86, 91-106, 131-146), designed for test, provides in parallel plural copies of a test data bit. The test data bit is applied through a single pin (30) and a common data-in lead (68), for storage in an addressed storage cell in each of the arrays. A readout circuit (110, 111, 112, 171, 127, 201-216, 131-146) is arranged for reading out the stored test data bit from the addressed storage cell in each of the arrays (31-46). The writing circuit, while in a block write test mode, stores the test data bit on the common data-in lead (68) in a block of address locations in each array (31-46).

