

FIG. 1

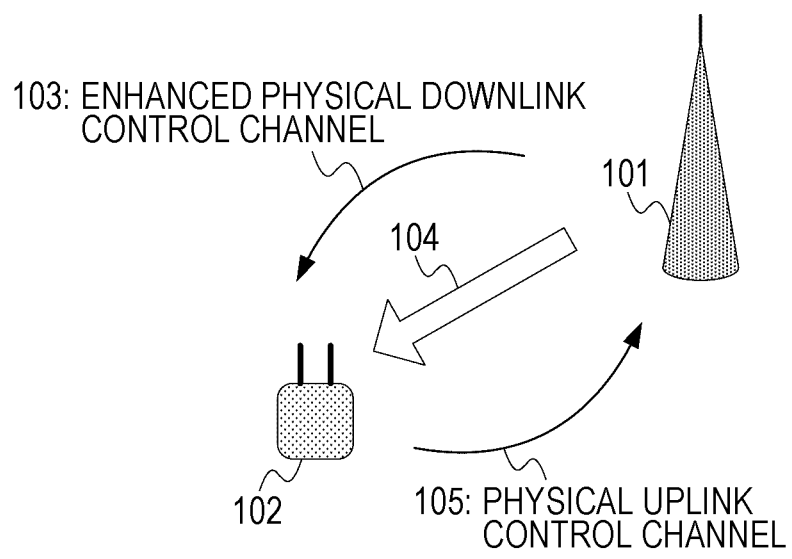


FIG. 2

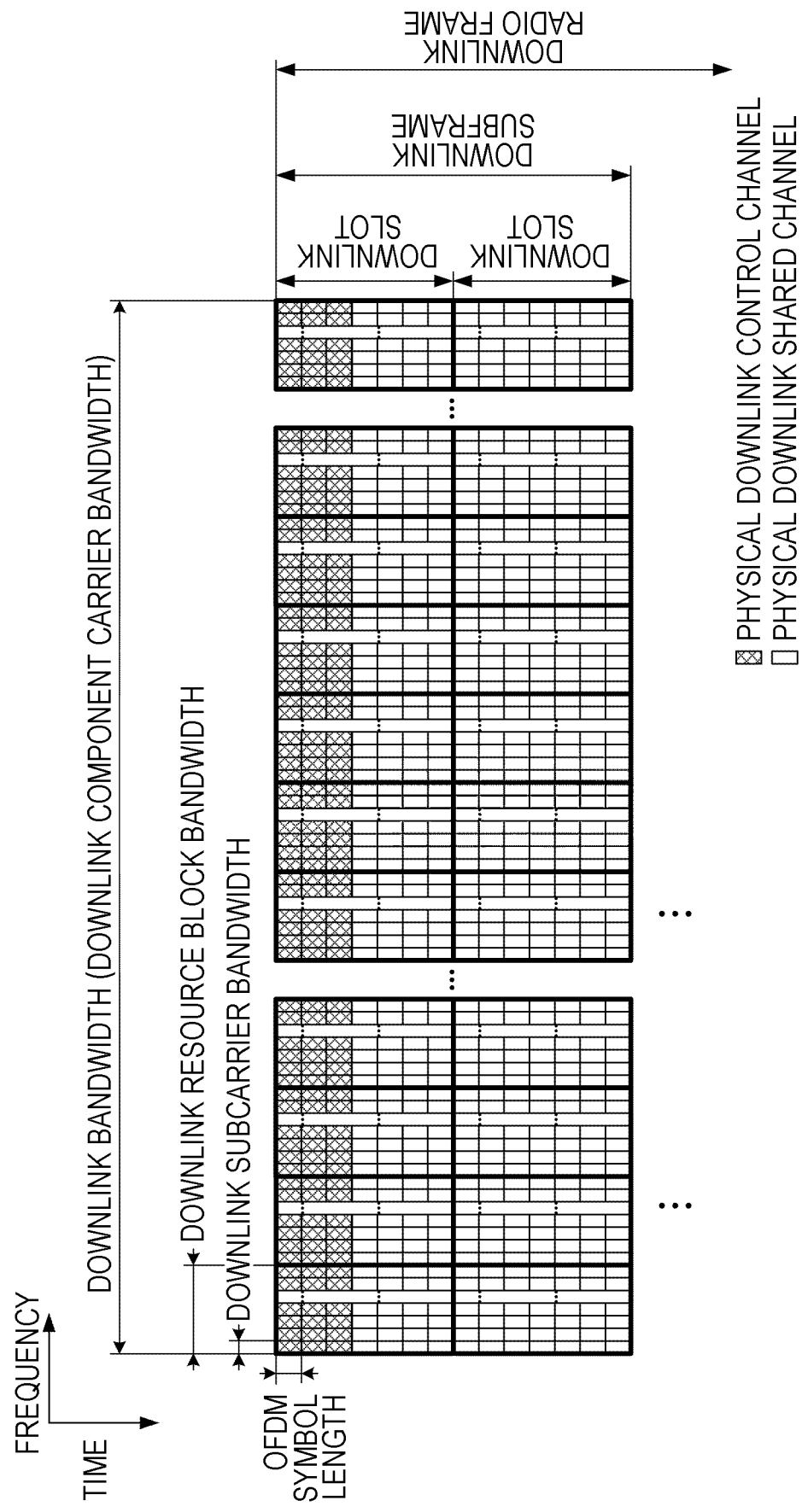


FIG. 3

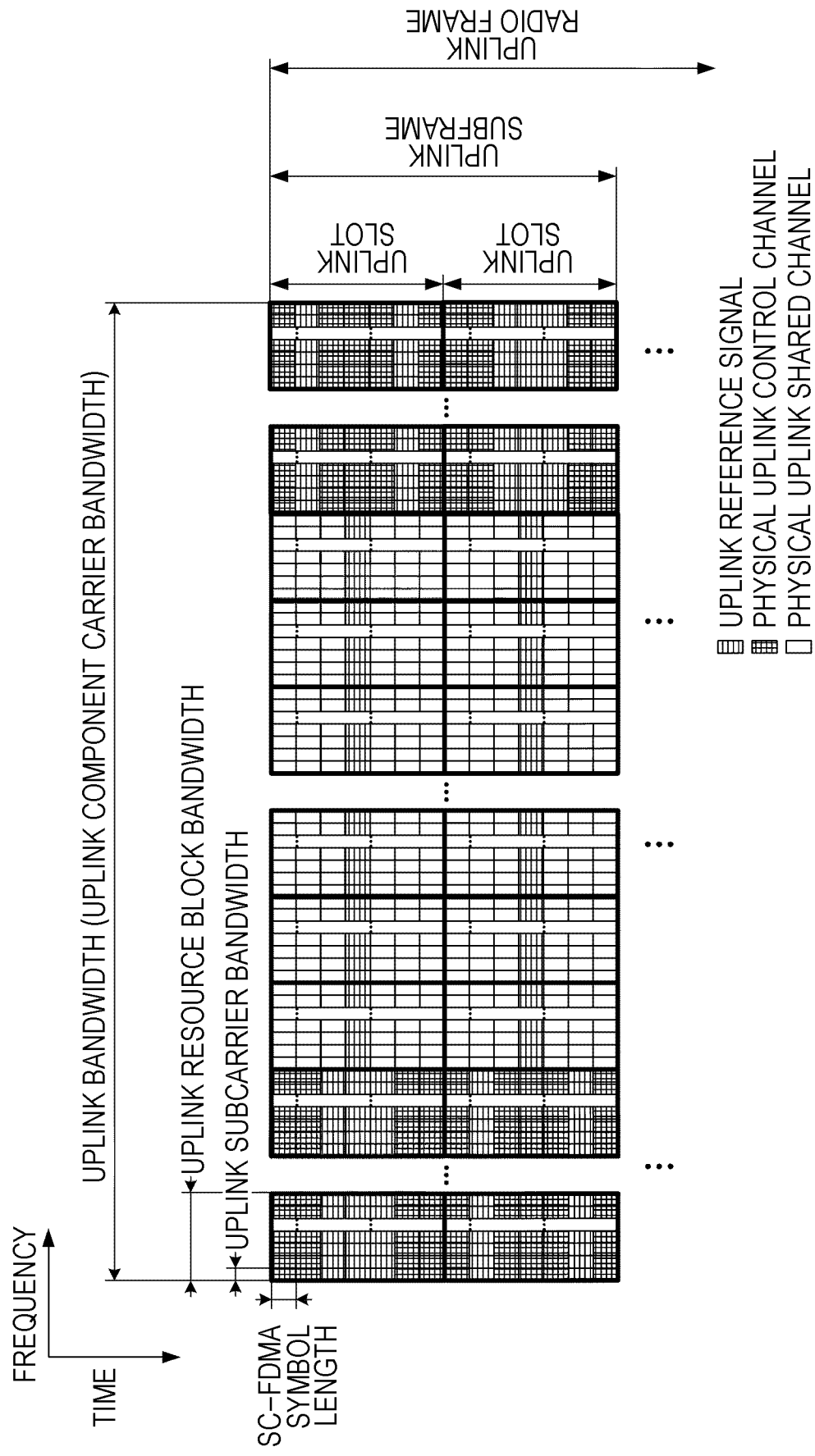


FIG. 4

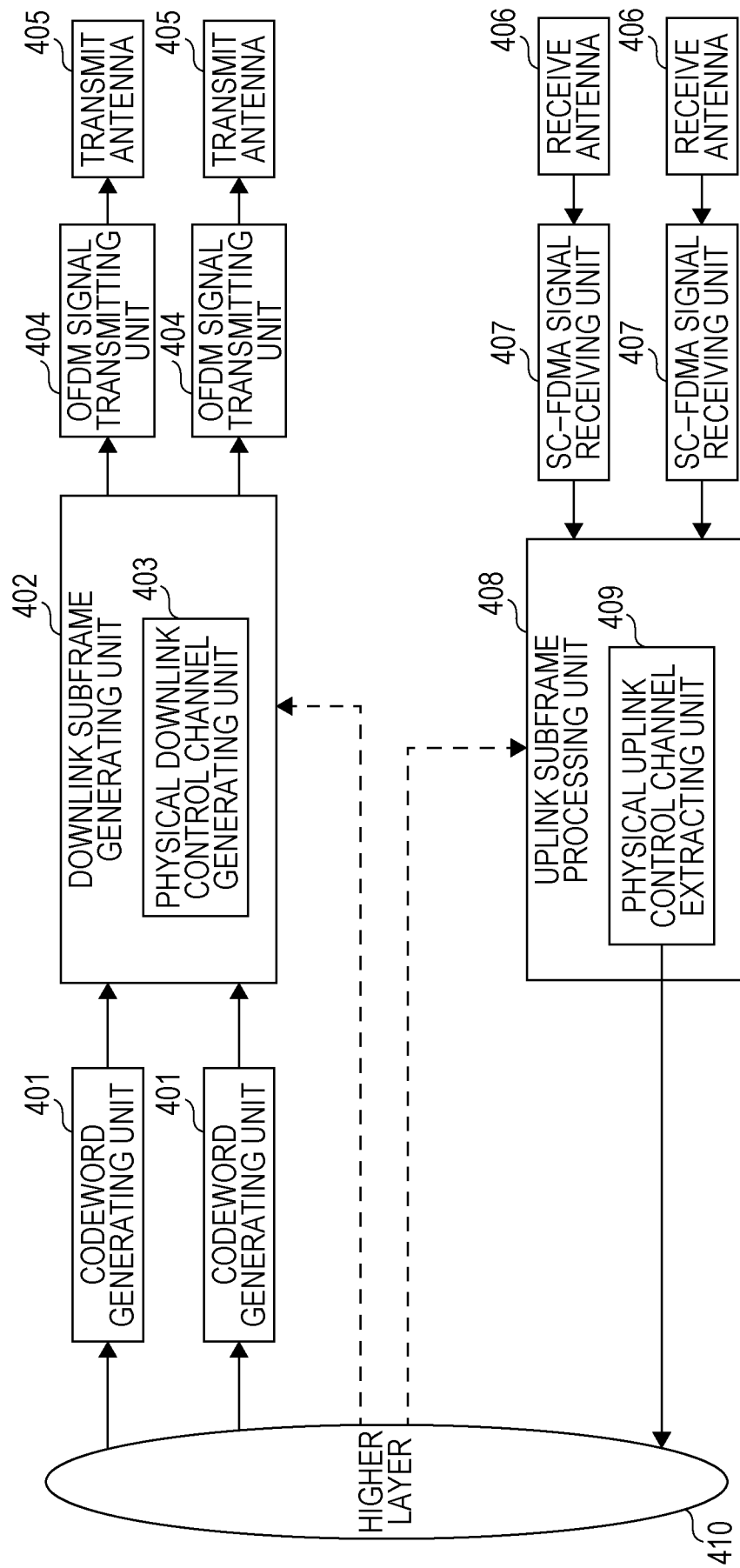


FIG. 5

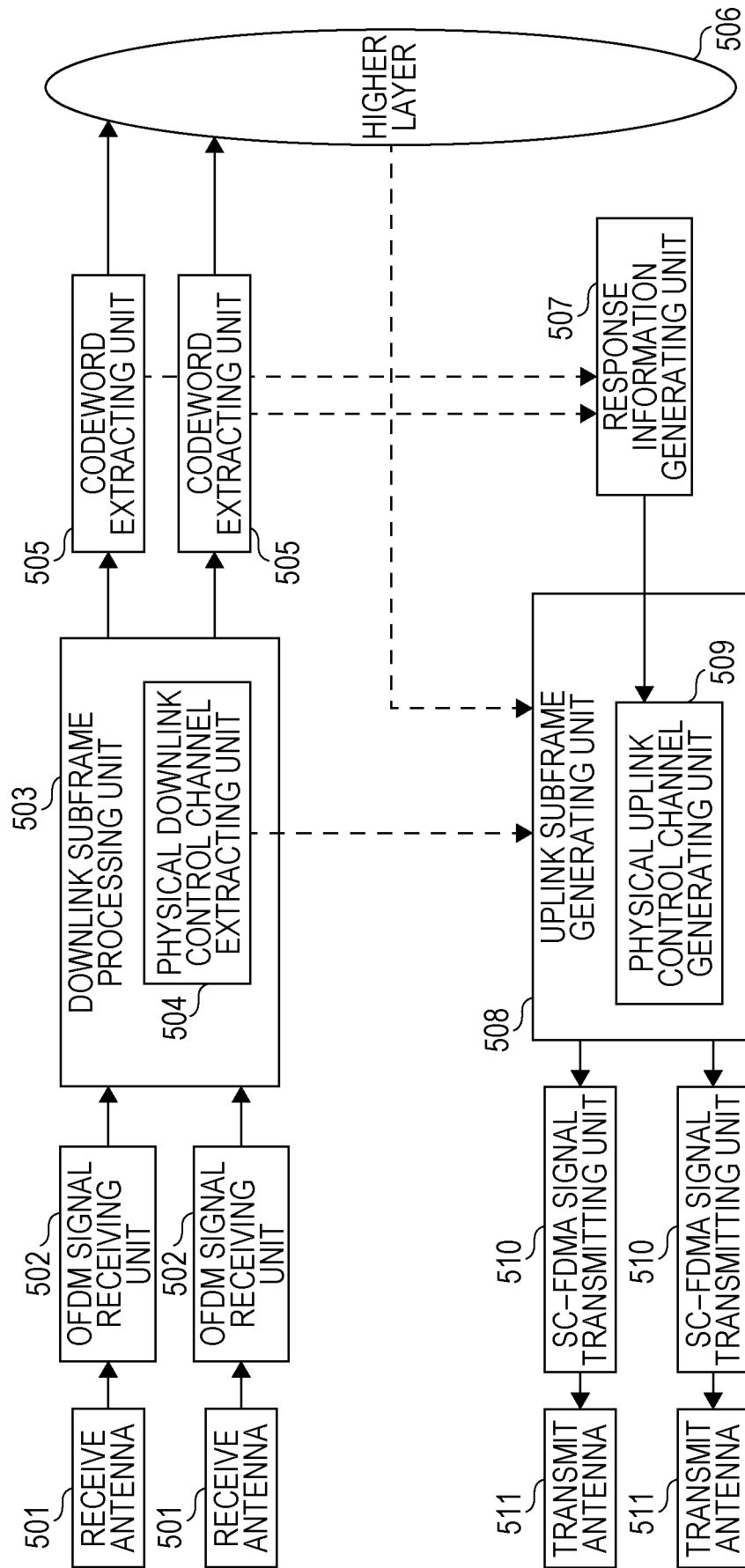


FIG. 6

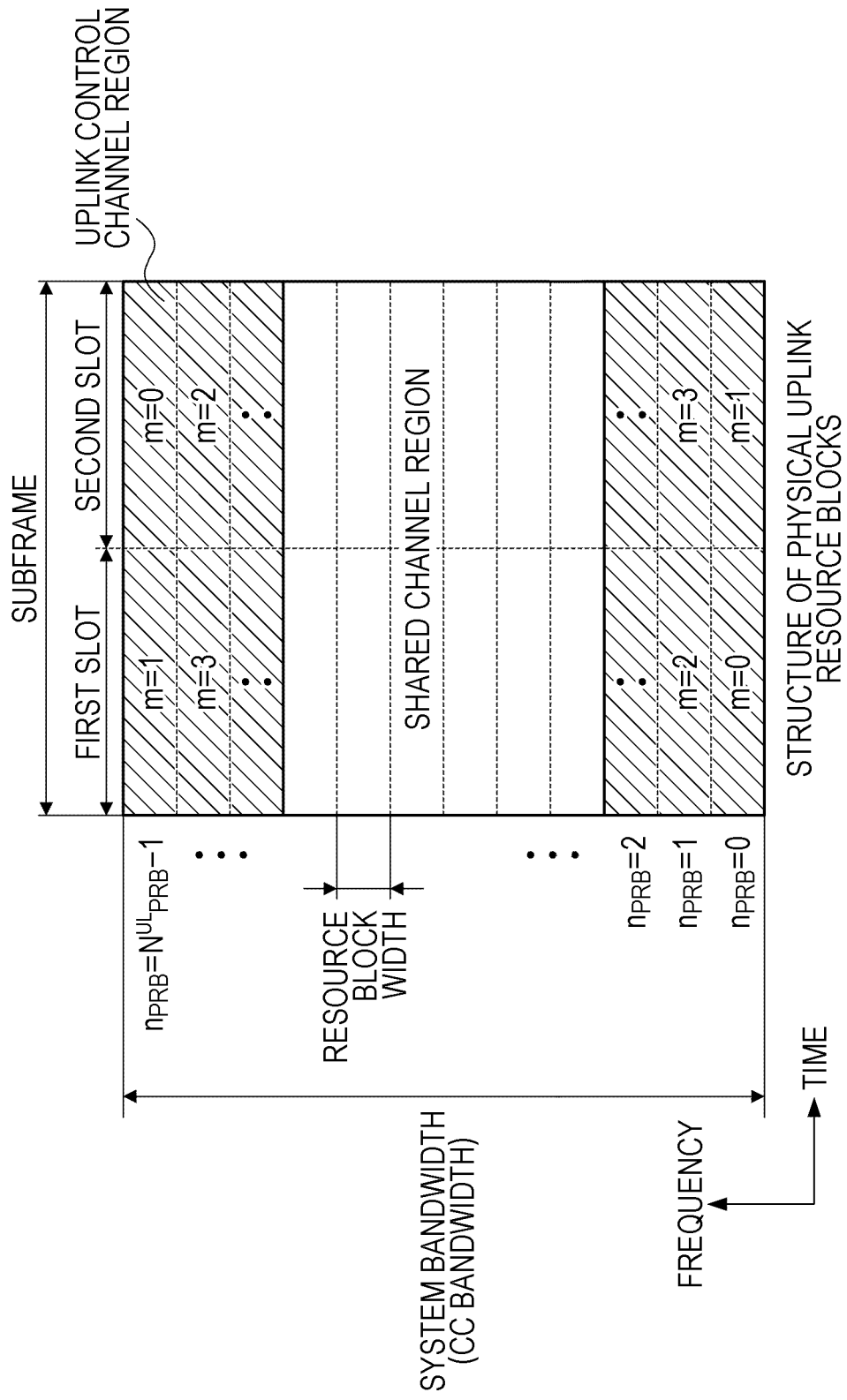


FIG. 7

UPLINK CONTROL CHANNEL LOGICAL RESOURCES

n_{PUCCH}	ORTHOGONAL CODE	CYCLIC SHIFT	m
0	OC0	CS0	N_{F2}
1	OC1	CS0	N_{F2}
2	OC2	CS0	N_{F2}
3	OC0	CS2	N_{F2}
4	OC1	CS2	N_{F2}
5	OC2	CS2	N_{F2}
$\vdots$	$\vdots$	$\vdots$	$\vdots$
15	OC0	CS10	N_{F2}
16	OC1	CS10	N_{F2}
17	OC2	CS10	N_{F2}
18	OC0	CS0	$N_{F2}+1$
19	OC1	CS0	$N_{F2}+1$
20	OC2	CS0	$N_{F2}+1$
$\vdots$	$\vdots$	$\vdots$	$\vdots$

FIG. 8

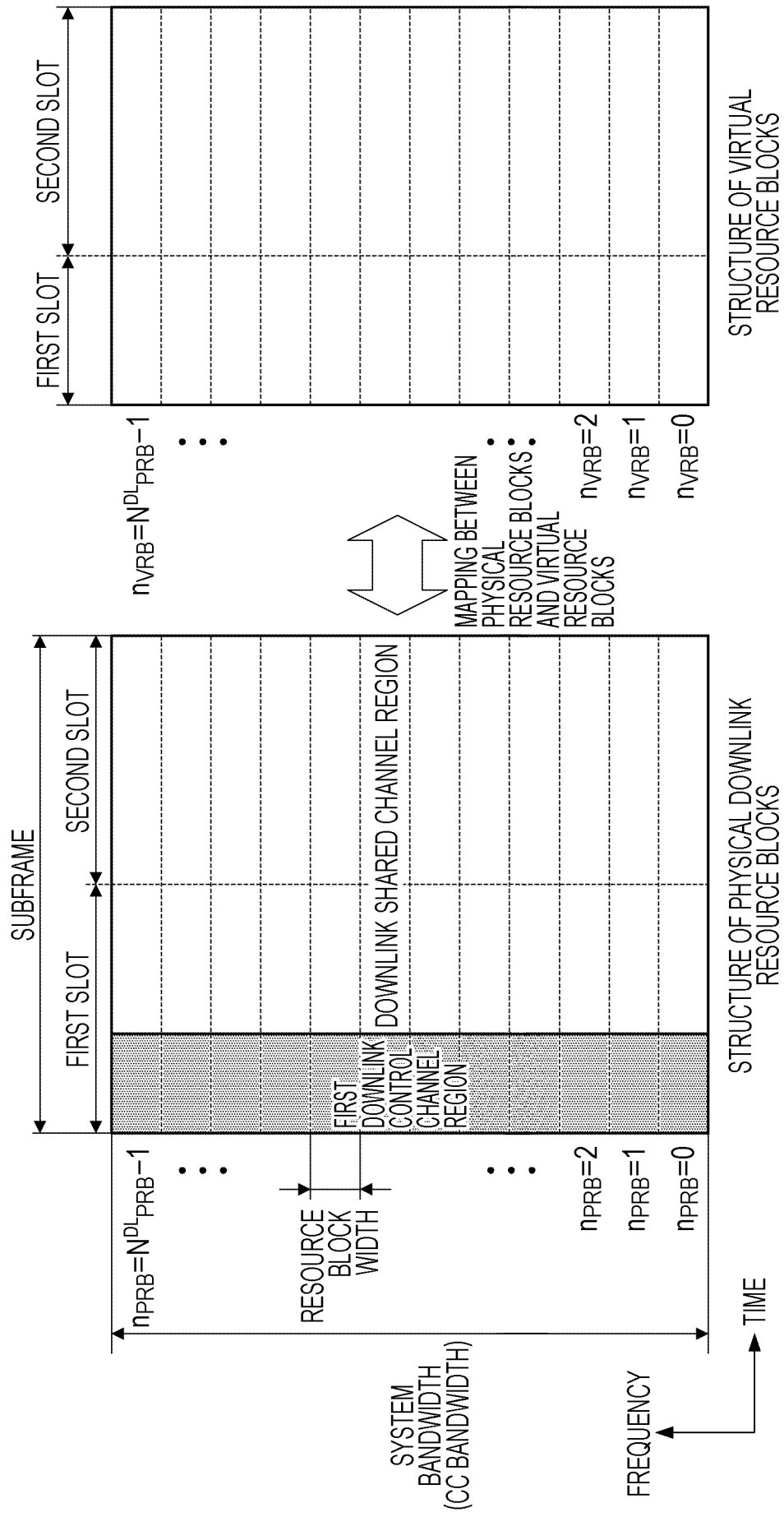


FIG. 9

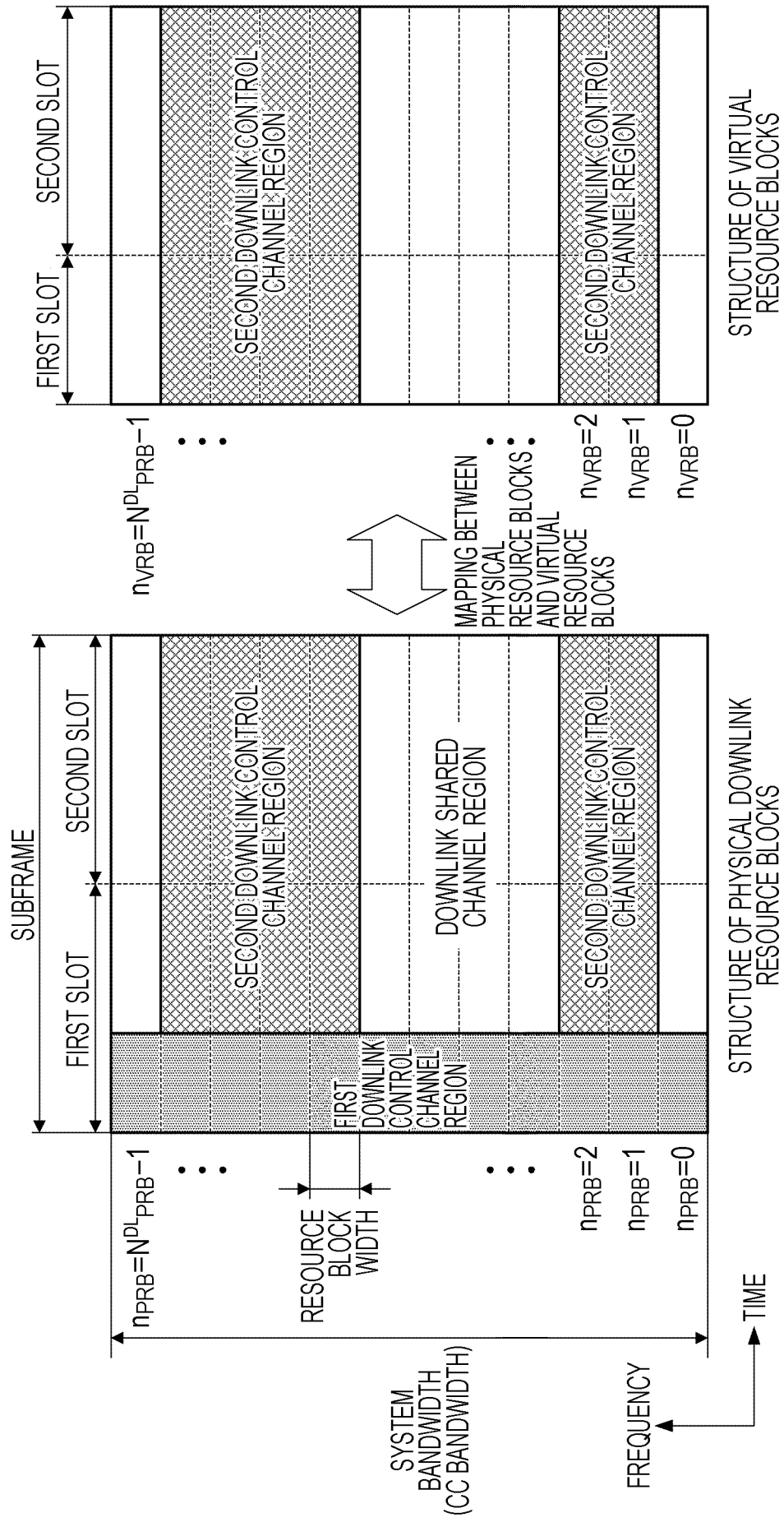


FIG. 10

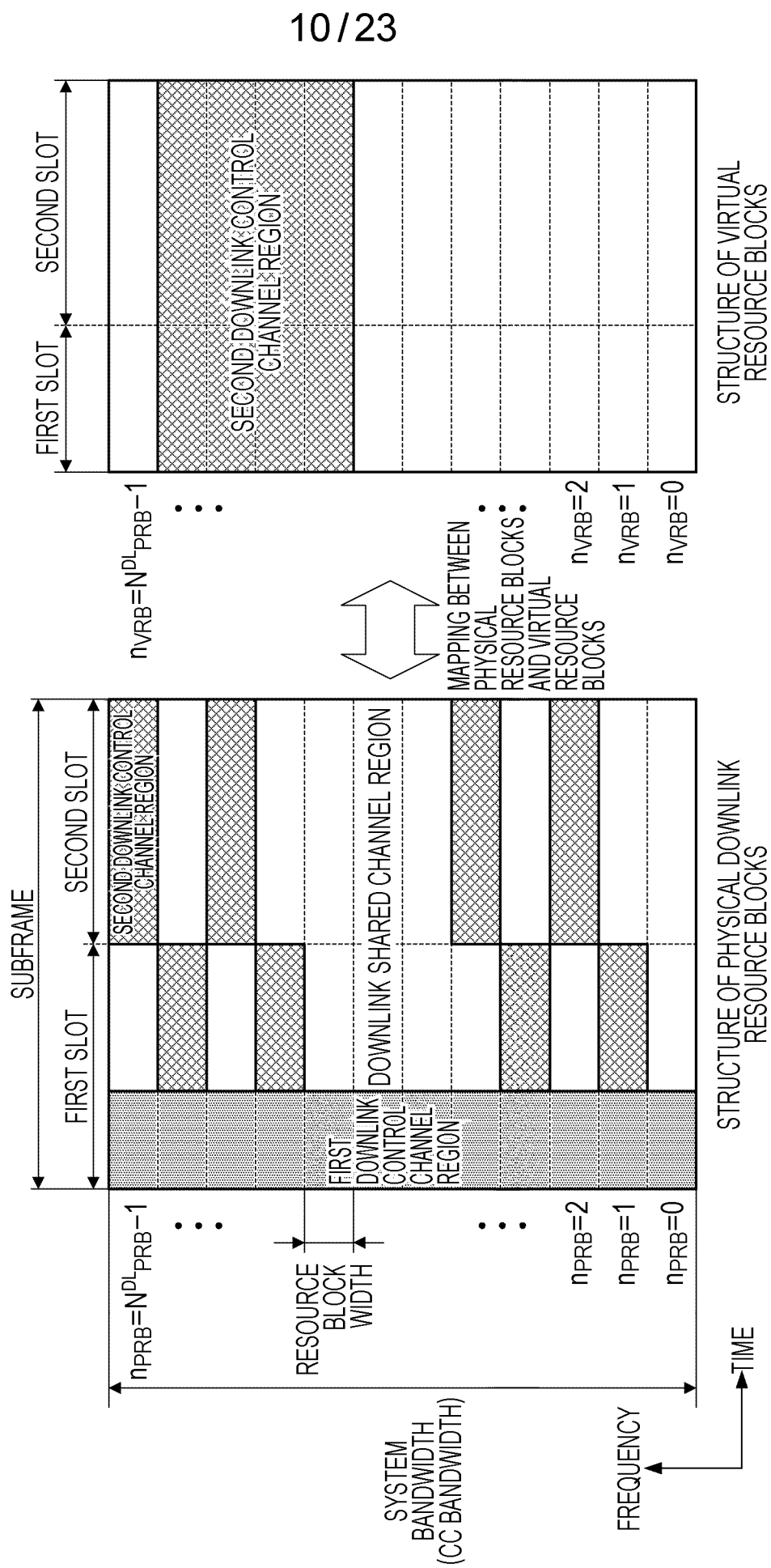


FIG. 11

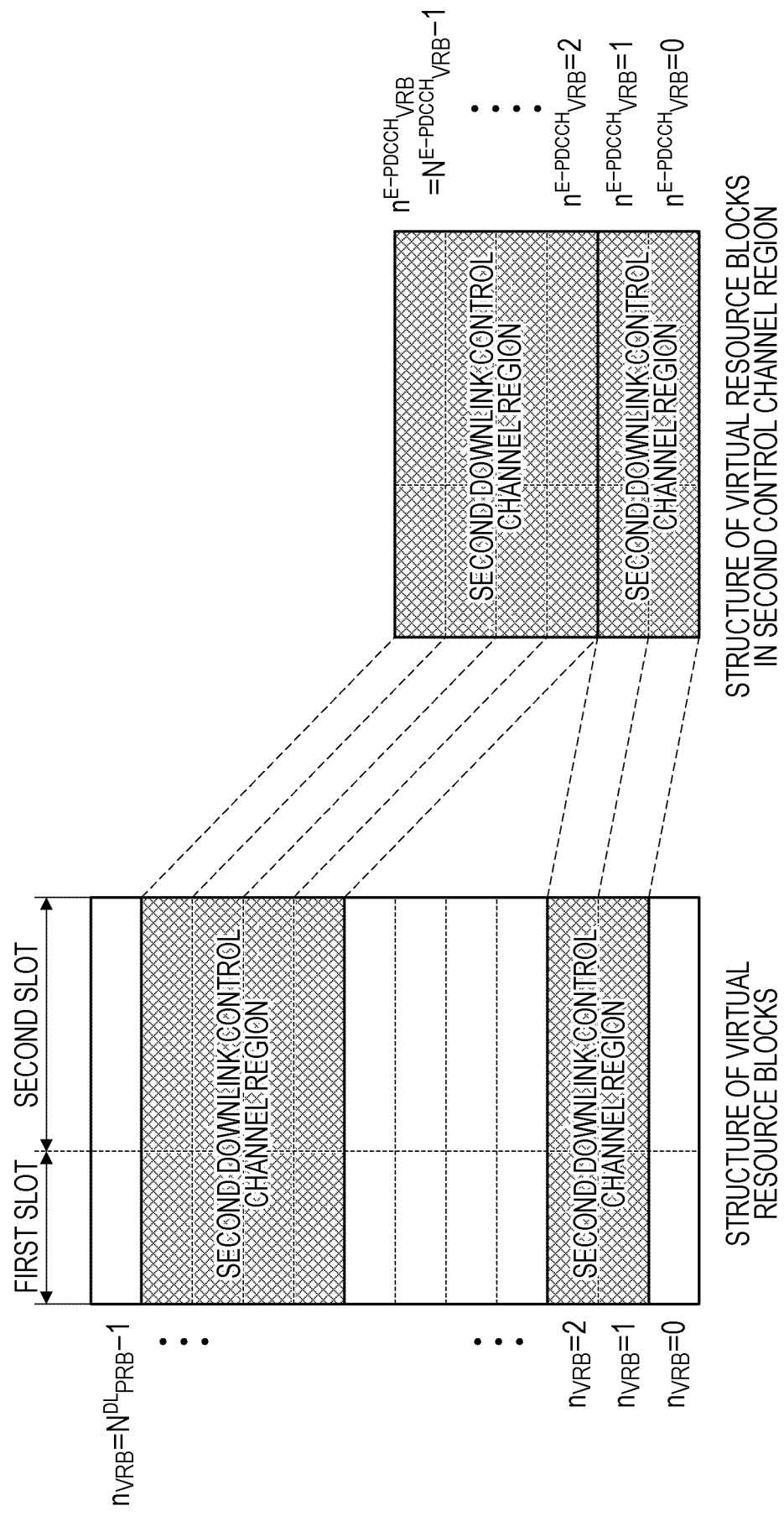


FIG. 13

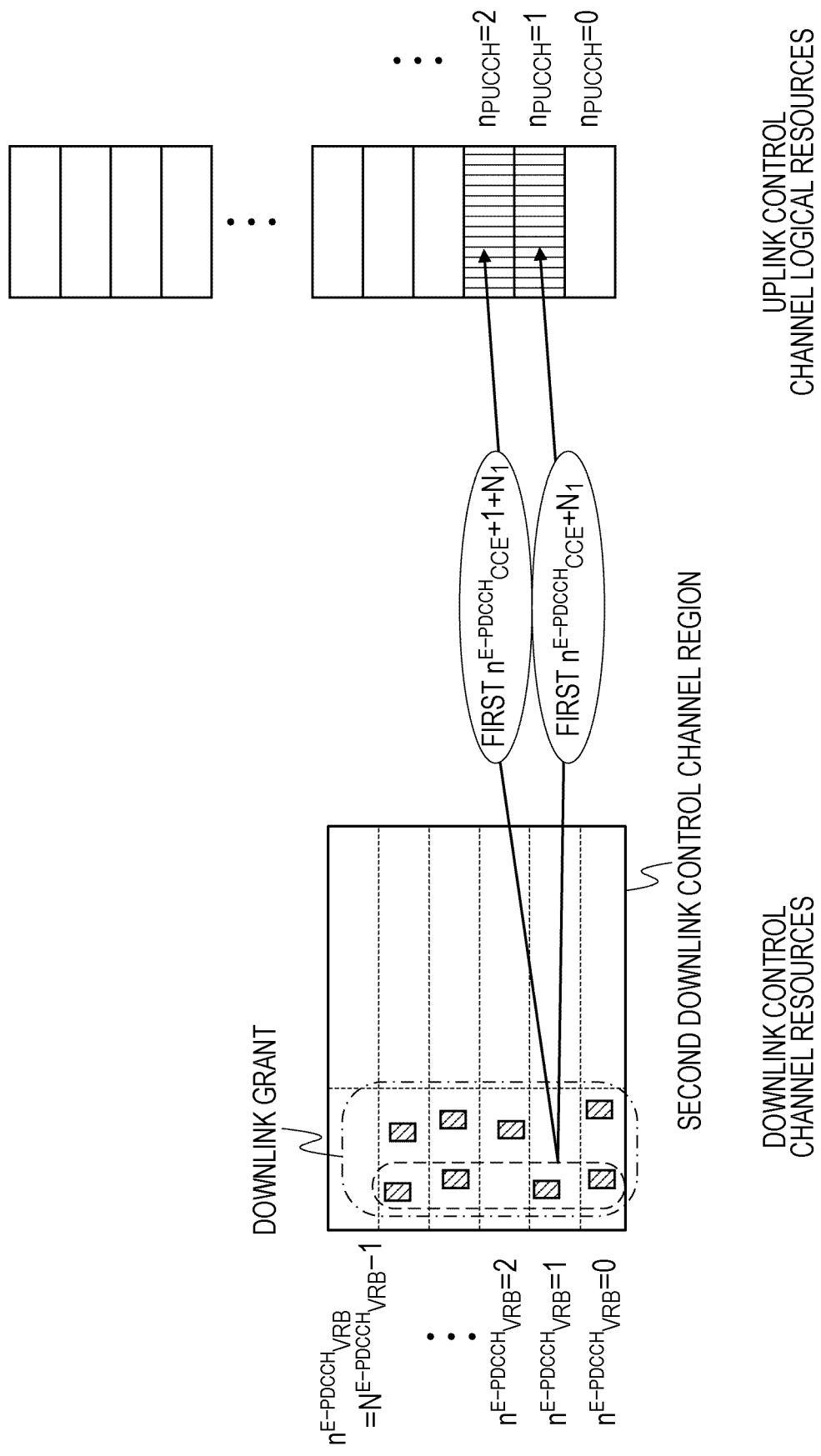


FIG. 14

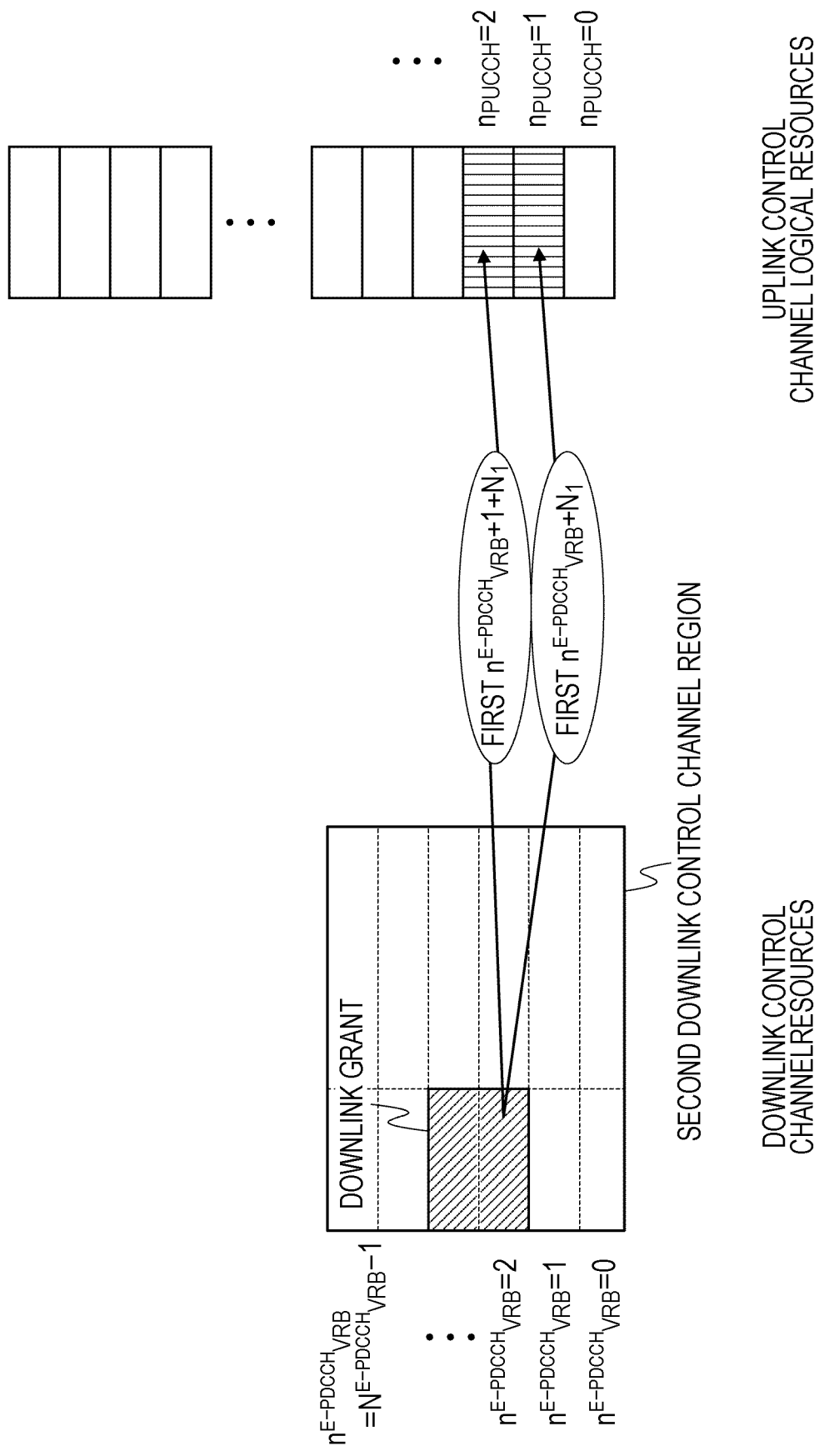


FIG. 15

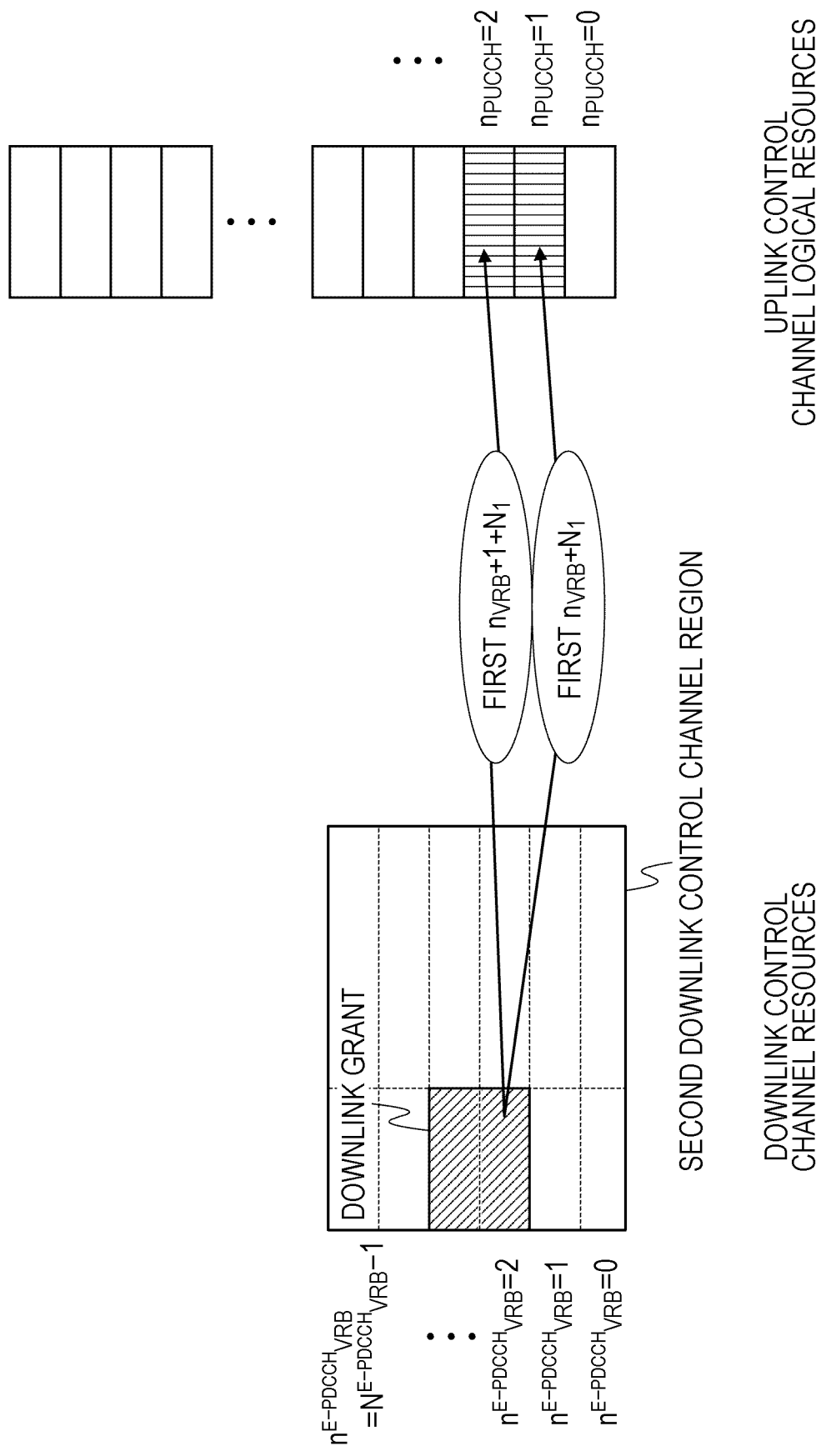


FIG. 16

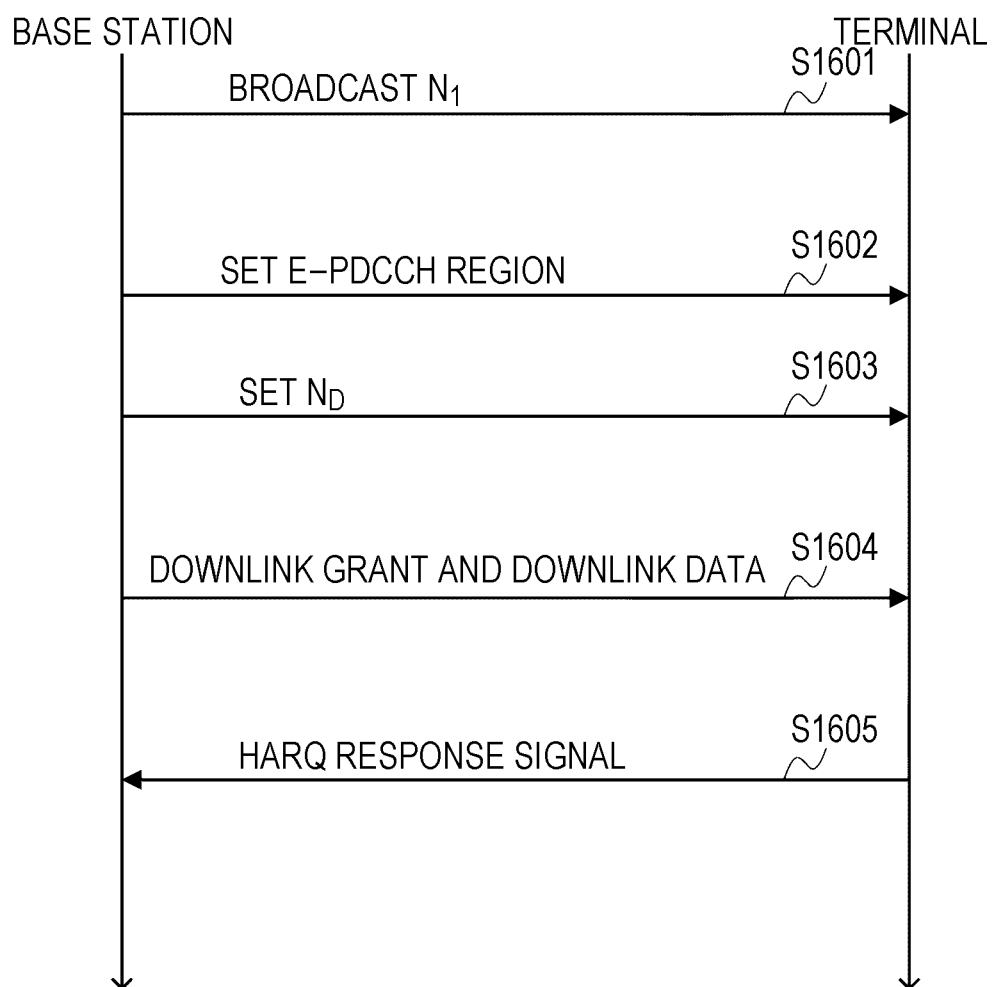


FIG. 17

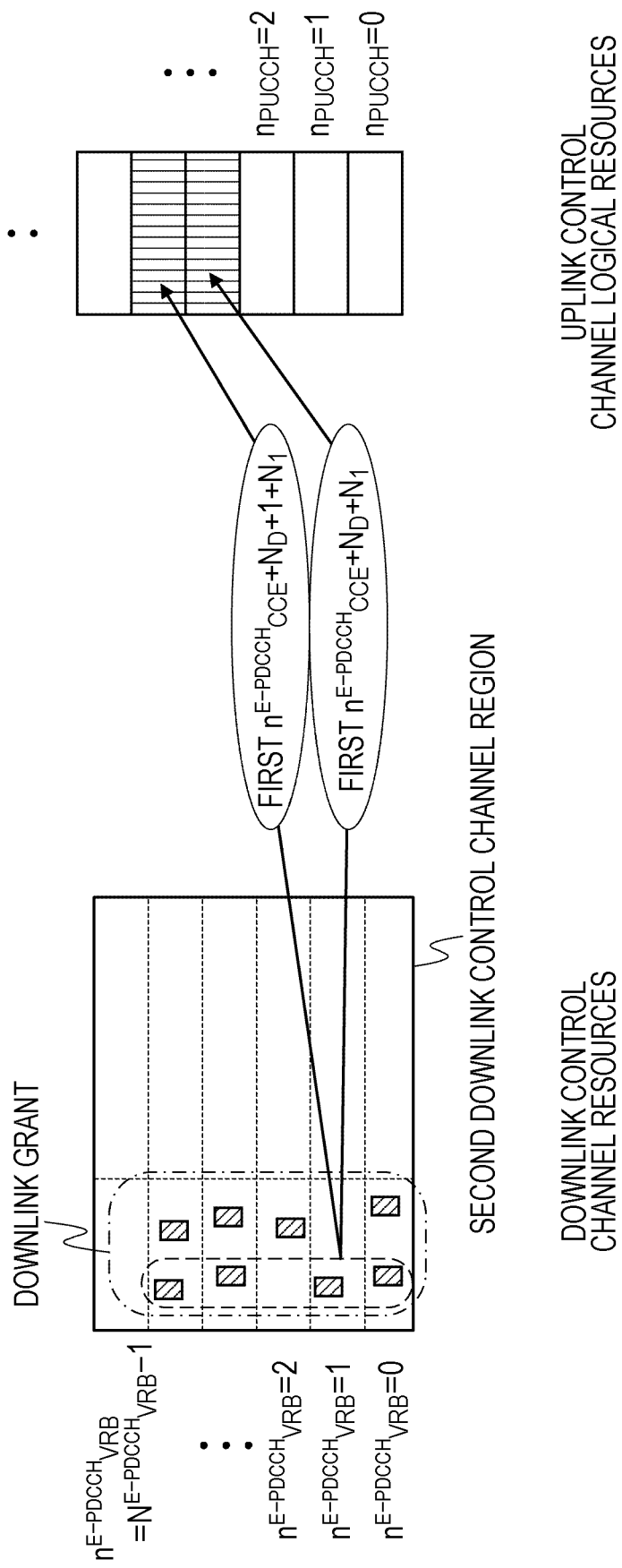


FIG. 18

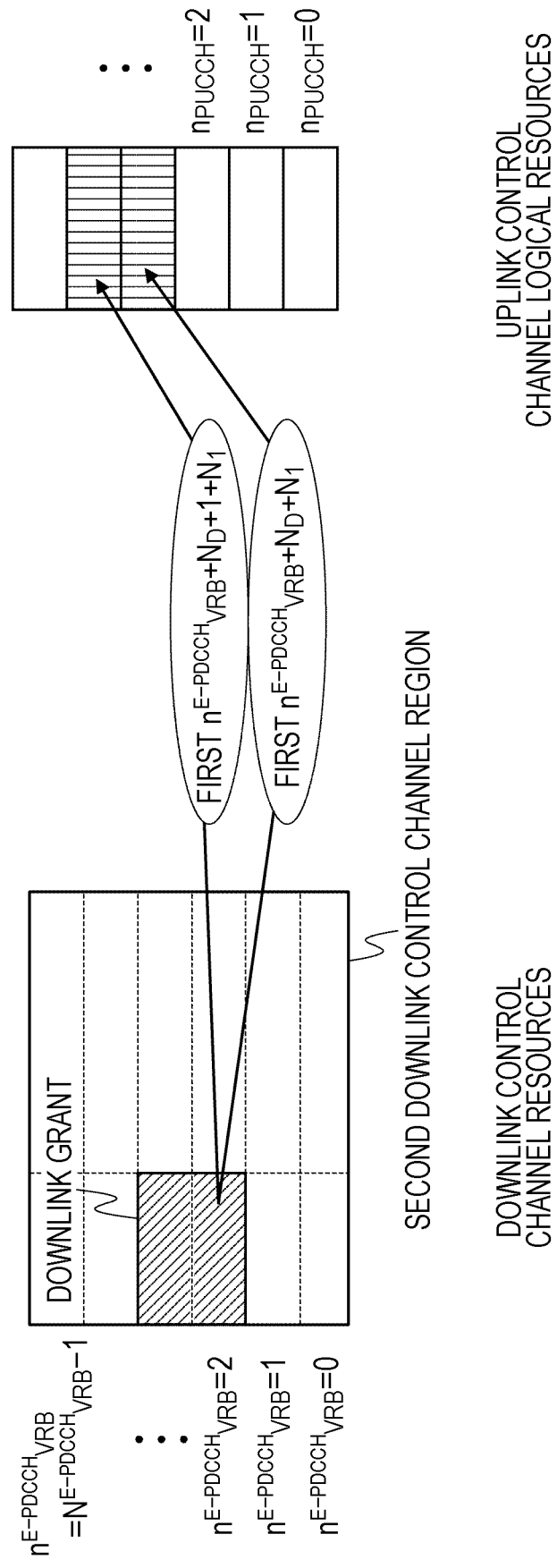


FIG. 19

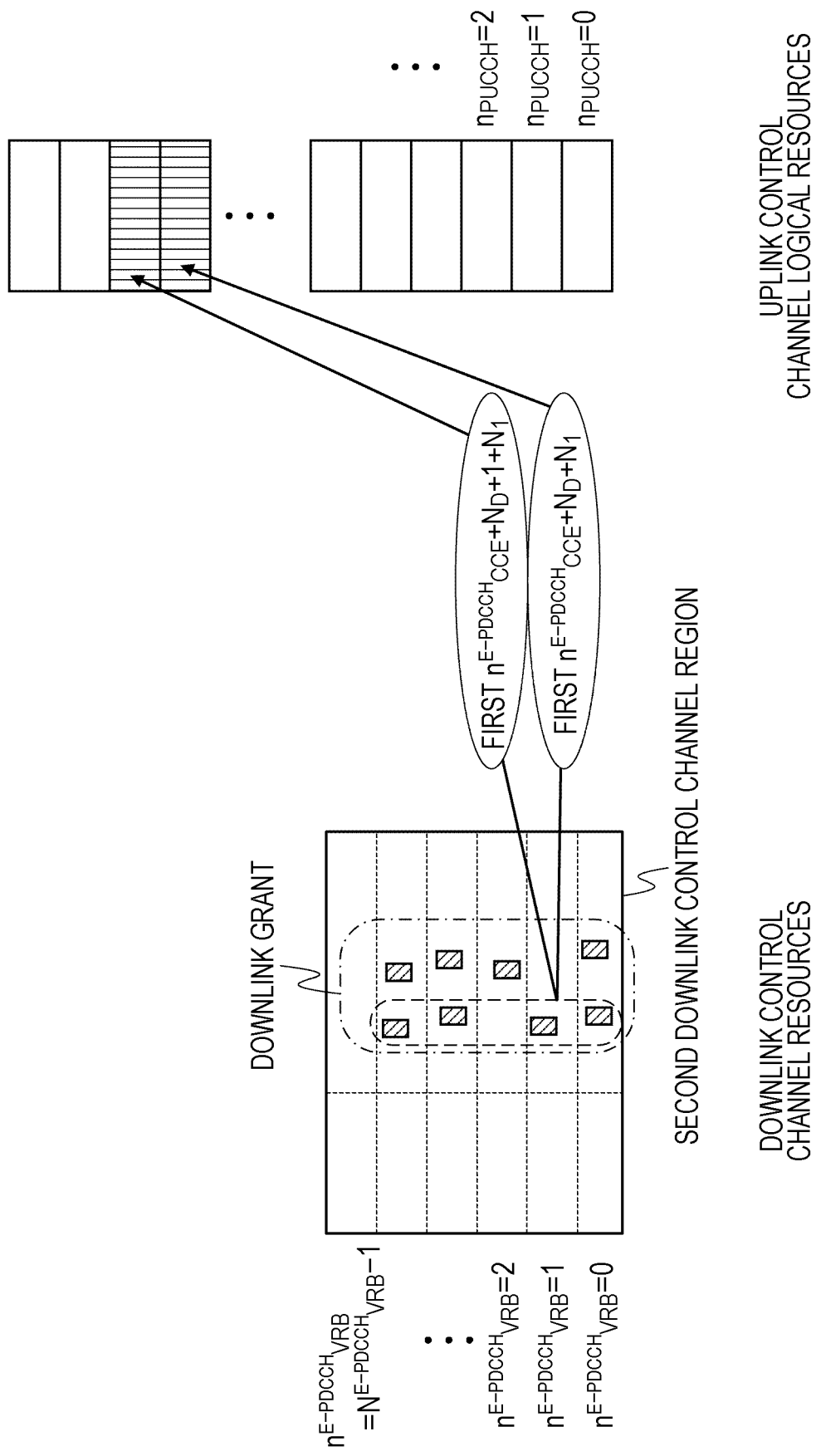


FIG. 20

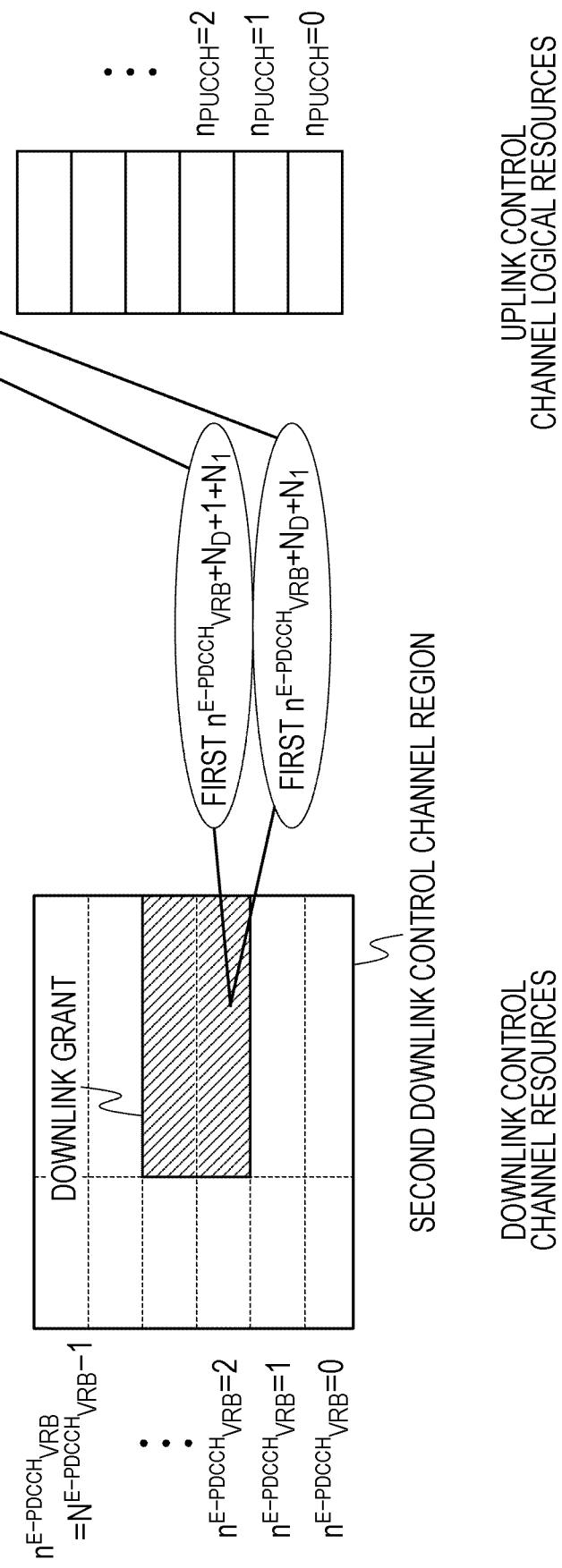


FIG. 21

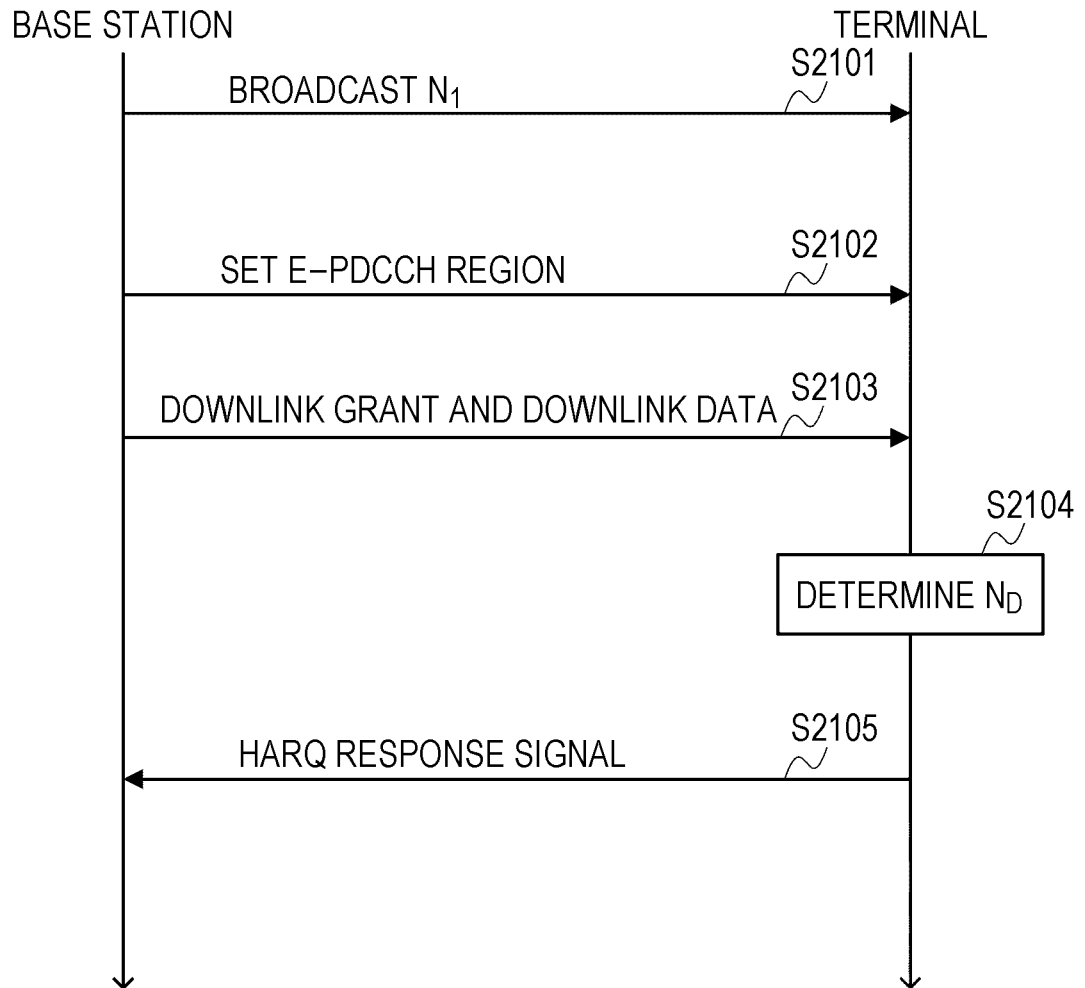


FIG. 22

SLOT NUMBER	N_D
EVEN NUMBER (FIRST SLOT)	A
ODD NUMBER (SECOND SLOT)	B

FIG. 23

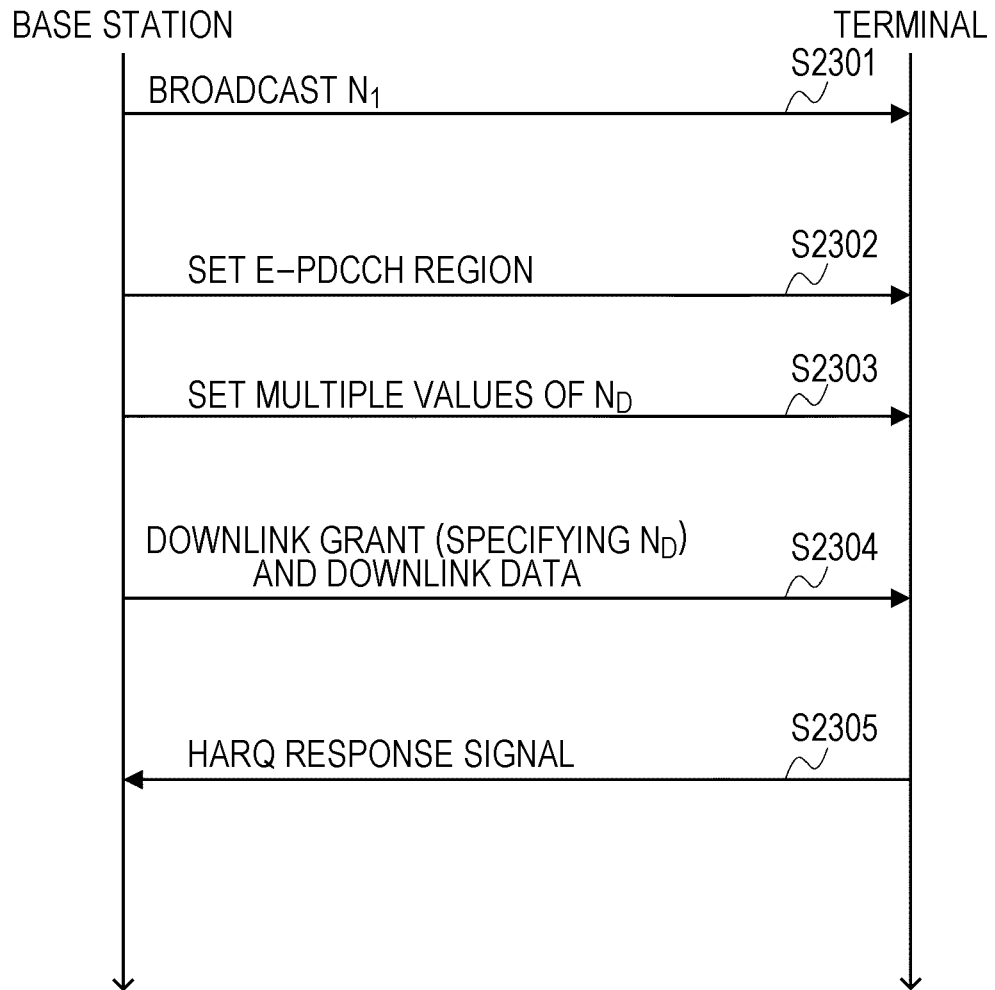


FIG. 24

INDEX	N_D
0	A
1	B
2	C
3	D

FIG. 25

