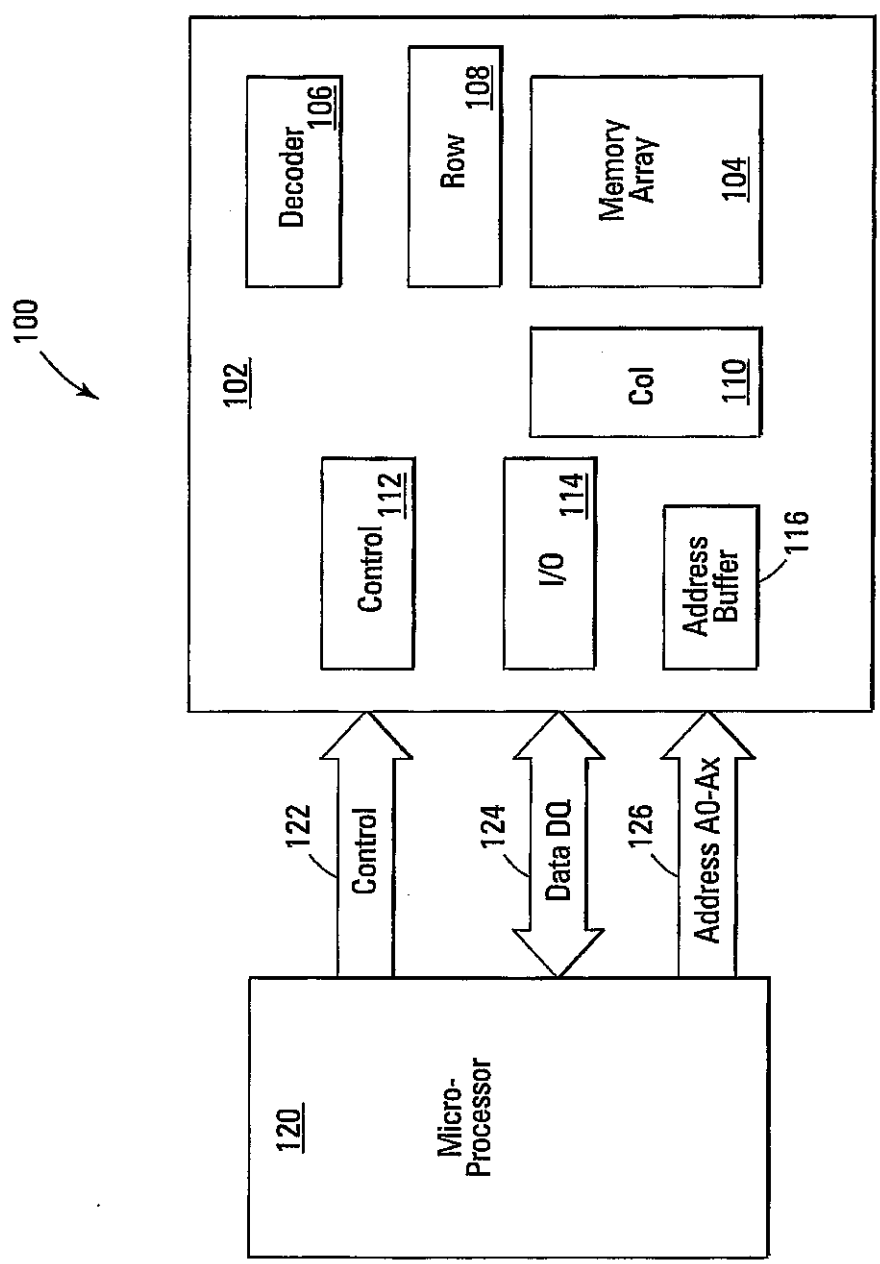

100
102
Decoder 106
Row 108
Memory Array 104
Col 110
Control 112
I/O 114
Address Buffer
116
122
Control
124
Data DQ
126
Address A0-Ax
120
Micro-Processor

Fig. 1

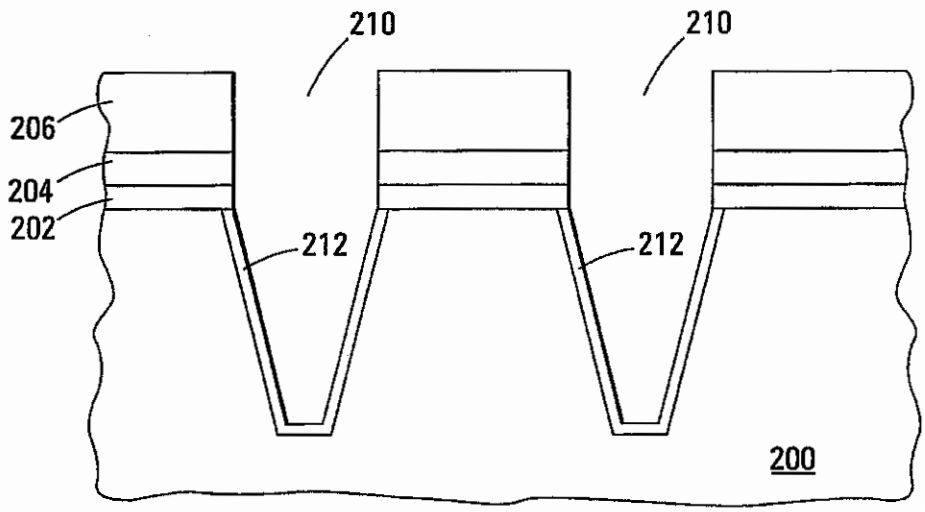

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Fig. 2A

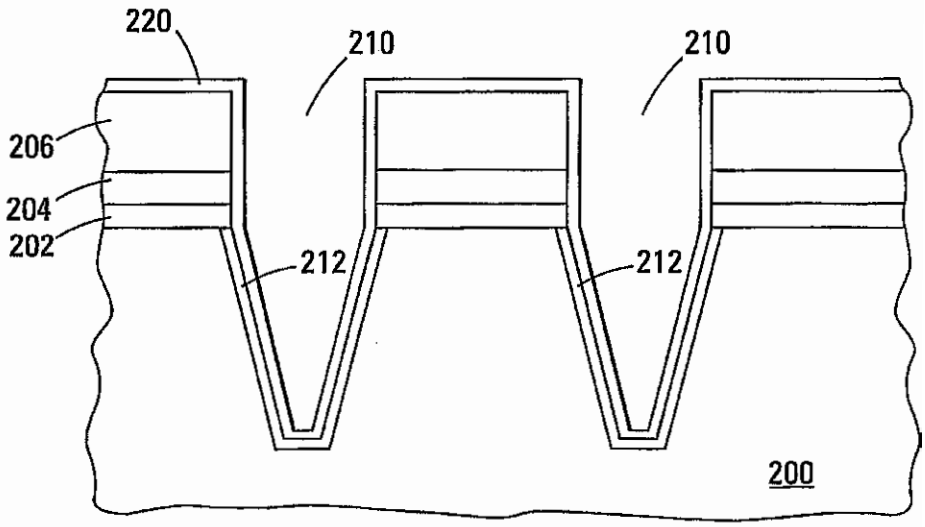

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Fig. 2B

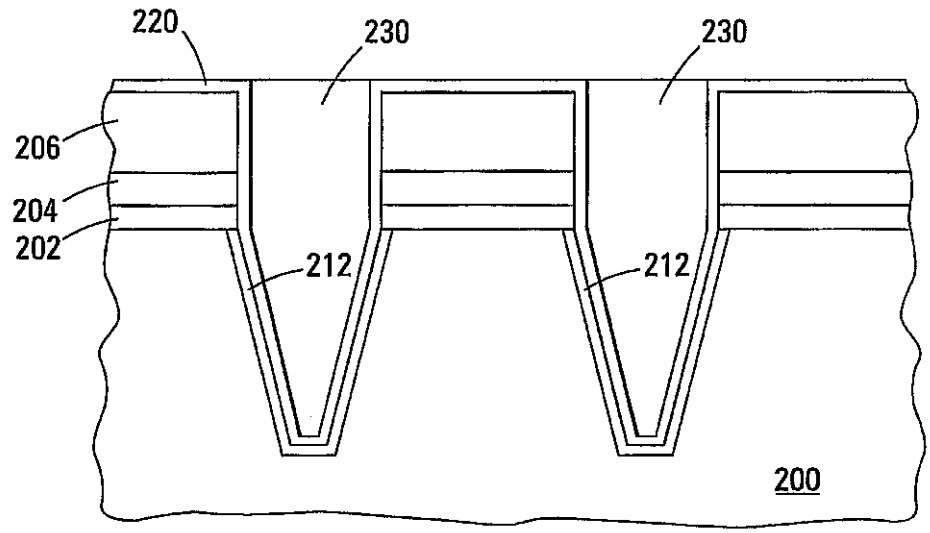

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Fig. 2C

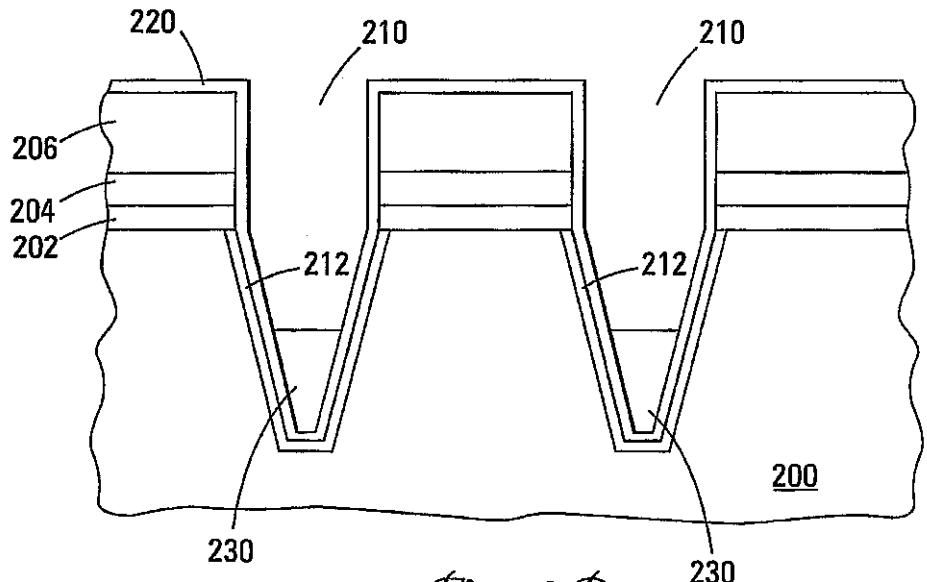

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Fig. 2D

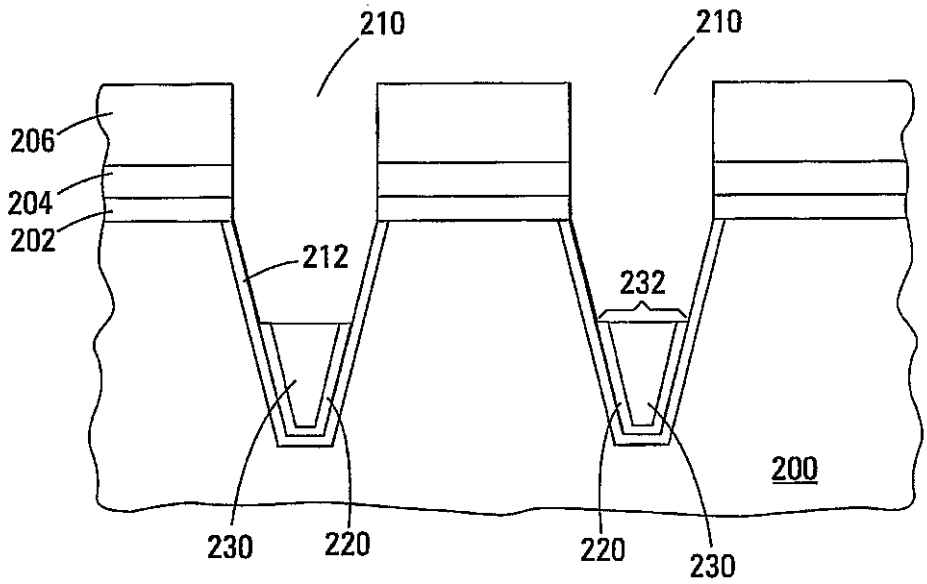

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Fig. 2E

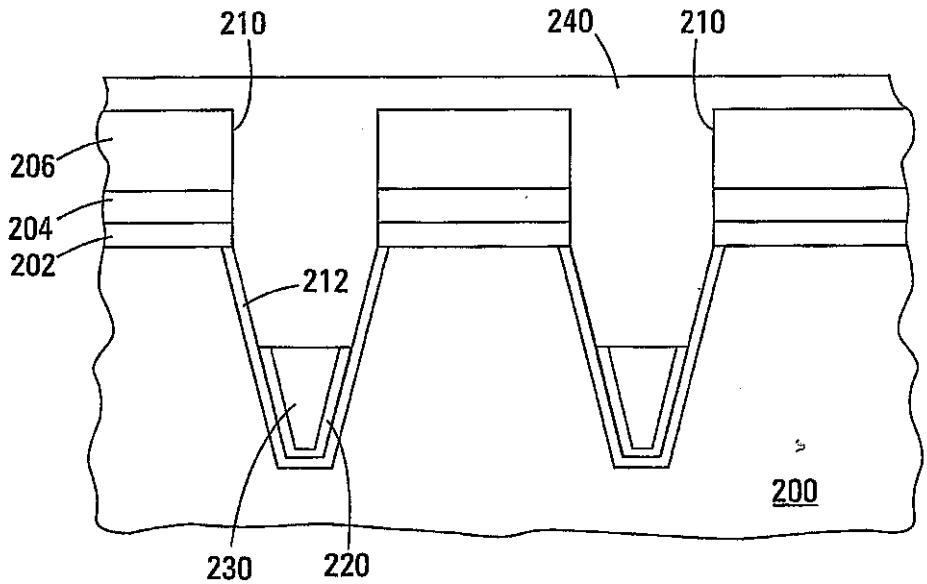

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Fig. 2F

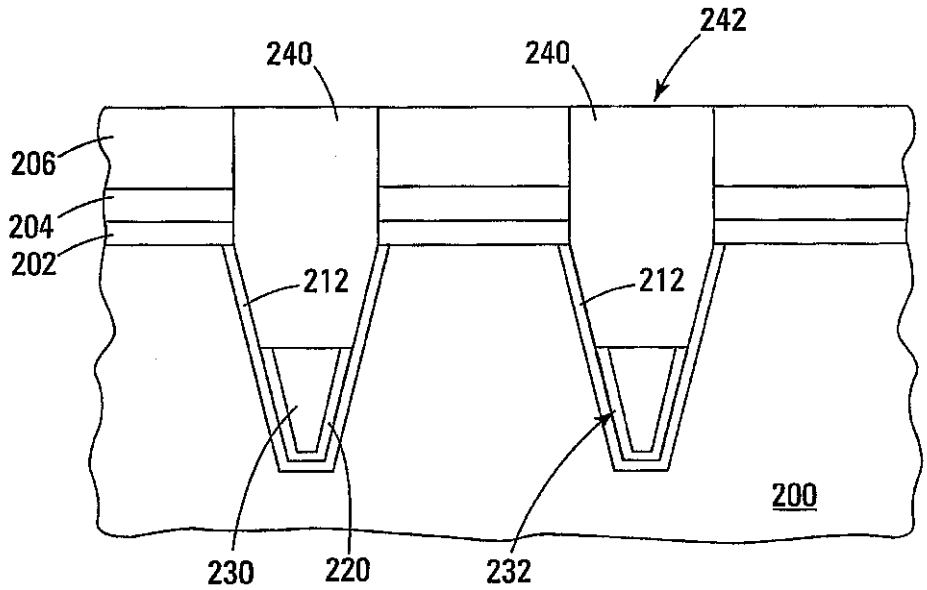

242
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Fig. 2G

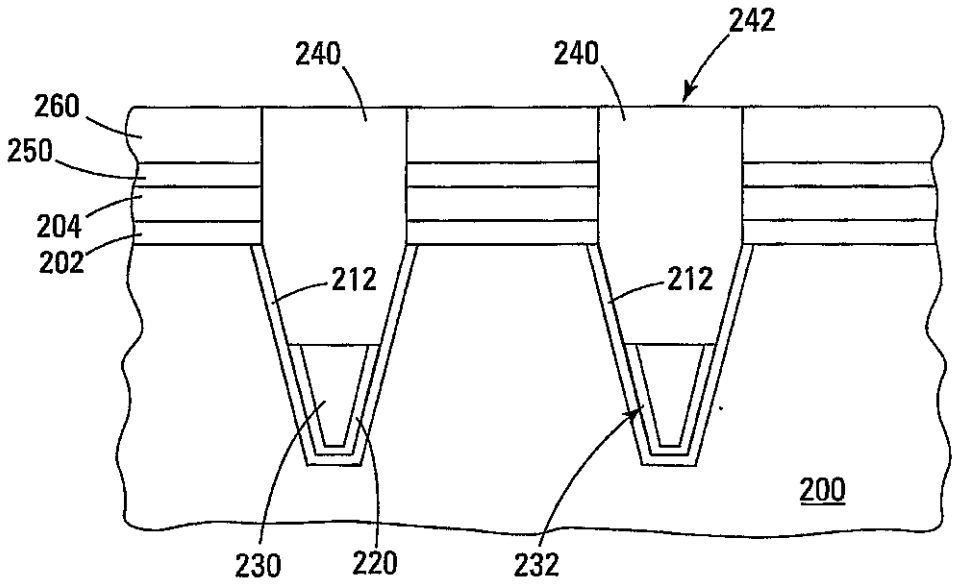

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212
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Fig. 2H