

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Transistor Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to transistor circuits, and to biasing arrangements for integrated circuits, including at least one amplifier, in particular.

As used herein, the term integrated circuit refers to a unitary or monolithic semiconductor device or chip which is the equivalent of a network of inter-connected active and passive circuit elements. Various problems have presented themselves in the design of such a semiconductor device. One problem, that of establishing and maintaining a stable operating point for integrated circuit amplifiers, is not solved by the use of techniques normally employed in discrete semiconductor amplifier circuits.

It is an object of the present invention, therefore, to provide an amplifier with an improved biasing circuit for establishing and maintaining a stable operating point suitable for integrated circuit amplifier configurations.

According to the invention there is provided the combination of at least one amplifier and a separate biasing circuit comprising first and second transistors, circuit means coupled to the emitter, base and collector electrodes of the first transistor for connecting said first transistor in a common emitter configuration, circuit means coupled to the emitter, base and collector electrodes of the second transistor for connecting said second transistor in a common collector configuration, means for coupling the collector electrode of said first transistor

to the base electrode of said second transistor, means for coupling the emitter electrode of said second transistor to the base electrode of said first transistor and means for deriving a direct output voltage between one of the emitter and base electrodes of said second transistor and the emitter electrode of said first transistor to bias one of said at least one amplifiers at a desired operating point.

A stabilized biasing voltage is developed between the emitter electrode of the first transistor and one of the base and emitter electrodes of the second transistor. The resultant circuit provides a very low impedance biasing voltage source which may be used to establish and maintain the operating point of semiconductor amplifier devices at a level primarily determined by the collector load resistance of the first transistor. A biasing circuit of the type described, when incorporated as an integral portion of an integrated circuit including the amplifier to be stabilized, is effective to maintain the operating point of the amplifier substantially constant over wide variations in power supply voltage and temperature.

Referring to the accompanying drawings: FIGURE 1 shows an example of amplifier loads connected to a stabilized biasing circuit forming a combination constructed in accordance with the invention;

FIGURE 2 shows a separate biasing circuit which when connected to an amplifier forms a combination in accordance with the invention;

FIGURE 3 shows a stage of transistor amplification provided with separate biasing in accordance with the invention; and

FIGURE 4 shows a portion of a radio receiver including a converter stage, an intermediate frequency (I.F.) amplifier stage and a separate stabilized biasing circuit in accordance with the invention, with the latter in-

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cluding provisions for automatic gain control

In FIGURE 1, the circuit includes a pair of transistors 12 and 14. Transistor 12 is arranged in a common emitter type configuration, with its collector electrode connected to an energizing potential terminal 16 through a resistor 18 and with its emitter electrode connected to a reference terminal 20 which is shown at ground potential. The other transistor 14 is arranged in a common collector type configuration, with its collector electrode connected to the energizing potential terminal 16 and with its emitter electrode connected to the reference terminal 20 through a resistor 24. The emitter electrode of transistor 14 is also connected to the base electrode of transistor 12 and to a first output terminal 22. The collector electrode of transistor 12 is additionally connected to the base electrode of transistor 14 and to a second output terminal 26. Appropriate amplifier load circuits 25 and 27 are connected between the first and second output terminals 22 and 26 and reference terminal 20, respectively. Potential terminal 16 and reference terminal 20 are adapted to be connected to a source of energizing potential of proper polarity (not shown).

If the current drawn by the load 25 is sufficient to permit the proper V_{be} voltage drop to develop across the base-emitter junction of transistor 14, the resistor 24 may be omitted. As used herein, the term V_{be} voltage represents the average base-to-emitter voltage of a transistor which is operating as the active device in an amplifier circuit or the like. For silicon transistors, the V_{be} voltage is approximately 0.7 volts, which is within the range of the proper V_{be} voltage for Class A amplification.

In the operation of the stabilized biasing circuit of FIGURE 1, i.e. with a proper polarity potential source connected between the terminals 16 and 20, a point of equilibrium is reached at which one V_{be} voltage drops are developed across the base-emitter junctions of each of the transistors 12 and 14. The base-emitter junction of transistor 14, however, is connected in parallel with the collector-base junction of transistor 12. The quiescent voltage developed between the collector and emitter electrodes of transistor 12 therefore equals the sum of the V_{be} voltage drops of transistors 12 and 14. With the emitter electrode of transistor 12 grounded via terminal 20, a potential equal to the V_{be} voltage drop of transistor 12 is developed at output terminal 22 relative to ground terminal 20 while a potential equal to the sum of the V_{be} voltage drops of transistors 12 and 14 is developed at output terminal 26 relative to ground terminal 20. If, on the other hand, the terminal 20 is not grounded but is at some level of voltage instead, then there output potentials would each be increased by that amount. In the discussion that follows, it will be understood that the tran-

sistors 12 and 14 are each composed of the same semiconductor material, such as is the case in monolithic silicon integrated circuits, so that their respective V_{be} voltage drops are equal. Thus the potential developed at output terminals 22 and 26 equal one and two V_{be} voltage drops, respectively, relative to the terminal 20.

The stabilized biasing circuit just described provides the following features. First, no capacitors are employed—thus the problems that would be created by incorporating capacitors in integrated circuit design is eliminated. Second, low values of resistance (of the order of 5,000 ohms) can be used for resistor 18 and for resistor 24 (where needed) which resistors, therefore, require only a small amount of space on an integrated circuit chip. And, third, the circuit presents a low output impedance at the terminal 22 for the load circuit 25 which is connected to it. This output impedance, between the terminals 20 and 22, is inversely proportional to the product of the gain of the common emitter stage and the transconductance of the common collector stage and, as such, is very low.

FIGURE 2 shows an arrangement of transistor interconnections which illustrates how an integral number of stabilized V_{be} voltage drops can be obtained and made available as biasing potentials. Three transistors 30, 32, and 34 are shown. The first transistor 30 is arranged in a common emitter type configuration, with its collector electrode connected to an energizing potential terminal 36 through a resistor 38 and with its emitter electrode connected to a reference terminal 31 which is connected to ground. The other two transistors 32 and 34 are arranged in a "cascaded" common collector type configuration, with the collector electrodes of each being connected to the energizing potential terminal 36 and with their emitter electrodes being connected to the reference terminal 31, that of transistor 32 through a resistor 40 and that of transistor 34 through a resistor 42. These resistors 40 and 42 are chosen to permit the proper V_{be} voltage drops to be developed across the base-emitter junctions of their respective transistors 32 and 34. The collector electrode of transistor 30 is also connected to the base electrode of transistor 32, the emitter electrode of transistor 32 to the base electrode of transistor 34, and the emitter electrode of transistor 34 to the base electrode of transistor 30. Output terminals 44, 46 and 48 are connected to the collector electrode of the transistor 30, the emitter electrode of the transistor 32, and the emitter electrode of the transistor 34, respectively.

In operation, i.e. with a proper polarity potential source connected between the terminals 36 and 31, a point of equilibrium is reached at which one V_{be} voltage drops are developed across the base-emitter junctions of

each of the transistors 30, 32 and 34. With the arrangement constructed as described, with terminal 31 grounded, and with transistors 30, 32 and 34 composed of the same semiconductor material, a potential of one V_{be} voltage drop is developed at terminal 48, a potential of two V_{be} voltage drops is developed at terminal 46, and a potential of three V_{be} voltage drops is developed at terminal 44. By virtue of the inter-connections between the various electrodes of transistors 30, 32 and 34, these potentials will remain substantially constant, even for wide variations in the applied energizing potential. As such, these potentials are useful for biasing purposes, at least one of which potentials is used to bias an amplifier in the combination of the invention.

It will be clear that higher biasing potentials than three V_{be} voltage drops can be obtained simply by increasing the number of cascaded common collector configurations—a four V_{be} voltage drop potential can be obtained by adding a third common collector stage, a five V_{be} voltage drop potential can be obtained by adding a fourth common collector stage, etc. Stabilized biasing potentials other than an integral number of V_{be} voltage drops can also be obtained through the use of appropriate voltage divider networks connected to one or more of the output terminals at which the V_{be} voltage drops are developed.

In FIGURE 3 the transistor amplifier 52 is stabilized by a biasing circuit 10 similar to that shown in FIGURE 1. Thus, the reference numerals used to designate selected components of the FIGURE 1 biasing circuit are used, whenever practical, to designate those same components in FIGURE 3 and also in FIGURE 4. FIGURE 3, however, differs from FIGURE 1 in that it includes a resistor 56 in the feedback path between the emitter electrode of transistor 14 and the base electrode of transistor 12.

Still referring to FIGURE 3, the amplifier circuit 52 shown includes a transistor 58 having its collector electrode connected to an energizing potential terminal 60 through a resistor 62 and its emitter electrode connected to ground. Signals to be amplified are applied across the input terminals 64 and are coupled via the conductor 98 to the base electrode of transistor 58. Amplified signals are developed at the collector electrode of transistor 58 and are coupled via the conductor 100 to the output terminal 66. The potential developed at the emitter electrode of the transistor 14 is applied to the base electrode of transistor 58 through an isolation resistor 68 to provide the operating bias for that transistor. The value of resistor 56 connected between the emitter electrode of transistor 14 and the base electrode of transistor 12 is so selected that the voltage drop across it is equal to the voltage drop produced across resistor 68 by the biasing current of transistor 58.

With a proper polarity potential source connected between potential terminal 60 and reference terminal 61, the operating point of the transistor 58 is established primarily by the value of the resistor 18, and this operating point is maintained substantially constant for wide variations in the applied energizing potential and temperature.

It will be understood that the biasing circuit 10 and the amplifier circuit 54 are both included in the same integrated circuit structure, such as a monolithic silicon integrated circuit made in accordance with known techniques. If desired, the biasing potential developed by the circuit 10 can be applied to several amplifiers. The low impedance presented by the biasing circuit minimizes the coupling between the various amplifiers from the common biasing supply connections.

In FIGURE 4 the converter stage of the radio receiver illustrated includes a transistor 70 arranged in a common emitter amplifier configuration, with its collector electrode connected to an energizing potential terminal 72 through a first I.F. resonant transformer circuit 74, and with its emitter electrode connected to ground. The converter stage also includes a radio frequency (R.F.) tuning circuit 76 and a local oscillator circuit 78 which is ganged to tune with the circuit 76. Input R.F. signals are coupled to the base electrode of transistor 70 through a secondary winding of the tuning circuit 76, one end of which is grounded for signal frequencies by capacitor 80. Local oscillator signals from circuit 78 are coupled to the base electrode of transistor 70 through coupling capacitor 82 to beat with the R.F. signals and produce amplified I.F. signals at the collector electrode of transistor 70. These amplified signals are then coupled through the secondary winding of the I.F. resonant circuit 74 to the base electrode of a transistor 84, included in the I.F. stage of the FIGURE 4 arrangement.

The transistor 84 is also arranged in a common emitter amplifier configuration, with its collector electrode connected to the potential terminal 72 through a second I.F. resonant transformer circuit 86 and with its emitter electrode connected to ground. The transistor 84 amplifies the I.F. signals coupled to its base electrode, the amplified signals being developed across the secondary winding of the I.F. resonant circuit 86. This winding may then be connected to a following amplifier or detector stage (not shown) for further processing of the amplified I.F. signals.

A bias potential for the converter transistor 70 and the I.F. transistor 84 is developed at the emitter electrode of the transistor 14 of the circuit 10 in the afore-described manner. This bias potential, which is in the order of one V_{be} voltage drop for the particular arrangement shown, is coupled through a resistor 88 to the base electrode of the I.F.

transistor 84 and, also through the secondary winding of the I.F. resonant circuit 74, and R.F. filter 90, and the secondary winding of the R.F. tuning circuit 76 to the base electrode of the converter transistor 70. A bypass capacitor 92 is connected between the junction of the R.F. filter 90 with the secondary winding of the I.F. resonant circuit 74 and ground. The R.F. filter 90 can be a low resistance unit, such as a choke coil or ferrite bead, so that the voltage drop across the unit due to the biasing current of the transistor 70 can be neglected.

Automatic gain control is provided in the circuit of FIGURE 4 by varying the bias coupled to the base electrodes of the converter and I.F. transistors 70 and 84. A transistor 94 is arranged in a common emitter configuration, with its collector electrode connected to the collector electrode of transistor 12 and with its emitter electrode connected to ground. A varying d.c. signal, indicative of variations in input signal intensity and derived in any suitable manner, is applied across the terminals 96 and coupled to the base electrode of transistor 94 to control its conductivity. In the discussion that follows, it will be understood that increases in the d.c. signal applied across terminal 96 correspond to increases in signal intensity from a threshold potential for no signal conditions. Increases in the d.c. signal, furthermore, are characterized by the d.c. signal going more positive than the threshold value.

In operation, any increase in the d.c. signal applied across the terminal 96 increases the conductivity of transistor 94, increases the voltage drop across resistor 18, and decrease the voltage at the base electrode of the transistor 14. The effect of any such decrease at the base electrode of the transistor 14 is to reduce the voltage developed at its emitter electrode and, therefore, the biasing potentials coupled to the base electrodes of transistors 70 and 84. As a result, the quiescent operating currents and transconductances of transistors 70 and 84 are reduced, with a corresponding reduction in the gain provided by the converter and I.F. stages. This automatic gain control action does not affect the stability of these stages, however, which is still controlled by the biasing arrangement 10. It will be understood that the converter transistor 70 and I.F. transistor 84 may be incorporated in the same integrated circuit structure as the biasing circuit 10 including the transistor 94. It will also be understood that this automatic gain control action can be used with the amplifier configuration of FIGURE 3 and can be included in the same integrated circuit structure as the arrangement there shown.

and a separate biasing circuit comprising first and second transistors, circuit means coupled to the emitter, base and collector electrodes of the first transistor for connecting said first transistor in a common emitter configuration, circuit means coupled to the emitter, base and collector electrodes of the second transistor for connecting said second transistor in a common collector configuration, means for coupling the collector electrode of said first transistor to the base electrode of said second transistor, means for coupling the emitter electrode of said second transistor to the base electrode of said first transistor and means for deriving a direct output voltage between one of the emitter and base electrodes of said second transistor and the emitter electrode of said first transistor to bias one of said at least one amplifiers at a desired operating point.

2. A combination as claimed in Claim 1, including first and second terminals adapted to be connected to a source of energizing potential; a first resistor connected between the collector electrode of said first transistor and said first terminal; a direct current connection from the emitter electrode of said first transistor to said second terminal; a direct current connection from the collector electrode of said second transistor to said first terminal; a direct current connection from the collector electrode of said first transistor to the base electrode of said second transistor; a direct current connection from the emitter electrode of said second transistor to the base electrode of said first transistor.

3. A combination as claimed in Claim 2, including a second resistor connected between the emitter electrode of said second transistor and said second terminal.

4. A combination as claimed in any one of the preceding claims, wherein one or more additional transistors coupled in the common collector configuration are cascaded with the second transistor, and means are provided for deriving output potentials from each of the cascaded transistors.

5. A combination as claimed in Claims 2 and 3, including a third transistor; a direct current connection from the collector electrode of said third transistor to said first terminal; a resistor connected between the emitter electrode of said third transistor and said second terminal; a direct current connection between the emitter electrode of said second transistor and the base electrode of said third transistor; a direct current connection between the emitter electrode of said third transistor and the base electrode of said first transistor; and means for deriving an output voltage between one of the emitter and base electrodes of said second and said third transistors and said second terminal.

6. A combination as claimed in Claim 5, including a semiconductor amplifier coupled

WHAT WE CLAIM IS:—

1. The combination of at least one amplifier

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transistor 84 and, also through the secondary winding of the I.F. resonant circuit 74, and R.F. filter 90, and the secondary winding of the R.F. tuning circuit 76 to the base electrode of the converter transistor 70. A bypass capacitor 92 is connected between the junction of the R.F. filter 90 with the secondary winding of the I.F. resonant circuit 74 and ground. The R.F. filter 90 can be a low resistance unit, such as a choke coil or ferrite bead, so that the voltage drop across the unit due to the biasing current of the transistor 70 can be neglected.

Automatic gain control is provided in the circuit of FIGURE 4 by varying the bias coupled to the base electrodes of the converter and I.F. transistors 70 and 84. A transistor 94 is arranged in a common emitter configuration, with its collector electrode connected to the collector electrode of transistor 12 and with its emitter electrode connected to ground. A varying d.c. signal, indicative of variations in input signal intensity and derived in any suitable manner, is applied across the terminals 96 and coupled to the base electrode of transistor 94 to control its conductivity. In the discussion that follows, it will be understood that increases in the d.c. signal applied across terminal 96 correspond to increases in signal intensity from a threshold potential for no signal conditions. Increases in the d.c. signal, furthermore, are characterized by the d.c. signal going more positive than the threshold value.

In operation, any increase in the d.c. signal applied across the terminal 96 increases the conductivity of transistor 94, increases the voltage drop across resistor 18, and decrease the voltage at the base electrode of the transistor 14. The effect of any such decrease at the base electrode of the transistor 14 is to reduce the voltage developed at its emitter electrode and, therefore, the biasing potentials coupled to the base electrodes of transistors 70 and 84. As a result, the quiescent operating currents and transconductances of transistors 70 and 84 are reduced, with a corresponding reduction in the gain provided by the converter and I.F. stages. This automatic gain control action does not affect the stability of these stages, however, which is still controlled by the biasing arrangement 10. It will be understood that the converter transistor 70 and I.F. transistor 84 may be incorporated in the same integrated circuit structure as the biasing circuit 10 including the transistor 94. It will also be understood that this automatic gain control action can be used with the amplifier configuration of FIGURE 3 and can be included in the same integrated circuit structure as the arrangement there shown.

WHAT WE CLAIM IS:—

1. The combination of at least one amplifier

and a separate biasing circuit comprising first and second transistors, circuit means coupled to the emitter, base and collector electrodes of the first transistor for connecting said first transistor in a common emitter configuration, circuit means coupled to the emitter, base and collector electrodes of the second transistor for connecting said second transistor in a common collector configuration, means for coupling the collector electrode of said first transistor to the base electrode of said second transistor, means for coupling the emitter electrode of said second transistor to the base electrode of said first transistor and means for deriving a direct output voltage between one of the emitter and base electrodes of said second transistor and the emitter electrode of said first transistor to bias one of said at least one amplifiers at a desired operating point.

2. A combination as claimed in Claim 1, including first and second terminals adapted to be connected to a source of energizing potential; a first resistor connected between the collector electrode of said first transistor and said first terminal; a direct current connection from the emitter electrode of said first transistor to said second terminal; a direct current connection from the collector electrode of said second transistor to said first terminal; a direct current connection from the collector electrode of said first transistor to the base electrode of said second transistor; a direct current connection from the emitter electrode of said second transistor to the base electrode of said first transistor.

3. A combination as claimed in Claim 2, including a second resistor connected between the emitter electrode of said second transistor and said second terminal.

4. A combination as claimed in any one of the preceding claims, wherein one or more additional transistors coupled in the common collector configuration are cascaded with the second transistor, and means are provided for deriving output potentials from each of the cascaded transistors.

5. A combination as claimed in Claims 2 and 3, including a third transistor; a direct current connection from the collector electrode of said third transistor to said first terminal; a resistor connected between the emitter electrode of said third transistor and said second terminal; a direct current connection between the emitter electrode of said second transistor and the base electrode of said third transistor; a direct current connection between the emitter electrode of said third transistor and the base electrode of said first transistor; and means for deriving an output voltage between one of the emitter and base electrodes of said second and said third transistors and said second terminal.

6. A combination as claimed in Claim 5, including a semiconductor amplifier coupled



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to receive said output voltage between one of the emitter and base electrodes of said second and third transistors and said second terminal.

5 7. A combination as claimed in Claim 6, wherein the operating point of said semiconductor amplifier is primarily determined by the value of the said first resistor.

10 8. A combination as claimed in Claim 6 or Claim 7, wherein said semiconductor amplifier includes a transistor having a collector electrode coupled to a first energizing potential terminal, an emitter electrode coupled to a second energizing potential terminal and a base electrode coupled to a source of input signals to be amplified; and wherein there are provided circuit means connecting the emitter electrode of the said second transistor to the base electrode of said first transistor for connecting the base-emitter junction of said second transistor in parallel with the collector-base junction of said first transistor; and means for deriving a first output voltage at low impedance between the emitter electrode of said second transistor and said second energizing potential terminal to bias said amplifier transistor at said operating point.

30 9. A combination as claimed in Claim 8, wherein there is also included means for deriving a second output voltage at a higher impedance between the base electrode of said second transistor and said second energizing potential terminal and at a voltage value substantially equal to twice the voltage value of said low impedance output voltage.

35 10. A combination as claimed in Claim 8 or Claim 9, wherein there is also included a third resistor connected between the emitter electrode of said second transistor and the base electrode of said amplifier transistor for isolating said input signal source from said output voltage deriving means and for coupling said derived output voltage to said amplifier transistor to bias said transistor at said operating point.

40 11. A combination as claimed in Claim 10, wherein there is additionally included means for applying an automatic gain control signal to the collector electrode of said first transistor for controlling the voltage value of said first output voltage and of the bias voltage coupled to the base electrode of said amplifier transistor.

50 12. A combination as claimed in any one of the preceding claims including a resistor in the feedback from the emitter of the second transistor to the base of the first transistor.

55 13. The combination as claimed in any one of the preceding claims integrated in the same semiconductor material.

60 14. A combination formed as a unitary

structure integrated with a single semiconductor body, including first, second, third and fourth transistors, each having an emitter electrode, a base electrode and a collector electrode; first and second terminals adapted to be connected to a source of energizing potential; a first resistor connected between the collector electrode of said first transistor and said first terminal; a direct current connection from the emitter electrode of said first transistor to said second terminal; a direct current connected from the base electrode of said first transistor to a source of input signals to be amplified; a second resistor connected between the collector electrode of said second transistor and said first terminal; a direct current connection from the emitter electrode of said second transistor to said second terminal; a direct current connection from the collector electrode of said third transistor to said first terminal; a third resistor connected between the emitter electrode of said third transistor and said second terminal; a fourth resistor connected between the emitter electrode of said third transistor and the base electrode of said first transistor; a direct current connection from the collector electrode of said second transistor to the base electrode of said third transistor; a fifth resistor connected between the emitter electrode of said third transistor and the base electrode of said second transistor; a direct current connection from the collector electrode of said fourth transistor to the collector electrode of said second transistor; a direct current connection from the emitter electrode of said fourth transistor to said second terminal; and a direct current connection from the base electrode of said fourth transistor to a source of d.c. signals indicative of the intensity level of said input signals to be amplified.

15. A circuit for a radio receiver including a converter stage and the combination as claimed in any one of the preceding claims, in which the amplifier is an intermediate frequency amplifier stage.

16. The combination of at least one amplifier, and a separate circuit for providing biasing voltages substantially as hereinbefore described with reference to Figure 1 or Figure 2 of the accompanying drawings.

17. An electrical circuit substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

18. An electrical circuit substantially as hereinbefore described with reference to Figure 4 of the accompanying drawings.

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