

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) IMPROVEMENTS IN OR RELATING TO CURRENT SOURCES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to current sources.

Integrated circuits are usually designed to use only PNP or NPN transistors in order to simplify the processing steps and thereby reduce the cost of manufacture. When one type of transistor is used, the integrated circuit can be optimized for that particular type. If transistors of the opposite type are also formed in this type of integrated circuit they usually have very low gains, in some cases less than unity. These transistors can be used only where a low gain will not affect performance.

In most circuit designs PNP transistors are used to provide positive sources of current. A typical circuit of this type is disclosed in U.S. Patent No. 3,185,858 which shows the use of two PNP transistors to form a current source. One of the transistors acts to control the current in the other transistor. This control is maintained because of the high gain of the transistor which produces a substantially flat $V_{CE}-I_C$ characteristic.

Other known circuits depend on the fact that high-gain PNP transistors have small base currents and, because of this, the base electrodes of these transistors can be connected to the control resistance without upsetting the control voltage. However, as already stated, this type of transistor is not usually present in most NPN majority monolithic integrated circuits.

This invention seeks to provide improved current sources suitable for manufacture in integrated circuit form.

According to one aspect of this invention a current source includes a first low-gain tran-

sistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, and means, including at least one high-gain transistor, connected both for diverting the base currents of said first and second low-gain transistors from said first resistance and for coupling voltage across said first resistance to the bases of said first and second low-gain transistors.

According to another aspect of this invention a current source includes a first low-gain transistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, a first high-gain transistor having its base connected to its collector and to the base of said first low-gain transistor, a second high-gain transistor having its collector connected to a second voltage source, its base connected to the collector of said second low-gain transistor, and its emitter connected to the emitter of said first high-gain transistor, and means for directing the emitter current of said first high-gain transistor to ground.

The said high-gain transistors may be of the NPN type and said low-gain transistors of the PNP type.

The means for directing the emitter current of said first high-gain transistor may be a second resistance.

As an alternative the means for directing the emitter current of said first high-gain transistor may be a current source of the opposite polarity including a third high-gain transistor

having its collector connected to the emitter of said first high-gain transistor and its emitter connected to ground, a fourth high-gain transistor having its base connected to its collector and to the base of said third transistor, and its emitter connected to ground, and a collector resistance having one end connected to the base of said fourth transistor and the other end to the collector of said second high-gain transistor.

There may be provided a circuit connected between said first resistance and said reference potential, said circuit comprising a pair of high-gain transistors, one of said transistors having its collector and base connected to said first resistance, and its emitter connected to said reference potential, and the other of said transistors having its emitter connected to said reference potential, its base connected to the base of said one transistor and its collector connected to a second output terminal, said source being such that, in operation, the ratio of the current output at said second output terminal to the current output at said first output terminal is substantially fixed.

The invention will now be described by way of example with reference to the accompanying drawing, in which:

Fig. 1 is a circuit diagram of a known positive current source;

Fig. 2 is a circuit diagram of an illustrative embodiment of the invention;

Fig. 3 is a circuit diagram of an illustrative embodiment of the invention with a known current source used to bias the circuit; and

Fig. 4 is a circuit diagram of an illustrative embodiment of the invention sharing a common control resistance with a known current source.

Referring now to Fig. 1, in a typical known positive current source the emitter electrodes 13 and 23 of transistors 10 and 20, respectively, and a positive voltage source V_s are connected to a terminal 14. The bases 12 and 22 of transistors 10 and 20, respectively, are connected to a terminal 15. The collector 11 of transistor 10 is connected to the output of the circuit and the collector 21 of transistor 20 is connected to a terminal 17. Terminal 15 is connected to terminal 17 and a control resistance 16 is connected between terminal 17 and ground. Because the bases and the emitters of the two transistors are connected together, the collector currents of the two substantially identical transistors are substantially the same. Since the base and collector of transistor 20 are connected together, this transistor acts as a diode. Therefore, the current through resistance 16 is substantially equal to

$$I = \frac{V_s - V_{BE}}{R_{16}} \quad (1)$$

where V_s is the value of the positive voltage source and V_{BE} is the base emitter voltage of transistor 22. Since the two transistors have high gains, nearly all of this current will be the collector current of transistor 20. Because the bases and the emitters of the two transistors are connected together, the output current I_o will nearly equal the control resistance current I .

Referring now to Fig. 2, the emitter electrodes 33 and 43 of low-gain PNP transistors 30 and 40, respectively, and a positive voltage source, V_{s1} , are connected to terminal 24. The bases 32 and 42 of transistors 30 and 40, respectively, are connected to terminal 25. The collector 31 of transistor 30 is connected to the output of the circuit and the collector 41 of transistor 40 is connected to terminal 27. Resistance 26 is connected between terminal 27 and ground. To control the current output of the circuit the control voltage developed across resistance 26 must be applied to the bases of the PNP transistors at terminal 25. However, since the PNP transistors have low gain, their relatively large base currents would upset the control voltage. In order to draw off the base current while still providing a path from terminal 25 to terminal 27, NPN transistors 50 and 60 are provided. Terminal 25 is connected to base 52 and collector 51 of transistor 50, emitter 53 of which is connected to terminal 34. Terminal 34 is connected to one side of resistance 35 and to emitter 64 of transistor 60. The other side of resistance 35 is connected to ground. Collector 61 of transistor 60 is connected to a second positive voltage source, V_{s2} , and base 62 of transistor 60 is connected to terminal 27. When the circuit is first turned ON an increasing current flows through transistor 40 and resistance 26. This produces an increasing voltage at terminal 27. The voltage at terminal 27 is coupled to terminal 25 through the base-emitter junctions of transistors 50 and 60. This control voltage increases until it comes within a normal base-emitter voltage level of the first voltage source, V_{s1} . When this happens, the circuit stabilizes, producing a constant current output. The large base currents of transistors 30 and 40 flow through transistor 50 and resistance 35 to ground. In this way a positive current source is provided using low-gain PNP transistors.

Fig. 3 is a modification of the arrangement of Fig. 2 where resistance 35 is replaced with a conventional negative constant current source similar to that shown in Fig. 1. The conventional negative constant current source is made up of transistors 70 and 80 and resistance 36. The collector 71 of transistor 70 is connected to terminal 34. The emitters 73 and 83 of transistors 70 and 80, respectively, are connected to ground. The bases 72 and 82 of transistors 70 and 80, res-

pectively, are connected to terminal 64. Collector 81 of transistor 80 and one end of resistance 36 are also connected to terminal 64. The other end of resistance 36 is connected to collector 61 of transistor 60. With the replacement of resistance 35 by this negative current source, the positive current source can operate over a wider range of V_{s1} voltages since a constant current is drawn through the emitters of transistors 50 and 60, substantially independent of the voltage at terminal 34.

Fig. 4 shows the circuit of Fig. 3 connected to a known circuit similar to that shown in Fig. 1 in order to form a dual current supply in which the output currents are locked in a fixed ratio. Both circuits share a common control resistance, 16. Since the known portion of Fig. 4 uses NPN transistors, it functions as a negative current source. The current through control resistance 16 is equal to

$$I = \frac{V_{s1} + V_{ss} - 2V_{BE}}{R_{16}} \quad (2)$$

where V_{s1} is the first positive voltage source, V_{ss} is the negative voltage source, V_{BE} is the base-emitter voltage of transistor 20 and 40 which are assumed to be the same, and R_{16} is resistor 16. Since the output currents of both circuits are determined by the current through the control resistance, the two output currents are locked together in a fixed ratio. If the emitter area of transistor 10 is twice that of transistor 30, the ratio will be 2:1. The ratio of output currents in this circuit will be maintained substantially regardless of changes in supply voltage or the control resistance.

As described the invention provides a source of positive current suitable for use in an NPN majority monolithic integrated circuit which has been optimized for NPN transistors, overcoming the problem of low gain in the PNP transistors. With suitable modifications of course the invention may equally well find application as a negative current source in a NPN majority monolithic integrated circuit.

WHAT WE CLAIM IS:—

1. A current source including a first low-gain transistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, and means, including at least one

high-gain transistor, connected both for diverting the base currents of said first and second low-gain transistors from said first resistance and for coupling voltage across said first resistance to the bases of said first and second low-gain transistors.

2. A current source including a first low-gain transistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, a first high-gain transistor having its base connected to its collector and to the base of said first low-gain transistor, a second high-gain transistor having its collector connected to a second voltage source, its base connected to the collector of said second low-gain transistor, and its emitter connected to the emitter of said first high-gain transistor, and means for directing the emitter current of said first high-gain transistor to ground.

3. A source as claimed in claim 2 wherein said high-gain transistors are of the NPN type and said low-gain transistors are of the PNP type.

4. A source as claimed in claim 2 or 3 wherein said means for directing the emitter current of said first high-gain transistor is a second resistance.

5. A source as claimed in claim 2 or 3 wherein said means for directing the emitter current of said first high-gain transistor is a current source of the opposite polarity including a third high-gain transistor having its collector connected to the emitter of said first high gain transistor and its emitter connected to ground, a fourth high-gain transistor having its base connected to its collector and to the base of said third transistor, and its emitter connected to ground, and a collector resistance having one end connected to the base of said fourth transistor and the other end to the collector of said second high-gain transistor.

6. A source as claimed in claim 2, 3 or 5 and including a circuit connected between said first resistance and said reference potential, said circuit comprising a pair of high-gain transistors, one of said transistors having its collector and base connected to said first resistance, and its emitter connected to said reference potential, and the other of said transistors having its emitter connected to said reference potential, its base connected to the base of said one transistor and its collector connected to a second output terminal, said source being such that, in operation, the ratio of the current output at said second output terminal to the current output



pectively, are connected to terminal 64. Collector 81 of transistor 80 and one end of resistance 36 are also connected to terminal 64. The other end of resistance 36 is connected to collector 61 of transistor 60. With the replacement of resistance 35 by this negative current source, the positive current source can operate over a wider range of V_{s1} voltages since a constant current is drawn through the emitters of transistors 50 and 60, substantially independent of the voltage at terminal 34.

Fig. 4 shows the circuit of Fig. 3 connected to a known circuit similar to that shown in Fig. 1 in order to form a dual current supply in which the output currents are locked in a fixed ratio. Both circuits share a common control resistance, 16. Since the known portion of Fig. 4 uses NPN transistors, it functions as a negative current source. The current through control resistance 16 is equal to

$$I = \frac{V_{s1} + V_{s3} - 2V_{BE}}{R_{16}} \quad (2)$$

where V_{s1} is the first positive voltage source, V_{s3} is the negative voltage source, V_{BE} is the base-emitter voltage of transistor 20 and 40 which are assumed to be the same, and R_{16} is resistor 16. Since the output currents of both circuits are determined by the current through the control resistance, the two output currents are locked together in a fixed ratio. If the emitter area of transistor 10 is twice that of transistor 30, the ratio will be 2:1. The ratio of output currents in this circuit will be maintained substantially regardless of changes in supply voltage or the control resistance.

As described the invention provides a source of positive current suitable for use in an NPN majority monolithic integrated circuit which has been optimized for NPN transistors, overcoming the problem of low gain in the PNP transistors. With suitable modifications of course the invention may equally well find application as a negative current source in a PNP majority monolithic integrated circuit.

WHAT WE CLAIM IS:—

1. A current source including a first low-gain transistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, and means, including at least one

high-gain transistor, connected both for diverting the base currents of said first and second low-gain transistors from said first resistance and for coupling voltage across said first resistance to the bases of said first and second low-gain transistors.

2. A current source including a first low-gain transistor having its collector connected to an output terminal and its emitter connected to a first voltage source, a second low-gain transistor having its emitter and base connected respectively to the emitter and to the base of said first low-gain transistor, a first resistance having one end connected to the collector of said second low-gain transistor and the other end to a point of reference potential, a first high-gain transistor having its base connected to its collector and to the base of said first low-gain transistor, a second high-gain transistor having its collector connected to a second voltage source, its base connected to the collector of said second low-gain transistor, and its emitter connected to the emitter of said first high-gain transistor, and means for directing the emitter current of said first high-gain transistor to ground.

3. A source as claimed in claim 2 wherein said high-gain transistors are of the NPN type and said low-gain transistors are of the PNP type.

4. A source as claimed in claim 2 or 3 wherein said means for directing the emitter current of said first high-gain transistor is a second resistance.

5. A source as claimed in claim 2 or 3 wherein said means for directing the emitter current of said first high-gain transistor is a current source of the opposite polarity including a third high-gain transistor having its collector connected to the emitter of said first high gain transistor and its emitter connected to ground, a fourth high-gain transistor having its base connected to its collector and to the base of said third transistor, and its emitter connected to ground, and a collector resistance having one end connected to the base of said fourth transistor and the other end to the collector of said second high-gain transistor.

6. A source as claimed in claim 2, 3 or 5 and including a circuit connected between said first resistance and said reference potential, said circuit comprising a pair of high-gain transistors, one of said transistors having its collector and base connected to said first resistance, and its emitter connected to said reference potential, and the other of said transistors having its emitter connected to said reference potential, its base connected to the base of said one transistor and its collector connected to a second output terminal, said source being such that, in operation, the ratio of the current output at said second output terminal to the current output

at said first output terminal is substantially fixed.

- 5 7. A source as claimed in claim 6 wherein said pair of high-gain transistors are of the NPN type, said low-gain transistors are of the PNP type, and said reference potential is negative.

8. A current source substantially as herein

described with reference to Fig. 2, 3 or 4 of the accompanying drawing.

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