CLAIMS:

1. A method for programming a resistive memory cell, the method comprising:
providing a programming signal to the resistive memory cell, the programming signal comprising:
an electrical pulse, and
a bias pulse coupled with the electrical pulse;
wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,
wherein the bias pulse comprises a voltage below a threshold switching voltage of the resistive memory cell, and
wherein the programming signal comprises a peak voltage above the threshold switching voltage of the resistive memory cell.

2. The method according to claim 1, wherein the resistive memory cell comprises a phase change memory cell.

3. The method according to claim 1, wherein providing the programming signal reduces the resistance of the resistive memory cell to a level corresponding to a SET state of the resistive memory cell.

4. The method according to claim 1, wherein the threshold switching voltage is in the range from about 0.3 V to about 2 V.

5. The method according to claim 4, wherein the threshold switching voltage is in the range from about 0.4 V to about 1 V.

6. The method according to claim 5, wherein the threshold switching voltage is in the range from about 0.6 V to about 0.8 V.

7. The method according to claim 1, wherein the duration of the bias pulse is longer than the duration of the electrical pulse.

8. The method according to claim 1, wherein the duration of the bias pulse is in the range of nanoseconds to microseconds.

9. The method according to claim 1, wherein the duration of the electrical pulse is in the range from about 10 nanoseconds to about 1 microsecond.

10. The method according to claim 1, wherein the duration of the electrical pulse is in the range from about 1 nanosecond to about 100 nanoseconds.

11. The method according to claim 1, wherein the resistive memory cell is a binary memory cell.

12. The method according to claim 1, wherein the resistive memory cell is a multilevel memory cell.

13. The method according to claim 12, wherein a first programming signal is provided

for programming the multilevel memory cell in a first resistance level, and a second programming signal is provided for programming the multilevel memory cell in a second resistance level, wherein the first resistance level is different from the second resistance level.

14. The method according to claim 13, wherein the first resistance level and the second resistance level are different from a lowest resistance level of the multilevel memory cell, wherein the lowest resistance level corresponds to the SET state of the multilevel memory cell.

15. The method according to claim 12, wherein depending on the resistance level of the multilevel memory cell, various programming signals are provided for programming the multilevel memory cell, the various programming signals varying in one or more of the following:
voltage of the bias pulse,
the peak voltage of the programming signal,
the duration of the bias pulse,
the duration of the electrical pulse.

16. A method for programming one or more resistive memory cells in a resistive memory array, the method comprising:
providing a programming signal to the one or more resistive memory cells, the programming signal comprising:
an electrical pulse, and
a bias pulse coupled with the electrical pulse;
wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,
wherein the bias pulse comprises a voltage below a threshold switching voltage of the one or more resistive memory cells, and
wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

17. The method according to claim 16, wherein the one or more resistive memory cells comprise one or more phase change memory cells.

18. A method for programming a resistive memory cell, the method comprising:
providing a programming signal to the resistive memory cell, the programming signal comprising:
an electrical pulse portion, and
at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions;
wherein each of the at least two bias pulse portions comprises a respective voltage below a threshold switching voltage of the resistive memory cell, and
wherein the programming signal comprises a peak voltage above the threshold switching voltage of the resistive memory cell.

19. A memory apparatus comprising a memory array, the memory array comprising:
one or more resistive memory cells; and

a programming circuit coupled with the one or more resistive memory cells and configured in use to provide a programming signal to the one or more resistive memory cells to program the one or more resistive memory cells, the programming signal comprising:
an electrical pulse, and
a bias pulse coupled with the electrical pulse;
wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,
wherein the bias pulse comprises a voltage below a threshold switching voltage of the one or more resistive memory cells, and
wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

20. The memory apparatus according to claim 19, wherein the one or more resistive memory cells comprise one or more phase change memory cells.

21. A memory apparatus comprising a memory array, the memory array comprising:
one or more resistive memory cells; and
a programming circuit coupled with the one or more resistive memory cells and configured in use to provide a programming signal to the one or more resistive memory cells to program the one or more resistive memory cells, the programming signal comprising:
an electrical pulse portion, and
at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions;
wherein each of the at least two bias pulse portions comprises a respective voltage below a threshold switching voltage of the one or more resistive memory cells, and
wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

22. The memory apparatus according to claim 21, wherein the one or more resistive memory cells comprise one or more phase change memory cells.

CLAIMS

1. A method for programming a resistive memory cell, the method comprising:

providing a programming signal to the resistive memory cell, the programming signal comprising:

an electrical pulse, and

a bias pulse coupled with the electrical pulse;

wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,

wherein the bias pulse comprises a voltage below a threshold switching voltage of the resistive memory cell, and

wherein the programming signal comprises a peak voltage above the threshold switching voltage of the resistive memory cell.

2. The method according to claim 1, wherein the resistive memory cell comprises a phase change memory cell.

3. The method according to any one of claims 1 or 2, wherein providing the programming signal reduces the resistance of the resistive memory cell to a level corresponding to a SET state of the resistive memory cell.

4. The method according to any one of claims 1 to 3, wherein the threshold switching voltage is in the range from about 0.3 V to about 2 V.

5. The method according to claim 4, wherein the threshold switching voltage is in the range from about 0.4 V to about 1 V.

6. The method according to claim 5, wherein the threshold switching voltage is in the range from about 0.6 V to about 0.8 V.

7. The method according to any one of claims 1 to 6, wherein the duration of the bias pulse is longer than the duration of the electrical pulse.

8. The method according to any one of claims 1 to 7, wherein the duration of the bias pulse is in the range of nanoseconds to microseconds.

9. The method according to any one of claims 1 to 8, wherein the duration of the electrical pulse is in the range from about 10 nanoseconds to about 1 microsecond.

10. The method according to any one of claims 1 to 8, wherein the duration of the electrical pulse is in the range from about 1 nanosecond to about 100 nanoseconds.

11. The method according to any one of claims 1 to 10, wherein the resistive memory cell is a binary memory cell.

12. The method according to any one of claims 1 to 10, wherein the resistive memory cell is a multilevel memory cell.

13. The method according to claim 12, wherein a first programming signal is provided for programming the multilevel memory cell in a first resistance level, and a second programming signal is provided for programming the multilevel memory cell in a second resistance level, wherein the first resistance level is different from the second resistance level.

14. The method according to claim 13, wherein the first resistance level and the second resistance level are different from a lowest resistance level of the multilevel memory cell, wherein the lowest resistance level corresponds to the SET state of the multilevel memory cell.

15. The method according to any one of claims 12 to 14, wherein depending on the resistance level of the multilevel memory cell, various programming signals are provided for programming the multilevel memory cell, the various programming signals varying in one or more of the following:

voltage of the bias pulse,

the peak voltage of the programming signal,

the duration of the bias pulse,

the duration of the electrical pulse.

16. A method for programming one or more resistive memory cells in a resistive memory array, the method comprising:

providing a programming signal to the one or more resistive memory cells, the programming signal comprising:

an electrical pulse, and

a bias pulse coupled with the electrical pulse;

wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,

wherein the bias pulse comprises a voltage below a threshold switching voltage of the one or more resistive memory cells, and

wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

17. The method according to claim 16, wherein the one or more resistive memory cells comprise one or more phase change memory cells.

18. A method for programming a resistive memory cell, the method comprising:

providing a programming signal to the resistive memory cell, the programming signal comprising:

an electrical pulse portion, and

at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions;

wherein each of the at least two bias pulse portions comprises a respective voltage below a threshold switching voltage of the resistive memory cell, and

wherein the programming signal comprises a peak voltage above the threshold switching voltage of the resistive memory cell.

19. A memory apparatus comprising a memory array, the memory array comprising:

one or more resistive memory cells; and

a programming circuit coupled with the one or more resistive memory cells and configured in use to provide a programming signal to the one or more resistive memory cells to program the one or more resistive memory cells, the programming signal comprising:

an electrical pulse, and

a bias pulse coupled with the electrical pulse;

wherein the electrical pulse comprises an electrical pulse portion, and the bias pulse comprises at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions,

wherein the bias pulse comprises a voltage below a threshold switching voltage of the one or more resistive memory cells, and

wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

20. The memory apparatus according to claim 19, wherein the one or more resistive memory cells comprise one or more phase change memory cells.

21. A memory apparatus comprising a memory array, the memory array comprising:

one or more resistive memory cells; and

a programming circuit coupled with the one or more resistive memory cells and configured in use to provide a programming signal to the one or more resistive memory cells to program the one or more resistive memory cells, the programming signal comprising:

an electrical pulse portion, and

at least two bias pulse portions, the electrical pulse portion being positioned between the at least two bias pulse portions;

wherein each of the at least two bias pulse portions comprises a respective voltage below a threshold switching voltage of the one or more resistive memory cells, and

wherein the programming signal comprises a peak voltage above the threshold switching voltage of the one or more resistive memory cells.

22. The memory apparatus according to claim 21, wherein the one or more resistive memory cells comprise one or more phase change memory cells.