

PATENT SPECIFICATION

(11) 1350 090

1350 090

- (21) Application No. 59075/71 (22) Filed 20 Dec. 1971
 (31) Convention Application No. 127219 (32) Filed 30 Dec. 1970 in
 (33) Japan (JA)
 (44) Complete Specification published 18 April 1974
 (51) International Classification G04C 3/00
 (52) Index at acceptance G3T A5X



(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIME-PIECES

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA a Japanese company, of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic time-pieces, hereinafter called watches; and more specifically to electronic watches of the kind comprising a time-standard oscillator driving a time indicator *via* a frequency divider. The invention is concerned with time re-setting means for such watches.

Electronic watches comprising a time-standard oscillator of relatively high frequency, a divider driven by said oscillator and time indicating means driven by said divider, are well known. In such a watch, when a required indicated time is to be set up, it is necessary not only to set the time indicator to a particular initial state but also to set the divider at zero. Also, when the watch is maintained at rest, it is desirable, in order to retain its accuracy, that the action of the time standard oscillator be not stopped.

The present invention seeks to provide improved electronic watches of the kind referred to with time resetting means which shall be simpler and cheaper than the comparable means at present employed in known watches of the said kind, and which shall also be of high reliability, and such as to result in very low power consumption when the watch is left at rest with the time standard oscillator in action. As will be seen later the invention utilises, for time setting purposes, portions of the normally provided frequency divider, thereby reducing the additional apparatus required for time setting.

According to this invention, the frequency divider of an electronic watch of the kind comprising a time standard oscillator, a frequency divider producing a lower frequency from a relatively high frequency output from

said oscillator, and time indicating means driven by said lower frequency, incorporates master-slave flip-flop binary circuits utilising complementary insulated gate field effect transistors; re-setting means are provided at least in one of the master or in one of the slave flip-flop circuits; and means providing a clock signal flip-flop action are so arranged that a master or slave flip-flop circuit which is not provided with re-setting means is caused, during the time in which re-setting is occurring, to be subordinated to a slave or master flip-flop circuit which is provided with re-setting means.

The invention is illustrated in and further explained with reference to the accompanying drawings, in which:—

Figure 1 shows diagrammatically a known binary frequency divider utilising complementary type insulated gate field effect transistors (hereinafter called CMOS);

Figure 2 similarly shows a binary frequency divider using CMOS and employed in carrying out this invention;

Figure 3 is a block diagram showing the circuit of Figure 2 as applied to an electronic watch in accordance with this invention; and

Figure 4 is a waveform diagram for explaining the action of Figure 3.

Referring to Figure 1, an electric power supply source (no shown: normally a dry battery) has its positive terminal connected to terminal 1 and its negative terminal connected to terminal 2. A master flip-flop 17 arranged within the chain line block so referenced comprises a first transfer gate 9, a second transfer gate 10, a first NAND circuit 11 and a first inverter 12. Each of these units, like other units to be described, is shown within its own broken line block.

A slave flip-flop 18 consists of a third transfer gate 13, a fourth transfer gate 14, a second NAND circuit 15 and a second inverter 16. Clock signal inputs are applied at terminals 3 and 4. These inputs are in phase opposition as indicated conventionally

[Price 25p]

by the legends ϕ and $\bar{\phi}$. The first transfer gate 9 and the third transfer gate 13 are in a signal state (to be called ON hereafter) at a high potential (to be called H hereafter), and in a signal interruption state (to be called OFF hereafter) at a low potential (to be called L hereafter). In the same way, the second transfer gate 10 and the fourth transfer gate 14 become ON when the clock input at 4 is at H and become OFF when the clock input at that terminal is at L.

When a re-set signal $\bar{P}$ applied at terminal 5 is at H, the first NAND circuit 11 and the second NAND circuit 15 work as inverters for the output of the transfer gate 9 or 10 and for the output of the transfer gate 13 or 14 respectively. When the re-set signal

$\bar{P}$ at the terminal 5 is at L the output of the transfer gate 9 or 10 and the output of the transfer gate 13 or 14 always become at H. Therefore, in the usual action, that is,

when $\bar{P}$ is at H, the master flip-flop 17 is kept connected through the first transfer gate 9 if the clock signal input $\bar{\phi}$ at 3 is at H, and the state of the said master flip-flop 17 is written in the slave flip-flop 18 through the third transfer gate 13. If the clock signal

input ϕ at 4 is at H, the slave flip-flop 18 is kept connected through the fourth transfer gate 14, and the state of opposite phase to the slave flip-flop 18 is written in the master flip-flop 17 through the second transfer gate 10. As a result, in two periods of the clock

signal input $\bar{\phi}$ at 3 (or of the clock signal input ϕ at 4) a signal of one period divided into halves in frequency is obtained at the outer terminal 6 ($\bar{Q}$) or at the output terminal 7 (Q).

On the other hand, in the case of a binary divider circuit chain, the fore-stage outputs

$\bar{Q}-1$ and $Q-1$ (to be mentioned later) are made to correspond to the clock signal inputs $\bar{\phi}$ and ϕ .

Because the master flip-flop or the slave flip-flop is in a subordinate relation to the other it follows that in the re-set condition the re-set circuit of the flip-flop in the subordinate state can be omitted by suitably setting the phase of the input flip-flop. Figure 2 shows, in manner similar to Figure 1, an arrangement in accordance with this invention in which such simplification is achieved. Figure 2 shows one example of a binary divider circuit simplified in accordance with this invention by using CMOS.

Comparing Figure 2 with Figure 1, it will be seen that the first NAND circuit of Figure 1 is replaced by the third inverter 19, and

the clock input $\bar{\phi}$ at 3 and the clock input ϕ at 4 are limited to the fore-stage outputs

$\bar{Q}-1$, $Q-1$, which are similar to those in Figure 2. In this condition, since in the

re-set state ($\bar{P} : L$) the output $\bar{Q}$ at 6 of the slave flip-flop 18 becomes at H

($\bar{Q}-1 : H$) and the output Q at 7 becomes

at L ($Q-1 : L$), the signal clock input $\bar{\phi}$ at 3 ($\bar{Q}-1$) becomes necessarily at L and

the clock signal input ϕ at 4 ($Q-1$) becomes at H. Therefore, the state of opposite phase of the slave flip-flop 18 is automatically written into the master flip-flop 17 which is in the subordinate state.

When the reset signal $\bar{P}$ at 5 is at H, the circuit of Figure 2 gives a binary frequency dividing action similar to that given by the known arrangement of Figure 1.

Similarly simplification can also be obtained by replacing the second NAND circuit 15 with an inverter, and making the relation of the clock signal to the fore-stage

output be clock signal $\bar{\phi} = \bar{Q}-1$ and clock signal $\phi = Q1$.

As will now be appreciated, the invention enables the binary divider circuit chain of a master-slave flip-flop system to be simplified by appropriately limiting the clock signal input in the re-set state (independent of difference in the means for re-setting and whether the means for re-setting operate on any position of the master flip-flop or of the slave flip-flop) it being then sufficient to apply the means for re-setting, between the master flip-flop and the slave flip-flop, to one flip-flop only, the one in question being determined by the phase of the clock input.

Figure 3 shows one way of applying the invention to an electronic watch. At an input terminal 20 is applied a time standard signal of (say) 16,384 c/s from a standard time oscillator (not shown). When a preset signal

$\bar{P}$ applied at 21 is at H, the time standard signals from terminal 20 reach the clock

input terminals $\bar{\phi}_0$ and ϕ_0 of a binary divider

circuit 25, ϕ_0 reaching the circuit 25 through a NAND circuit 23 and $\bar{\phi}_0$ reaching said circuit through said NAND circuit and an inverter 24. Each step stage in the binary divider

circuit chain 25, 26 . . . 32 is a binary divider circuit without re-set means, each being as shown in Figure 1 but modified by replacing each of the NAND circuits 11 and 15 in

In Figure 3, ϕ_0 to ϕ_{14} and ϕ_0 to ϕ_{14} and clock signals of opposite phase to each other

respectively, $\bar{Q}_0$ to $\bar{Q}_{14}$ and Q_0 to Q_4 are output signals of opposite phase to each other respectively. The symbols S_8 to S_{13} indicate

that, when a re-set signal $\bar{P}$ at 21 acts on the slave flip-flop side, each of the outputs

$\bar{Q}_8$ to $\bar{Q}_{13}$ is re-set at H. As already seen,

when the re-set signal $\bar{P}$ at 21 is at H, the binary divider circuit chain 25 to 38 carry out their normal frequency dividing function. 39 is a $1/2$ period ($\frac{1}{2}D$) delay circuit by which a $1c/s$ frequency divided output Q_{13} fed to the input of the delay circuit is delayed by the period $\frac{1}{2}D$ that is, $(1/64th)$ half of the

period of the clock signal ϕ_{14} , i.e. the period

of $\bar{Q}_8H$, and is transferred to the output Q_{14} (or $\bar{Q}_{14}$).

The frequency divided output Q_{13} and the delayed output $\bar{Q}_{14}$ are applied to a NAND circuit 40 which passes out an L level signal to the output terminal 22 for a period of $1/64$ sec once a second.

Summarising, it will be seen that when the present input $\bar{P}_{21}$ is at H, the time standard signal of $16,384$ c/s at the terminal 20 is frequency divided down to 1 c/s through the binary frequency circuit chain 25 to 38, and by the action of the $\frac{1}{2}D$ delay circuit 39 and the NAND circuit 40, there is obtained at the output terminal 22 an L signal of $1/64$ sec in width and 1 sec in period.

Next, in a re-set state, that is, when $\bar{P}_{21}$ is at L, since the NAND circuit 23 will have an output independent of the input 20, the circuits including the inverter 24, the binary frequency dividing circuit chain 25 to 38, the $\frac{1}{2}D$ delay circuit 39 and the NAND circuit 40 come to a rest state. In this state, because of the use of CMOS components, the power consumption is so small as to be negligible, (in a CMOS circuit the power consumption due to a discharge of capacity in the transition state occupies a major part of the consumed power), and as the output Q_{14} of the $\frac{1}{2}D$ delay circuit 39 has been

determined so as to coincide with Q_{13} when

input Q_{14} ($\bar{Q}_8$) is at H level, the output of the NAND circuit 40 becomes at H level, so that there occurs no power consumption in the driving circuit (not shown in the figure) connected to the NAND circuit 40. There is, therefore, very low power consumption of the watch when it is maintained at rest for a long time without stopping the time standard signal.

The action for re-setting to the correct time will now be explained with reference to Figure 4.

In Figure 4 (t) is the time axis and the lines $\bar{P}$, Q_8 , Q_9 , Q_{13} , $\bar{Q}_{14}$, 22 represent the signal waveforms at the correspondingly referenced terminals in Figure 3 respectively. Suppose that a present operation is done at times (t_0). The action of the binary divider circuit chain takes place as already described, and, in addition, the indication of seconds is set at 59 secs. by means of a mechanism

not shown. Then, if signal $\bar{P}$ is changed to the high level H at the instant t_1 when the indicated time indicates the correct time there at a time (t_2) which is only a very small fraction of a second (one period of the binary divider circuit 32) after (t_1), the output Q_8 of the binary divider circuit 33 necessarily changes to H level. Since, during the time from (t_0) to (t_2), a content of opposite phase to the slave flip-flop is written into the master flip-flop of the binary divider

circuit 34, at the instant when ϕ_9 (Q_9) changes to H level at the time (t_2), a signal of the same phase is sent in the binary divider circuit 34 from the master flip-flop to the slave flip-flop, and the output Q_8 thereof changes to H level. Thereafter, similar actions occur one after another in the binary divider circuit chain 35 to 38 bringing Q_{13} into H level.

However, since the clock ϕ_{14} (Q_8) has a delay ($1/64$ sec) of the amount of the H level period as signal Q_8 as mentioned before,

in the $\frac{1}{2}$ delay circuit $39Q_{14}$ changes to L level at a time (t_3) which is $1/64$ sec. from (t_2). In the flip-flop circuit of the 8th stage

in Figure 3, the master flip-flop ($M8$) is also preset so as correctly to maintain the time from (t_2) to (t_3). As a result, the output 22 of the binary divider circuit chain produces, as shown in line 22 of Figure 4, an L level signal of $1/64$ sec duration that starts at the time (t_2) which is less than $1/64$ sec after the time (t_1) when the preset is released and stops at the time (t_3) $1/64$ sec after the time (t_2), so that the correct time

in seconds is indicated by a mechanism not shown.

5 In obtaining the signal for setting the correct time in seconds there is a time delay of the order of $1/64$ sec, but this does not matter in practice. As will now be appreciated this use of part of the binary divider circuit chain of the watch for the pre-setting operation enables a substantial simplification of the circuitry to be effected. At the time of re-setting, the seconds indication of the watch is set correctly. The application of the re-set means of Figure 3 to a master flip-flop,

15 makes $Q-1$ and $\bar{Q}-1$ correspond to ϕ and $\bar{\phi}$ respectively in the phase condition of the binary divider circuit chain 33, and the clock ϕ of the binary divider circuit 33 is obtained by so setting it as to become at H level at the time of re-setting.

20 The invention offers the advantages of simplicity and economy of manufacture; low power consumption (with a consequent low rate of deterioration of the watch battery) if the watch is left at rest for long periods; reliability; and capability of embodiment in miniaturised circuit form—a particularly important advantage in the case of wristwatches where small size and compactness are highly desirable.

30 Attention is directed to the Specification of our Patent No. 1,287,542 which claims an invention which enables an electronic watch to be started without any appreciable time delay and therefore accurately in accordance with a time signal.

WHAT WE CLAIM IS:—

1. An electronic watch of the kind com-

prising a time standard oscillator, a frequency divider producing a lower frequency from a relatively high frequency output from said oscillator, and time indicating means driven by said lower frequency wherein said divider incorporates master-slave flip-flop binary circuits utilising complementary insulated gate field effect transistors; re-setting means are provided at least in one of the master or in one of the slave flip-flop circuits; and means providing a clock signal controlled flip-flop action are so arranged that a master or slave flip-flop circuit which is not provided with re-setting means is caused during the time in which re-setting is occurring to be subordinated to a slave or master flip-flop circuit which is provided with re-setting means.

2. A watch as claimed in claim 1, wherein the divider consists of a plurality of flip-flops in a binary divider chain; pulse shaping means are provided for pulse width shaping in an intermediate stage and in the last stage of said divider chain; and an input circuit of said chain is provided with means for cutting off the clock signal when re-setting the watch to the correct time.

3. An electronic watch having re-setting means substantially as herein described with reference to Figures 2 and 4 inclusive of the accompanying drawings.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
262 High Holborn,
London, WC1V 7EF.



in seconds is indicated by a mechanism not shown.

5 In obtaining the signal for setting the correct time in seconds there is a time delay of the order of $1/64$ sec, but this does not matter in practice. As will now be appreciated this use of part of the binary divider circuit chain of the watch for the pre-setting operation enables a substantial simplification of the circuitry to be effected. At the time of re-setting, the seconds indication of the watch is set correctly. The application of the re-set means of Figure 3 to a master flip-flop,

makes $Q-1$ and $\bar{Q}-1$ correspond to ϕ and

15 $\bar{\phi}$ respectively in the phase condition of the binary divider circuit chain 33, and the clock ϕ of the binary divider circuit 33 is obtained by so setting it as to become at H level at the time of re-setting.

20 The invention offers the advantages of simplicity and economy of manufacture; low power consumption (with a consequent low rate of deterioration of the watch battery) if the watch is left at rest for long periods; reliability; and capability of embodiment in miniaturised circuit form—a particularly important advantage in the case of wristwatches where small size and compactness are highly desirable.

30 Attention is directed to the Specification of our Patent No. 1,287,542 which claims an invention which enables an electronic watch to be started without any appreciable time delay and therefore accurately in accordance with a time signal.

WHAT WE CLAIM IS:—

1. An electronic watch of the kind com-

prising a time standard oscillator, a frequency divider producing a lower frequency from a relatively high frequency output from said oscillator, and time indicating means driven by said lower frequency wherein said divider incorporates master-slave flip-flop binary circuits utilising complementary insulated gate field effect transistors; re-setting means are provided at least in one of the master or in one of the slave flip-flop circuits; and means providing a clock signal controlled flip-flop action are so arranged that a master or slave flip-flop circuit which is not provided with re-setting means is caused during the time in which re-setting is occurring to be subordinated to a slave or master flip-flop circuit which is provided with re-setting means.

2. A watch as claimed in claim 1, wherein the divider consists of a plurality of flip-flops in a binary divider chain; pulse shaping means are provided for pulse width shaping in an intermediate stage and in the last stage of said divider chain; and an input circuit of said chain is provided with means for cutting off the clock signal when re-setting the watch to the correct time.

3. An electronic watch having re-setting means substantially as herein described with reference to Figures 2 and 4 inclusive of the accompanying drawings.

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
262 High Holborn,
London, WC1V 7EF.