

FLASH MEMORY CELL ON SeOI HAVING A SECOND CONTROL GATE BURIED UNDER THE INSULATING LAYER

FIELD OF THE INVENTION

The field of the invention is that of semiconductor devices, and more particularly that of memory devices comprising a plurality of memory cells.

The invention relates more particularly to a flash-type memory cell on a
5 semiconductor on insulator (SeOI) substrate, formed by a field-effect transistor FET that has a floating gate. The invention also relates to a memory array consisting of a plurality of memory cells of this type, and a method of controlling such a flash memory cell.

BACKGROUND OF THE INVENTION

10 The structure of a Flash-type memory cell is, globally, similar to that of a conventional MOSFET transistor, apart from the fact that the flash transistor has two gates instead of one. A top gate corresponds to the control gate of the transistor (as is the case for other MOS transistors), while another gate, the floating gate, is arranged between the control gate and the channel of the
15 transistor. An inter-gate dielectric layer is arranged between the control gate and the floating gate, while a gate dielectric layer is arranged between the floating gate and the channel. In as much as the floating gate is fully insulated by these dielectric layers, charges can be stored therein in a particularly durable manner.

20 The example of an NOR-type flash cell consisting of an NMOS transistor is described hereinbelow. Such a cell is equivalent in its inactive state to a logic "1" because a current flows through the channel by applying an appropriate voltage to the control gate.

Such a cell can be programmed (to set it to the "0" logic state) by the
25 following procedure that implements a hot electron injection phenomenon.

A very high voltage is applied to the control gate and to the drain. The channel is passing so that electrons flow from the source to the drain. The source-drain current is then sufficiently high for high-energy electrons (hot electrons resulting from the collision of the charges with the crystalline
30 network of the channel) to reach the floating gate by passing through the gate dielectric layer.

These hot electrons are then trapped in the floating gate, which alters the threshold voltage of the transistor. This mechanism decreases the voltage in the floating gate, and increases the apparent threshold voltage of the transistor (so that a higher voltage must be applied to the control gate for the transistor to be able to be passing – ON state). However, in normal reading conditions, the coupling of the two gates is insufficient to render the transistor passing. The read current of a programmed cell is thus “0”.

The cell can be erased (reset to the “1” logic state) by applying a low voltage to the control gate so that the transistor is not passing (OFF state), and whether it contained a “0” or “1” (that is to say, whether it was programmed or not) is unimportant. A very high voltage is applied to the drain so that a high voltage, of opposite polarity to that implemented in programming, is thus applied between the control gate and the source. The electrical field between the two gates increases until electrons can escape from the floating gate through the gate dielectric layer by tunnel effect.

During this erasure operation, the floating gate voltage decreases and the apparent threshold voltage of the transistor decreases.

In order to read the cell, a nominal read voltage V_{DD} is applied to the control gate. Depending on the status of the cell (programmed or erased), the transistor is either passing (ON state if it is erased) or blocked (OFF state if it is programmed).

A positive voltage is also applied to the drain (any value below V_{DD} to avoid disturbances while obtaining an adequate read signal). The drain will then be discharged if the transistor is ON. An analysis amplifier can then read either the current or the voltage drop.

Such flash cells have the drawback that a very high voltage must be applied to the control gate during programming operations to generate the hot electrons capable of reaching the floating gate through the gate dielectric layer.

As it happens, such high programming voltages are undesirable in as much as they increase the complexity of the design of the peripheral circuits

(dedicated circuitry implementing charge pumps is in particular necessary to generate these high voltages), they are likely to damage the cell and even disrupt the operation of nearby memory cells.

US 5,455,791A describes a EEPROM device fabricated on a SOI substrate having a back semiconducting layer and a front semiconducting layer separated by a buried insulating layer. The EEPROM device comprises two separate control gates, a front control gate and a back control gate. The back control gate is formed by the back semiconducting layer and a back gate contact made of a conductive material that extends all over the back semiconducting layer and is separated from the buried insulating layer by the back semiconducting layer. The back control gate is not suitable to be used for performing a programming operation because of the distance separating the back gate contact from the channel region.

BRIEF DESCRIPTION OF THE INVENTION

Embodiments of the invention seek to provide a response to these problems of design complexity regarding the peripheral circuits and of reliability of the cell and of the circuit in general.

The invention provides, according to a first aspect, a flash memory cell consisting of a FET transistor with a floating gate on a semiconductor on insulator substrate comprising a thin film of semiconductor material separated from a base substrate by an insulating layer, the transistor having, in the thin film, a channel, characterized in that it comprises two control gates, a front control gate being arranged above the floating gate and separated therefrom by an inter-gate dielectric and a back control gate being arranged within the base substrate directly under the insulating layer so as to be separated from the channel only by the insulating layer, the two control gates being designed to be used in combination to perform a cell programming operation.

Some preferred, but nonlimiting, embodiments of this memory cell are as follows:

- the back control gate extends under the entire width of the cell;

- the back control gate is located in such a way as to extend only facing the floating gate;
- the polarity of the back control gate is of the same type as that of the channel of the transistor;
- 5 – the back control gate is insulated in the base substrate by a well of opposite bias;
- the cell also comprises insulating regions extending depthwise into the base substrate to insulate the back control gate;
- the cell is of the fully depleted type;
- 10 – the floating gate is arranged on the surface of the thin film and is insulated from the channel in the thin film via a gate dielectric layer;
- the floating gate is formed in a trench made in the channel, and insulated from the channel via a gate dielectric layer arranged on the walls of the trench;
- 15 – the FET transistor comprises a source region and a drain region that are arranged asymmetrically in the thin film on either side of the floating gate formed in the channel so that the drain region is closer to the floating gate than the source region is.

According to another aspect, the invention relates to a memory array
 20 comprising a plurality of cells according to the first aspect of the invention arranged in rows and in columns, in which a back gate line is coupled to the back control gate of each of the cells along a row or a column.

A word line can be coupled to the front control gate of each of the cells along a column, the back gate line extending in parallel to the word line.

25 According to yet another aspect, the invention relates to a memory array comprising a plurality of memory cells arranged in rows and in columns, in which a first set of cells consists of flash cells with a floating gate recessed in the channel in accordance with the first aspect of the invention, and a second set of cells consists of DRAM cells with a floating channel and control
 30 gate recessed in the channel.

According to yet another aspect, the invention provides a method of fabricating a memory array comprising a first set of flash memory cells with floating gate recessed in the channel that conform to the first aspect of the invention and a second set of DRAM memory cells with floating channel and control gate recessed in the channel. The method comprises:

- a first series of steps common to said first and second sets of cells, comprising, for each cell:
 - the formation of a trench in the thin film,
 - the coating of the walls of the trench by the gate dielectric layer,
 - the filling of the trench with a gate material;
- said first series of steps being followed:
 - for each of the cells of the first set, by the formation of the inter-gate dielectric layer on the trench and the formation of the front control gate on the inter-gate dielectric layer,
 - for each of the cells of the second set, by the formation of a control gate directly on the trench.

An embodiment of the invention also extends to a method of controlling a memory cell according to the first aspect of the invention, in which, during a cell programming operation, the front control gate and the back control gate are used in combination by applying a first positive voltage to the front control gate and a second positive voltage to the back control gate, said first voltage being less than the voltage needed to programme the cell when no voltage is applied to the back control gate.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, aims and advantages of the present invention will become more apparent from reading the following detailed description of preferred embodiments thereof, given as nonlimiting examples, and with reference to the appended drawings in which:

- Figure 1 represents one possible embodiment of a fully depleted planar flash memory cell according to the invention;

- Figure 2 represents one possible embodiment of a flash memory cell with fully depleted recessed floating gate according to the invention;
- Figures 3a-3k illustrate different steps of sequences in forming and insulating a back control gate in the base substrate;
- 5 – Figure 4 represents a topology of a memory array according to a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figure 1, a flash memory cell 1 is represented, consisting
 10 of an FET transistor with floating gate on a semiconductor on insulator substrate comprising a thin film of semiconductor material separated from a base substrate 5 by an insulating layer, typically a buried oxide BOX layer.

The semiconductor on insulator substrate is, for example, a silicon on insulator (SOI) substrate.

15 According to a preferred embodiment, the insulating layer is a layer of SiO_2 . According to an advantageous variant, the insulating layer comprises a layer of Si_3N_4 sandwiched between two layers of SiO_2 .

The transistor comprises, in the thin film, a source region 2, a drain region 3 and a channel 4 separating the source region 2 from the drain
 20 region 3.

In Figure 1, the drain D and the source S are in contact with the buried oxide BOX layer so that the FET transistor is fully depleted.

The source S can thus be shared between two adjacent memory cells (along a row of a memory array extending in the plane of Figure 2a; the
 25 columns of the memory array extending perpendicularly to the plane of Figure 2a). Such sharing means that the space occupied by a memory cell can be reduced.

It will be understood that the invention is not limited to a fully depleted memory cell but also extends to a memory cell on partially depleted SeOI.
 30 Conventionally, as is known per se, it is then necessary to insulate the cells along a row of the memory array in order to insulate the channels of adjacent

cells from one another. This is conventionally done using insulating trenches (according to the STI – “shallow trench isolation” – technique) extending depthwise from the surface of the substrate to the BOX.

Referring to Figure 1, the flash memory cell 1 comprises a floating gate 10 extending on the surface of the substrate above the channel 4. The floating gate 10 is insulated from the channel via a gate dielectric layer 11.

A front control gate 12 is arranged in a conventional manner that is known per se above the floating gate 10, an inter-gate dielectric layer 13 being interposed between the front control gate 12 and the floating gate 10.

The flash memory cell 1 also comprises a back control gate 6 arranged within the base substrate 5 directly under the insulating BOX layer, so as to be separated from the channel 4, only by the insulating BOX layer.

The memory cell thus has two control gates: the front control gate 12 used conventionally, and the back control gate 6 proposed by the invention which is in particular designed to be used in combination with the front control gate to perform a cell programming operation.

As a purely illustrative example, the thickness of the thin film of the semiconductor on insulator substrate is between 1.5 nm and 50 nm, the thickness of the insulating layer is between 1.5 nm and 50 nm.

Figure 2 illustrates another possible embodiment of a fully depleted flash memory cell 10 according to the invention, in which the floating gate is not arranged on the surface of the substrate, but is, on the contrary, embedded in the channel. The floating gate 20 in this case fills a trench formed in the thickness of the channel 4, a gate dielectric layer 21 being arranged on the walls of the trench so as to insulate the floating gate 20 from the channel 4.

This second embodiment is advantageous in that the back control gate 6 is then situated relatively close to the floating gate 20 recessed in the channel. This second embodiment thus allows greater thin film thicknesses, for example up to 300 nm.

In each of the embodiments described hereinabove, the back control gate 6 increases the current flowing in the channel during a cell programming operation (the back control gate thus provides a *boost* effect).

Because the current is higher, the current density also increases since the dimensions of the flash transistor remain substantially minimal. Using the back control gate therefore makes it possible to obtain hot electrons at a lower voltage when programming. The programming voltages can thus be lowered, which considerably helps in the design of the peripheral circuits and strengthens the reliability of the cell and of the circuit in general.

As an illustrative example for the current technologies implemented in 2009, the programming is done with voltages of the order of 7 to 9V, erasure with voltages of the order of -4V to -6V. The invention overall makes it possible to lower by approximately 40% the voltages required for programming, and therefore to have roughly the same amplitudes for the programming and erasure operations.

It will be noted that, instead of lowering the programming voltages, it is possible to utilize programming voltages of the same amplitude. Use of the back control gate then makes it possible to reduce the time needed to carry out the programming which is of particular interest for a flash cell which is conventionally not very fast in write mode.

The polarity of the back control gate 6 is preferentially chosen so as to be of the same type as that of the channel of the transistor (or an N type polarity for an NPN-type transistor, a P type polarity for a PNP transistor). A threshold voltage of the bottom transistor is defined in such a way.

However, the invention also extends to a back gate that has a working voltage (polarity opposite to that of the FET transistor). In this particular case however, the threshold voltage of the transistor is increased and it is then necessary to apply a higher voltage to the back control gate in a cell programming operation.

According to one embodiment that is not represented, the source region and the drain region of the FET transistor are arranged asymmetrically in the

thin film on either side of the floating gate formed in the channel so that the drain region is closer to the floating gate than the source region is.

A cell erasure operation can be modelled by two series coupling capacitors, one between the drain and the floating gate, the other between
 5 the floating gate and the front control gate. The floating gate voltage then follows the drain voltage according to a coupling that depends on the ratio between these coupling capacitors. By implementing an additional N- or N+ implant in the drain region so that it is closer to the floating gate than the source region is, the drain-floating gate coupling is increased. The electrical
 10 field between the front control gate and the floating gate then increases until, by tunnel effect, electrons pass from the floating gate to the front control gate.

Figures 3a-3k represent different steps of possible sequences in constructing and insulating a back control gate in the base substrate. These
 15 figures show both the case of a P type and an N type back control gate.

Figure 3a represents an SeOI substrate comprising a thin film of semiconductor material 30 separated from a base substrate 31 by an insulating BOX layer.

In a first step, alignment marks are defined in the SeOI substrate so as
 20 to allow for the necessary alignment in later masking and pattern formation steps (formation of wells, back control gates, insulating structures, etc.).

This first substrate marking step thus consists in forming, in the substrate, a groove, a trench, a mesa, or any other sign (such as a cross for example).

25 Figure 3b to this end illustrates the formation of mesas by surface layer etching. For this, standard CMOS fabrication methods are used.

Figures 3c, 3d and 3e represent different possible approaches for the formation of "wells" buried under the insulating BOX layer, with a view to ultimately insulating one or more back control gates with respect to the base
 30 substrate 31.

In each of Figures 3c, 3d and 3e, the base substrate 31 is doped so as to exhibit, in a top layer thereof, an N-type conductivity. The doping level is typically between $1 \cdot 10^{15}$ and $5 \cdot 10^{16} \text{ cm}^{-3}$.

In Figure 3c, a P-type well 32 has been produced, by dopant
5 implantation, beneath the insulating BOX layer in the N-type base substrate 31. The P-type well 32 is thus insulated from the N-type substrate by a pn junction.

In Figure 3d, both a P-type well 32 and an N-type well 33 have been produced. The wells 32, 33 are insulated from one another by a pn junction.

10 In Figure 3e, both a P-type well 32 and an N-type well 33 have been produced, as in Figure 3d. An STI-type insulating trench 38 has also been produced, extending, from the surface of the SeOI substrate, under the insulating BOX layer, depthwise in the base substrate 31, this trench providing the insulation between the wells 32, 33.

15 The doping level in the wells of Figures 3c, 3d and 3e is typically between $5 \cdot 10^{16}$ and $5 \cdot 10^{18} \text{ cm}^{-3}$.

It will be noted that the steps needed to fabricate the structures represented in Figures 3c, 3d and 3e are based on standard CMOS fabrication methods.

20 Starting from the structure represented in Figures 3c (respectively Figure 3d and Figure 3e), dopant implantation is then implemented in order to form back control gates 34, 35, 36, 37 within the base substrate, directly under the insulating BOX layer as represented in Figure 3f (respectively Figure 3g and Figure 3h).

25 The doping level to form a back control gate is typically between $5 \cdot 10^{18}$ and $5 \cdot 10^{20} \text{ cm}^{-3}$.

As represented in Figures 3g and 3h, the back control gate 34, 35, 36, 37 is insulated from the base substrate 5 by a well 32, 33 of opposite bias (P-type well 32 for the N-type back control gate 34, 36; N-type well 33 for a P-type back control gate 35, 37).

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In the case of Figure 3f, a well has been produced solely for a single back control gate bias (P well 32 insulating an N back control gate 34, while a P-type back control gate 35 is arranged directly in the N-biased base substrate 31).

5 It will be noted that, generally, the well voltage is chosen so that the diode created by the electrical node between the back control gate and the well is always reversed, the diode then insulating the back control gate from the well and from anything that it might contain (other back control gates in particular).

10 According to a first embodiment represented in Figure 3h, the back control gate 36, 37 extends under the entire width of the well 32, 33. In this particular case, the insulating trench 35 insulates the back control gates 37, 38 from one another.

15 According to another embodiment represented in Figure 3g, the back control gate 34, 35 is localized in such a way as to extend only over a portion of the width of the well 32, 33. It will be noted that an insulating trench can also be provided when the back control gate is localized, by thus contributing to the insulation of the wells.

20 According to a variant embodiment that is not represented, a second insulating layer, arranged in the base substrate below the insulating BOX layer, can wholly or partly contribute to insulating a back control gate from the base substrate.

25 Starting from the structure represented in Figure 3f (respectively Figure 3g and Figure 3h), the mesas are then filled, and, where appropriate, the insulating trenches are also filled, by deposition of a dielectric. This filling implements standard passivation treatments of the side walls, filling and surface planarization.

30 One or more transistors (of the same type) can then be formed in each of the regions of the thin film 30 delimited by the insulating regions 39 formed by the duly deposited dielectric.

It will have been understood from the foregoing that the invention provides for a flash memory cell that has an individualized back control gate. At the very least, only the cells arranged along one and the same row or one and the same column of the memory array share the same back control gate. A back gate line is thus coupled to the back control gate of each of the cells along a row or a column.

In a manner that is known per se, a word line is coupled to the front control gate of each of the cells along a column of the memory array. Preferentially, provision is made for the back gate line to extend in parallel to the word line (the back control gate effectively assisting the front control gate during programming).

Figure 4 shows a topology of a memory array conforming to a preferred embodiment of the invention. In this figure, the dotted lines identify two adjacent memory cells C1 and C2, as described previously. Also shown are the various access or control lines to the different regions of the transistors: source line SL linking the source regions S of each of the transistors, bit lines BL1, BL2 used to address the drain region of each of the transistors, word line WL1, WL2 linking the front control gate of each of the transistors, back gate lines BG1, BG2 used to address the back control gate of each of the transistors. In the preferred embodiment illustrated by this Figure 4, the back control gate BG1, BG2 associated with a memory cell C1-C2 extends in parallel with the word line WL1, WL2 coupled to the front control gate of the transistor forming the memory cell.

In the context of the invention, the individualized back control gate is used dynamically: the voltage that is applied to it is effectively modulated according to the type of cell control operations (programming, erasure, read, hold).

According to a preferred embodiment, the back control gate voltage is positive for programming (which means that the programming voltage that has to be applied to the front control gate can be reduced) and zero for the other operations.

As a variant, the voltage applied to the back control gate can be negative in a hold operation, to allow for a better retention of the charges in the floating gate.

The invention is also advantageous in that it makes it possible to
 5 fabricate easily on one and the same substrate both flash-type memory cells and DRAM-type memory cells with floating channel (DRAM being the acronym for "Dynamic Random Access Memory").

Referring to Figures 1 and 2, the elimination of the inter-gate oxide layer 13, 23, or more directly the joining of the floating gate 11, 21 and the front
 10 control gate 12, 22 in a single control gate makes it possible to change effectively from a flash memory cell to a DRAM memory cell in which the floating channel 4 can accumulate charges.

It will be noted that the back control gate is also advantageous for a DRAM cell in that it makes it possible to modify the effective threshold
 15 voltage. An appropriate control of the back control gate thus makes it possible to reduce the effective threshold voltage (for example, a positive voltage applied to a back control gate with no working function), which makes it possible to increase the conduction current, advantageously in operations in which the circuit has to be as powerful as possible. The effective threshold
 20 voltage can also be increased (via a negative voltage applied to a back control gate with no working function), which makes it possible to reduce the leaks, advantageously in a globally inactive state of the circuit.

The invention thus extends to a method of fabricating a hybrid memory array comprising a first set of flash memory cells and a second set of DRAM
 25 memory cells. The method comprises more specifically:

- a first series of steps common to said first and second sets of cells, comprising, for each cell:
 - the formation of a trench in the thin film,
 - the coating of the walls of the trench by the gate dielectric layer,
 - 30 ○ the filling of the trench with a gate material;
- said first series of steps being followed:

- for each of the cells of the first set, by the formation of the inter-gate dielectric layer on the trench and the formation of the front control gate on the inter-gate dielectric layer so as to form flash cells with floating gate,
- 5 ○ for each of the cells of the second set, by the formation of a control gate directly on the trench, so as to form DRAM cells with floating gate.

It will also be noted that the back control gate of a flash cell according to the first aspect of the invention can also be used as DRAM cell control gate, the channel 4 then forming a floating channel for the DRAM cell. A hybrid
10 memory cell is thus formed, comprising a flash cell on the front face and a DRAM cell on the back face.

CLAIMS

1. Flash memory cell consisting of a FET transistor with a floating gate on a semiconductor on insulator substrate comprising a thin film of semiconductor material separated from a base substrate by an insulating layer, the transistor having, in the thin film, a channel,

characterized in that it comprises two control gates, a front control gate being arranged above the floating gate and separated therefrom by an inter-gate dielectric and a back control gate being arranged within the base substrate directly under the insulating layer so as to be separated from the channel only by the insulating layer, the two control gates being designed to be used in combination to perform a cell programming operation.

2. Memory cell according to Claim 1, in which the back control gate extends under the entire width of the cell.

3. Memory cell according to Claim 1, in which the back control gate is located in such a way as to extend only facing the floating gate.

4. Memory cell according to one of the preceding claims, in which the polarity of the back control gate is of the same type as that of the channel of the transistor.

5. Memory cell according to one of the preceding claims, in which the back control gate is insulated in the base substrate by a well of opposite bias.

6. Memory cell according to one of the preceding claims, also comprising insulating trenches extending depthwise into the base substrate to insulate the back control gate.

7. Memory cell according to one of the preceding claims, characterized in that it is of the fully depleted type.

8. Memory cell according to one of Claims 1 to 7, in which the floating gate is arranged on the surface of the thin film and is insulated from the channel in the thin film via a gate dielectric layer.

9. Memory cell according to one of Claims 1 to 7, in which the floating gate is formed in a trench made in the channel, and insulated from the channel via a gate dielectric layer arranged on the walls of the trench.

10. Memory cell according to Claim 9, in which the FET transistor comprises a source region and a drain region that are arranged asymmetrically in the thin film on either side of the floating gate formed in the channel so that the drain region is closer to the floating gate than is the source region.

11. Memory array comprising a plurality of cells according to one of Claims 1 to 10 arranged in rows and in columns, in which a back gate line is coupled to the back control gate of each of the cells along a row or a column.

12. Memory array according to Claim 11, in which a word line is coupled to the front control gate of each of the cells along a column and in which the back gate line extends parallel to the word line.

13. Memory array comprising a plurality of memory cells arranged in rows and in columns, in which a first set of cells of said plurality of cells consists of flash cells in accordance with one of Claims 9 or 10, and a second set of

cells of said plurality of cells consists of DRAM cells with floating channel and control gate recessed in the channel.

14. Method of fabricating a memory array according to Claim 13, comprising:

- 5 – a first series of steps common to said first and second sets of cells, comprising, for each cell:
 - the formation of a trench in the thin film,
 - the coating of the walls of the trench by the gate dielectric layer,
 - the filling of the trench with a gate material;
- 10 – said first series of steps being followed:
 - for each of the cells of the first set, by the formation of the inter-gate dielectric layer on the trench and the formation of the front control gate on the inter-gate dielectric layer,
 - for each of the cells of the second set, by the formation of a
 - 15 control gate directly on the trench.

15. Method of controlling a memory cell according to one of Claims 1 to 10, in which, during a cell programming operation, the front control gate and the back control gate are used in combination by applying a first positive voltage

20 to the front control gate and a second positive voltage to the back control gate, said first voltage being less than the voltage needed to programme the cell when no voltage is applied to the back control gate.

FLASH MEMORY CELL ON SeOI HAVING A SECOND CONTROL GATE
BURIED UNDER THE INSULATING LAYER

DESCRIPTIVE ABSTRACT

The invention relates, according to a first aspect, to a flash memory cell (1, 10) consisting of an FET transistor with a floating gate (10, 20) on a semiconductor on insulator substrate comprising a thin film of semiconductor material separated from a base substrate (5) by an insulating (BOX) layer, the transistor having, in the thin film, a channel (4), characterized in that it comprises two control gates, a front control gate (12, 22) being arranged above the floating gate (10, 20) and separated therefrom by an inter-gate dielectric (13, 23) and a back control gate (6, 34-37) being arranged within the base substrate (5) directly under the insulating (BOX) layer so as to be separated from the channel (4) only by the insulating (BOX) layer, the two control gates (10, 20; 6, 34-37) being designed to be used in combination to perform a cell programming operation. The invention also extends to a memory array comprising a plurality of memory cells according to the first aspect of the invention, and to a method of fabricating such a memory cell.

FIGURE 2