

Abstract

SELF-ALIGNED FLOATING GATE FOR MEMORY APPLICATION USING SHALLOW TRENCH ISOLATION

A method of to make a self-aligned floating gate in a memory device. The method patterns the floating gate (FG) using the trench etch for the shallow trench isolation (STI). Because the floating gate (FG) is adjacent to the raised STI, sharp corners are eliminated between the FG and CG thereby increasing the effectiveness of the intergate dielectric layer. The method includes: forming an first dielectric layer (gate oxide) and a polysilicon layer over a substrate. We etch through the first dielectric oxide layer and the polysilicon layer and into the substrate to form a trench. The remaining first dielectric layer and polysilicon layer function as a tunnel dielectric layer and a floating gate. The trench is filled with an isolation layer. The masking layer is removed. An intergate dielectric layer and a control gate are formed the floating gate and the isolation layer.

(FIGURE 1B IS SUGGESTED FOR PUBLICATION)